128Kx36 Pipelined SRAM with NoBL™ Architecture

Features

- **Zero Bus Latency, no dead cycles between write and read cycles**
- **Fast clock speed: 143, 133 and 100 MHzInternally synchronized registered outputs eliminate the need to control OE**
- **Single 3.3V –5% and +5% power supply V_{CC}**
- **Separate V_{CCQ} for 3.3V or 2.5V I/O**
- **Single R/W (Read/Write) control pin**
- **Positive clock-edge triggered, address, data, and control signal registers for fully pipelined applications**
- **Interleaved or linear 4-word burst capability**
- **Individual byte write (BWa–BWd) control (may be tied LOW)**
- **CKE pin to enable clock and suspend operations**
- **Three chip enables for simple depth expansion**
- **Snooze Mode for low-power standby**
- **Automatic power-down**
- **Packaged in a JEDEC standard 100-pin TQFP package**

Functional Description

The CY7C1350A/GVT71128ZC36 SRAM are designed to eliminate dead cycles when transitioning from Read to Write or vice versa. This SRAM is optimized for 100 percent bus utilization and achieve Zero Bus Latency (ZBL)/No Bus Latency™ (NoBL™). It integrates 131,072x36 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. The Cypress Synchronous Burst SRAM family employs high-speed, low-power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high-valued resistors.

All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, depth-expansion Chip Enables ($\overline{CE}$, $\overline{CE_2}$ and CE_2), Cycle Start Input (ADV/$\overline{LD}$), Clock Enable ($\overline{CKE}$), Byte Write Enables ($\overline{BWa}$, $\overline{BWb}$, $\overline{BWc}$, and $\overline{BWd}$), and Read-Write Control (R/$\overline{W}$).

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later, its associated data occurs, either read or write.

A clock enable ($\overline{CKE}$) pin allows operation of the CY7C1350A/GVT71128ZC36 to be suspended as long as necessary. All synchronous inputs are ignored when ($\overline{CKE}$) is HIGH and the internal device registers will hold their previous values.

There are three chip enable pins ($\overline{CE}$, CE_2, $\overline{CE_2}$) that allow the user to deselect the device when desired. If any one of these three are not active when ADV/$\overline{LD}$ is LOW, no new memory operation can be initiated and any burst cycle in progress is stopped. However, any pending data transfers (read or write) will be completed. The data bus will be in high-impedance state two cycles after chip is deselected or a write cycle is initiated.

The CY7C1350A/GVT71128ZC36 has an on-chip 2-bit burst counter. In the burst mode, the CY7C1350A/GVT71128ZC36 provides four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the MODE input pin. The MODE pin selects between linear and interleaved burst sequence. The ADV/$\overline{LD}$ signal is used to load a new external address (ADV/$\overline{LD}$ = LOW) or increment the internal burst counter (ADV/$\overline{LD}$ = HIGH)

Output Enable ($\overline{OE}$), Snooze Enable (ZZ) and burst sequence select (MODE) are the asynchronous signals. $\overline{OE}$ can be used to disable the outputs at any given time. ZZ may be tied to LOW if it is not used.

The CY7C1350A/GVT71128ZC36 utilizes a high-performance high-volume 3.3V CMOS process, and is packaged in a JEDEC Standard 14-mm x 20-mm 100-pin plastic quad flatpack (TQFP) for high board density.

Selection Guide

		7C1350A-143 71128ZC36-4	7C1350A-133 71128ZC36-5	7C1350A-133 71128ZC36-6	7C1350A-100 71128ZC36-7
Maximum Access Time (ns)		4.0	4.2	4.2	5.0
Maximum Operating Current (mA)	Com'l	400	380	380	300
Maximum CMOS Standby Current (mA)	Com'l	10	10	10	10

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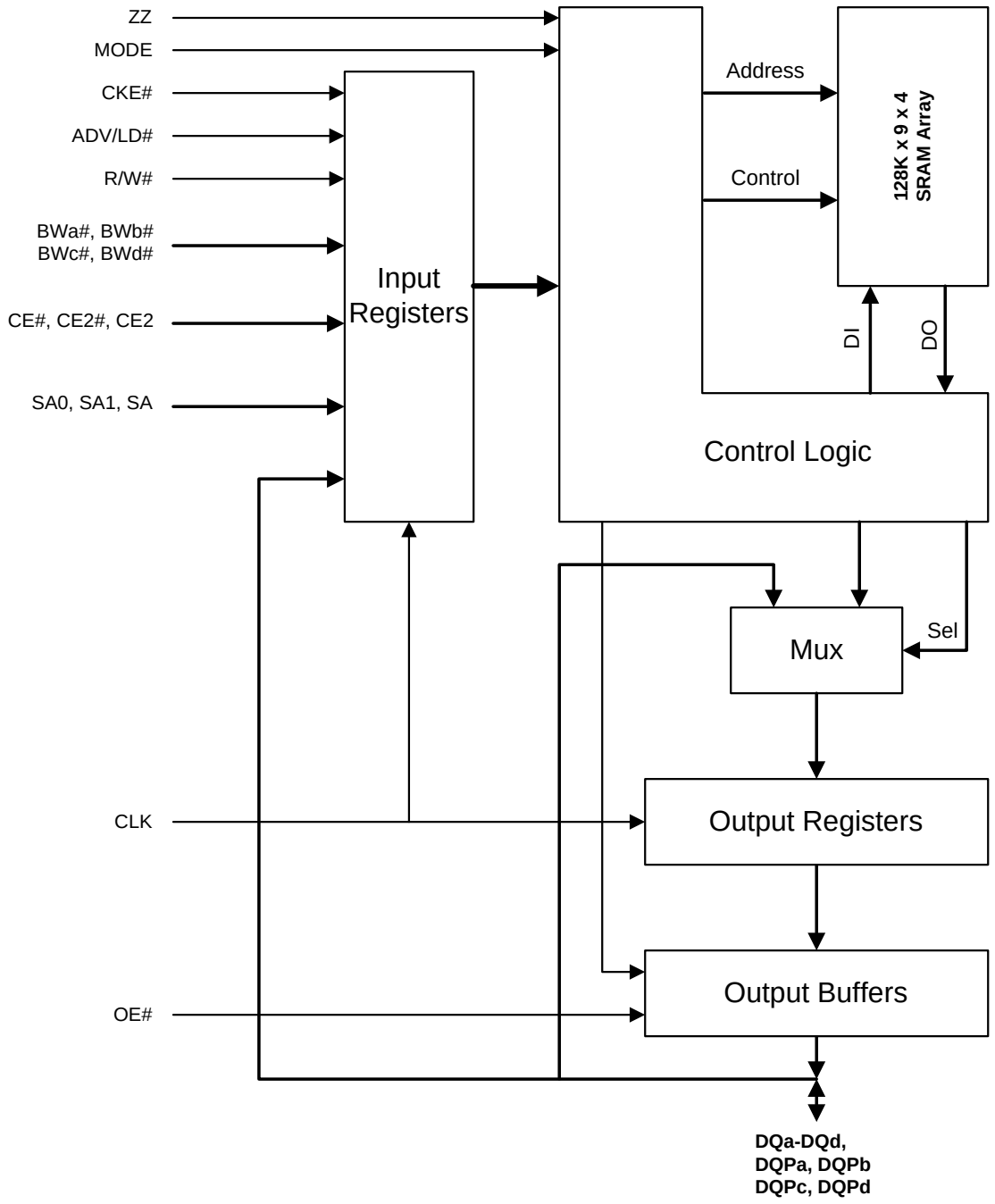
Functional Block Diagram—128Kx36[1]



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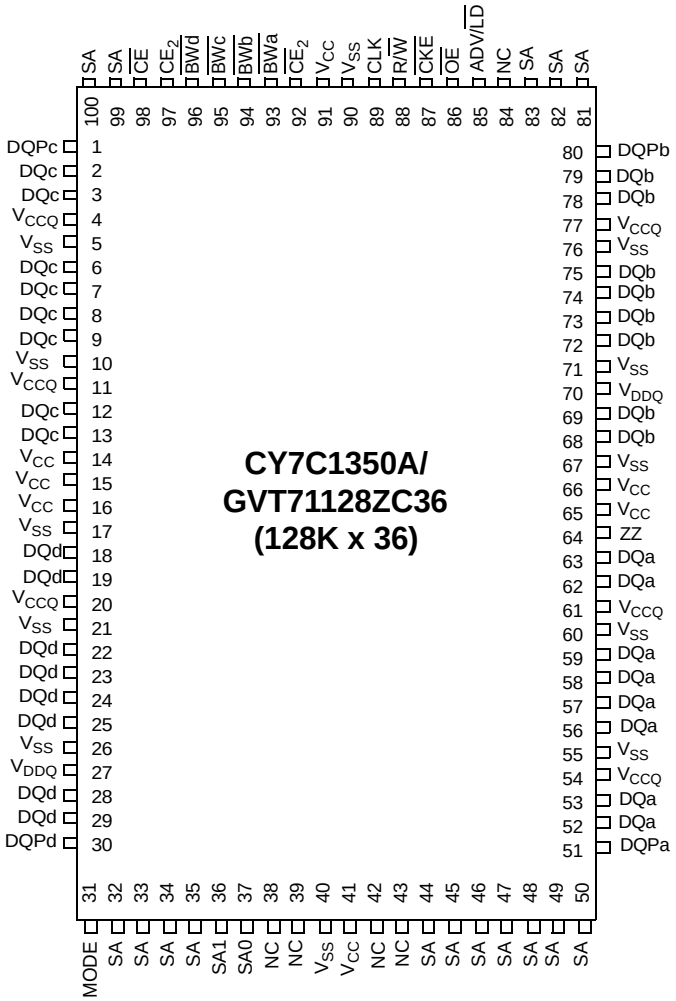
Note:
1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

Pin Configurations

100-Pin TQFP Package



Pin Descriptions

TQFP Pins	Name	Type	Description
37, 36, 32, 33, 34, 35, 44, 45, 46, 47, 48, 49, 50, 81, 82, 83, 99, 100	SA0, SA1, SA	Input-Synchronous	Synchronous Address Inputs: The address register is triggered by a combination of the rising edge of CLK, ADV/LD LOW, CKE LOW and true chip enables. SA0 and SA1 are the two least significant bits of the address field and set the internal burst counter if burst cycle is initiated.
93, 94, 95, 96	$\overline{BWa}$, $\overline{BWb}$, $\overline{BWc}$, $\overline{BWd}$	Input-Synchronous	Synchronous Byte Write Enables: Each 9-bit byte has its own active LOW byte write enable. On load write cycles (when R/$\overline{W}$ and ADV/$\overline{LD}$ are sampled LOW), the appropriate byte write signal (BWx) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte write signals are ignored when R/$\overline{W}$ is sampled HIGH. The appropriate byte(s) of data are written into the device two cycles later. BWa controls DQa pins; BWb controls DQb pins; BWc controls DQc pins; BWd controls DQd pins. BWx can all be tied LOW if always doing write to the entire 36-bit word.

Pin Descriptions (continued)

TQFP Pins	Name	Type	Description
87	$\overline{CKE}$	Input-Synchronous	Synchronous Clock Enable Input: When $\overline{CKE}$ is sampled HIGH, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of $\overline{CKE}$ sampled HIGH on the device outputs is as if the LOW-to-HIGH clock transition did not occur. For normal operation, $\overline{CKE}$ must be sampled LOW at rising edge of clock.
88	R/$\overline{W}$	Input-Synchronous	Read Write: R/$\overline{W}$ signal is a synchronous input that identifies whether the current loaded cycle and the subsequent burst cycles initiated by ADV/$\overline{LD}$ is a Read or Write operation. The data bus activity for the current cycle takes place two clock cycles later.
89	CLK	Input-Synchronous	Clock: This is the clock input to CY7C1350A/GVT71128ZC36. Except for $\overline{OE}$, ZZ and MODE, all timing references for the device are made with respect to the rising edge of CLK.
98, 92	$\overline{CE}$, $\overline{CE_2}$	Input-Synchronous	Synchronous Active LOW Chip Enable: $\overline{CE}$ and $\overline{CE_2}$ are used with CE_2 to enable the CY7C1350A/GVT71128ZC36. $\overline{CE}$ or $\overline{CE_2}$ sampled HIGH or CE_2 sampled LOW, along with ADV/$\overline{LD}$ LOW at the rising edge of clock, initiates a deselect cycle. The data bus will be High-Z two clock cycles after chip deselect is initiated.
97	CE_2	Input-Synchronous	Synchronous Active HIGH Chip Enable: CE_2 is used with $\overline{CE}$ and $\overline{CE_2}$ to enable the chip. CE_2 has inverted polarity but otherwise is identical to $\overline{CE}$ and $\overline{CE_2}$.
86	$\overline{OE}$	Input	Asynchronous Output Enable: $\overline{OE}$ must be LOW to read data. When $\overline{OE}$ is HIGH, the I/O pins are in high-impedance state. $\overline{OE}$ does not need to be actively controlled for read and write cycles. In normal operation, $\overline{OE}$ can be tied LOW.
85	ADV/$\overline{LD}$	Input-Synchronous	Advance/Load: ADV/$\overline{LD}$ is a synchronous input that is used to load the internal registers with new address and control signals when it is sampled LOW at the rising edge of clock with the chip is selected. When ADV/$\overline{LD}$ is sampled HIGH, then the internal burst counter is advanced for any burst that was in progress. The external addresses and R/$\overline{W}$ are ignored when ADV/$\overline{LD}$ is sampled HIGH.
31	MODE	Input-Static	Burst Mode: When MODE is HIGH or NC, the interleaved burst sequence is selected. When MODE is LOW, the linear burst sequence is selected. MODE is a static DC input.
64	ZZ	Input-Asynchronous	Snooze Enable: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC.
52, 53, 56-59, 62, 63, 68, 69, 72-75, 78, 79 2, 3, 6–9, 12, 13 18, 19, 22–25, 28, 29	DQa DQb DQc DQd	Input/ Output	Data Inputs/Outputs: Both the data input path and data output path are registered and triggered by the rising edge of CLK. Byte “a” is DQa pins; Byte “b” is DQb pins; Byte “c” is DQc pins; Byte “d” is DQd pins.
51, 80, 1, 30	DQPa, DQPb, DQPc, DQPd	Input/ Output	Parity Inputs/Outputs: Both the data input path and data output path are registered and triggered by the rising edge of CLK. DQPa is parity bit for Byte “a”; DQPb is parity bit for Byte “b”; DQPc is parity bit for Byte “c”; DQPd is parity bit for Byte “d”.
14, 15, 16, 41, 65, 66, 91	V_{CC}	Supply	Power Supply: +3.3V –5% and +5%.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	Ground	Ground: GND.
4, 11, 20, 27, 54, 61, 70, 77	V_{CCQ}	I/O Supply	Output Buffer Supply: +3.3V –0.165V and +0.165V for 3.3V I/O. +2.5V –0.125V and +0.4V for 2.5V I/O.
38, 39, 42, 43, 83, 84	NC	-	No Connect: These signals are not internally connected. It can be left floating or be connected to V_{CC} or to GND.

Interleaved Burst Address Table (MODE = V_{CC} or NC)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)[2]
A...A_{00}	A...A_{01}	A...A_{10}	A...A_{11}
A...A_{01}	A...A_{00}	A...A_{11}	A...A_{10}
A...A_{10}	A...A_{11}	A...A_{00}	A...A_{01}
A...A_{11}	A...A_{10}	A...A_{01}	A...A_{00}

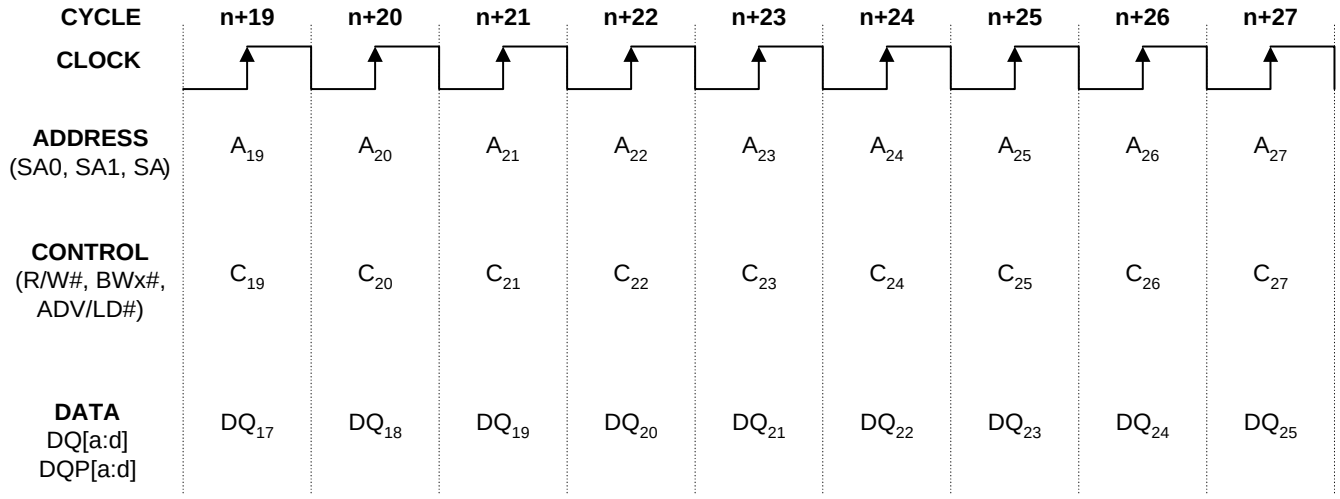
Linear Burst Address Table (MODE = V_{SS})

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)[2]
A...A_{00}	A...A_{01}	A...A_{10}	A...A_{11}
A...A_{01}	A...A_{10}	A...A_{11}	A...A_{00}
A...A_{10}	A...A_{11}	A...A_{00}	A...A_{01}
A...A_{11}	A...A_{00}	A...A_{01}	A...A_{10}

Partial Truth Table for Read/Write[3]

Function	R/$\overline{W}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
Read	H	X	X	X	X
No Write	L	H	H	H	H
Write Byte a (DQa, DQPa)[4]	L	L	H	H	H
Write Byte b (DQb, DQPb)[4]	L	H	L	H	H
Write Byte c (DQc, DQPc)[4]	L	H	H	L	H
Write Byte d (DQd, DQPd)[4]	L	H	H	H	L
Write all bytes	L	L	L	L	L

Functional Timing Diagram[5, 6]



Notes:

2. Upon completion of the Burst sequence, the counter wraps around to its initial state and continues counting.
3. L means logic LOW. H means logic HIGH. X means "Don't Care."
4. Multiple bytes may be selected during the same cycle.
5. This assumes that $\overline{CKE}$, $\overline{CE}$, CE_2 and $\overline{CE_2}$ are all True.
6. All addresses, control and data-in are only required to meet set-up and hold time with respect to the rising edge of clock. Data out is valid after a clock-to-data delay from the rising edge of clock.

Truth Table[7, 8, 9, 10, 11, 12, 13, 14, 15]

OPERATION	Previous Cycle	Address Used	R/$\overline{W}$	ADV/$\overline{LD}$	$\overline{CE}$	$\overline{CKE}$	$\overline{BWx}$	$\overline{OE}$	DQ (2 cycles later)
Deselect Cycle	X	X	X	L	H	L	X	X	High-Z
Continue Deselect/NOP[16]	Deselect	X	X	H	X	L	X	X	High-Z
Read Cycle (Begin Burst)	X	External	H	L	L	L	X	X	Q
Read Cycle (Continue Burst)[16]	Read	Next	X	H	X	L	X	X	Q
Dummy Read (Begin Burst)[17]	X	External	H	L	L	L	X	H	High-Z
Dummy Read (Continue Burst)[16, 17]	Read	Next	X	H	X	L	X	H	High-Z
Write Cycle (Begin Burst)	X	External	L	L	L	L	L	X	D
Write Cycle (Continue Burst)[16]	Write	Next	X	H	X	L	L	X	D
Abort Write (Begin Burst)[17]	X	External	L	L	L	L	H	X	High-Z
Abort Write (Continue Burst)[16, 17]	Write	Next	X	H	X	L	H	X	High-Z
Ignore Clock Edge/NOP[18]	X	X	X	H	X	H	X	X	-

Notes:

7. L means logic LOW. H means logic HIGH. X means "Don't Care." High-Z means High Impedance. $\overline{BWx}$ = L means [$\overline{BWa}$*$\overline{BWb}$*$\overline{BWc}$*$\overline{BWd}$] equals LOW. $\overline{BWx}$ = H means [$\overline{BWa}$*$\overline{BWb}$*$\overline{BWc}$*$\overline{BWd}$] equals HIGH.
8. $\overline{CE}$ equals H means $\overline{CE}$ and $\overline{CE_2}$ are LOW along with CE_2 being HIGH. $\overline{CE}$ equals L means $\overline{CE}$ or $\overline{CE_2}$ is HIGH or CE_2 is LOW. $\overline{CE}$ equals X means $\overline{CE}$, $\overline{CE_2}$, and CE_2 are "Don't Care."
9. $\overline{BWa}$ enables WRITE to byte "a" (DQa pins). $\overline{BWb}$ enables WRITE to byte "b" (DQb pins). $\overline{BWc}$ enables WRITE to byte "c" (DQc pins). $\overline{BWd}$ enables WRITE to byte "d" (DQd pins).
10. The device is not in Snooze Mode, i.e. the ZZ pin is LOW.
11. During Snooze Mode, the ZZ pin is HIGH and all the address pins and control pins are "Don't Care." The SNOOZE MODE can only be entered two cycles after the Write cycle, otherwise the Write cycle may not be completed.
12. All inputs, except $\overline{OE}$, ZZ, and MODE pins, must meet set-up time and hold time specification against the clock (CLK) LOW-to-HIGH transition edge.
13. $\overline{OE}$ may be tied to LOW for all the operation. This device automatically turns off the output driver during WRITE cycle.
14. Device outputs are ensured to be in High-Z during device power-up.
15. This device contains a 2-bit burst counter. The address counter is incremented for all Continue Burst cycles. Address wraps to the initial address every fourth burst cycle.
16. Continue Burst cycles, whether Read or Write, use the same control signals. The type of cycle performed, Read or Write, depends upon the R/$\overline{W}$ control signal at the Begin Burst cycle. A Continue Deselect cycle can only be entered if a Deselect cycle is executed first.
17. Dummy Read and Abort Write cycles can be entered to set up subsequent Read or Write cycles or to increment the burst counter.
18. When an Ignore Clock Edge cycle enters, the output data (Q) will remain the same if the previous cycle is Read cycle or remain High-Z if the previous cycle is Write or Deselect cycle.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Voltage on V_{CC} Supply Relative to V_{SS} ..... –0.5V to +4.6V

V_{IN} .....–0.5V to V_{CC}+0.5V

Storage Temperature (plastic) ..... –55°C to +125°C

Junction Temperature ..... +125°C

Power Dissipation 2.0W

Short Circuit Output Current ..... 50 mA

Operating Range

Range	Ambient Temperature[19]	V_{CC}/V_{CCQ}
Com'l	0°C to +70°C	3.3V ± 5%

Electrical Characteristics Over the Operating Range [20]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IHD}	Input High (Logic 1) Voltage[21, 22]	Data Inputs (DQxx)	2.0	V_{CC}+0.3	V
V_{IH}		All Other Inputs	2.0	4.6	V
V_{II}	Input Low (Logic 0) Voltage[21, 22]		–0.5	0.8	V
IL_I	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	-	5	µA
IL_I	MODE and ZZ Input Leakage Current[21]	$0V \le V_{IN} \le V_{CC}$	-	30	µA
IL_O	Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	-	5	µA
V_{OH}	Output High Voltage[21]	I_{OH} = –5.0 mA for 3.3V I/O	2.4		V
		I_{OH} = –1.0 mA for 2.5V I/O	2.0		V
V_{OL}	Output Low Voltage[21]	I_{OL} = 8.0 mA		0.4	V
V_{CC}	Supply Voltage[21]		3.135	3.465	V
V_{CCQ}	I/O Supply Voltage[21]	3.3V I/O	3.135	3.465	V
		2.5V I/O	2.4	2.9	V

Parameter	Description	Conditions	Typ.	143 MHz/ -4	133 MHz/ -5	117 MHz/ -6	100 MHz/ -7	Unit
I_{CC}	Power Supply Current: Operating[24, 25, 26, 27]	Device selected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; cycle time $\ge t_{KC}$ min.; V_{CC} =Max.; outputs open, ADV/LD = X, f = $f_{MAX}/2$	150	400	380	350	300	mA
I_{SB2}	CMOS Standby[25, 26, 27]	Device deselected; V_{CC} = Max.; all inputs $\le V_{SS}$ + 0.2 or $\ge V_{CC}$ – 0.2; all inputs static; CLK frequency = 0	5	10	10	10	10	mA
I_{SB3}	TTL Standby[25, 26, 27]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; all inputs static; V_{CC} = Max.; CLK frequency = 0	20	40	40	40	40	mA
I_{SB4}	Clock Running[25, 26, 27]	Device deselected; all inputs $\le V_{IL}$ or $\ge V_{IH}$; V_{CC} = MAX; CLK cycle time $\ge t_{KC}$ Min.	50	95	85	80	70	mA

Notes:

19. T_A is the case temperature.
20. Values in table are associated with the operating frequencies listed.
21. All voltages referenced to V_{SS} (GND).
22. Overshoot: $V_{IH} \le +6.0V$ for $t \le t_{KC}/2$
    Undershoot:$V_{IL} \le -2.0V$ for $t \le t_{KC}/2$.
23. MODE pin has an internal pull-up and ZZ pin has an internal pull-down. These two pins exhibit an input leakage current of ±50 µA.
24. I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
25. "Device Deselected" means the device is in Power-Down mode as defined in the truth table. "Device Selected" means the device is active.
26. Typical values are measured at 3.3V, 25°C, and 20 ns cycle time.
27. At $f = f_{MAX}$, inputs are cycling at the maximum frequency of read cycles of $1/t_{CYC}$; f = 0 means no input lines are changing.

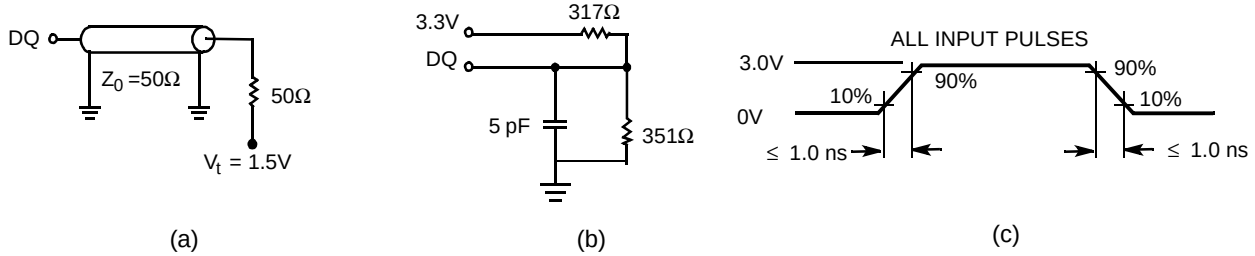
Capacitance[28]

Parameter	Description	Test Conditions	Typ.	Max.	Unit
C_I	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	4	4	pF
C_O	Input/Output Capacitance (DQ)		7	6.5	pF

Thermal Resistance

Description	Test Conditions	Symbol	TQFP Typ.	Units
Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer PCB	Θ_{JA}	25	°C/W
Thermal Resistance (Junction to Case)		Θ_{JC}	9	°C/W

AC Test Loads and Waveforms



(a) (b) (c)

Note:
28. This parameter is sampled.

Switching Characteristics Over the Operating Range[29]

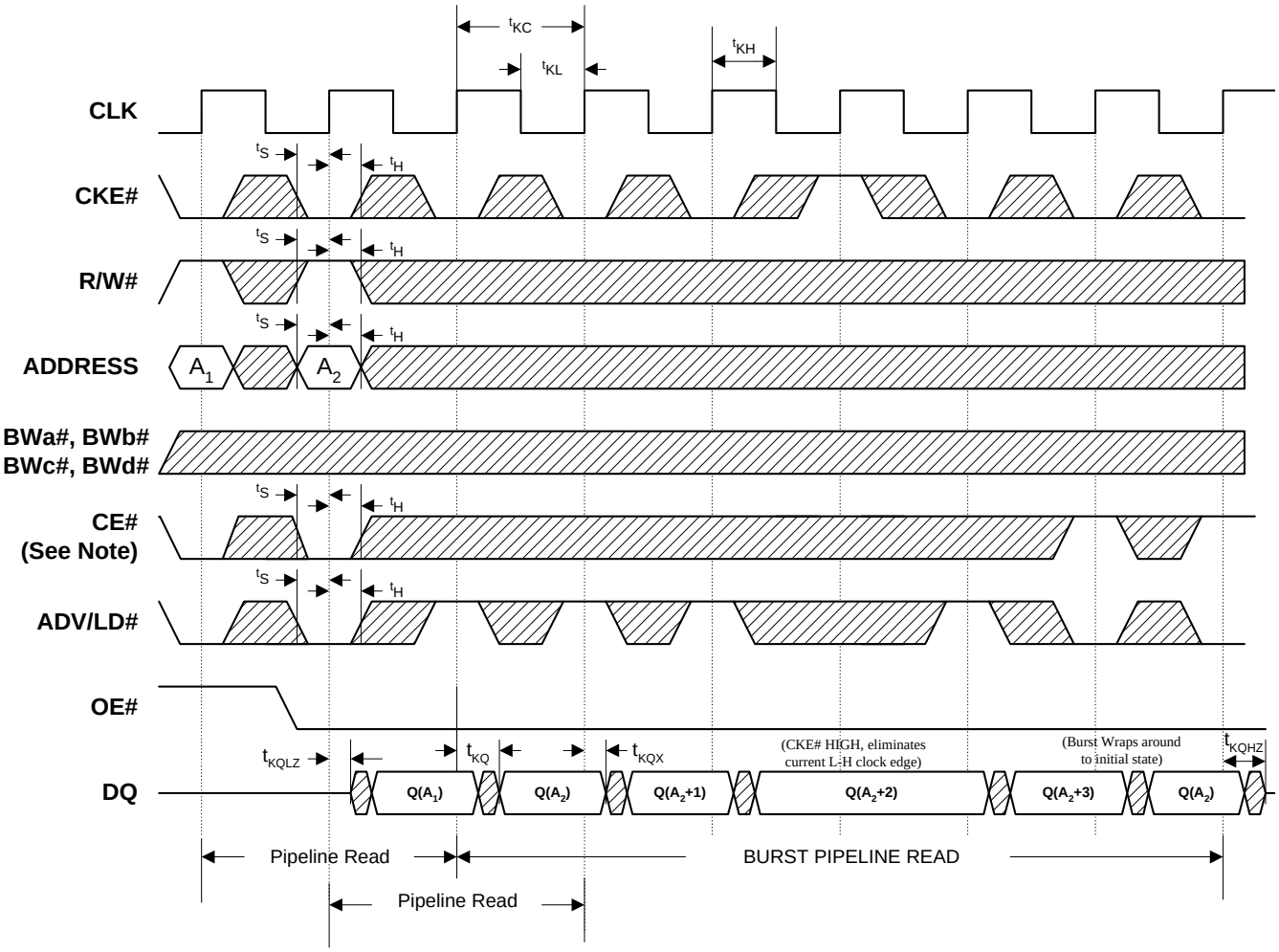
Parameter	Description	-4/ 143 MHz		-5/ 133 MHz		-6/ 117 MHz		-7/ 100 MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock										
t_{KC}	Clock Cycle Time	7.0		7.5		8.5		10		ns
t_{KH}	Clock HIGH Time	2.0		2.2		3.4		3.5		ns
t_{KL}	Clock LOW Time	2.0		2.2		3.4		3.5		ns
Output Times										
t_{KQ}	Clock to Output Valid		4.0		4.2		4.5		5.0	ns
t_{KQX}	Clock to Output Invalid	1.5		1.5		1.5		1.5		ns
t_{KQLZ}	Clock to Output in Low-Z[28, 30, 31]	1.5		1.5		1.5		1.5		ns
t_{KQHZ}	Clock to Output in High-Z[28, 30, 31]	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	ns
t_{OEQ}	OE to Output Valid		4.0		4.2		4.5		5.0	ns
t_{OELZ}	OE to Output in Low-Z[28, 30, 31]	0		0		0		0		ns
t_{OEHZ}	OE to Output in High-Z[28, 30, 31]		4		5		6		6	ns
Set-up Times										
t_S	Address and Controls[32]	2.0		2.0		2.0		2.2		ns
t_{SD}	Data In[32]	1.7		1.7		1.7		2.0		ns
Hold Times										
t_H	Address and Controls[32]	0.5		0.5		0.5		0.5		ns
t_{HD}	Data In[32]	0.5		0.5		0.5		0.5		ns

Notes:

29. Test conditions as specified with the output loading as shown in part (a) of AC Test Loads unless otherwise noted. Values in table are associated with the operating frequencies listed.
30. Output loading is specified with C_L=5 pF as in part (a) of AC Test Loads.
31. At any given temperature and voltage condition, t_{KQHZ} is less than t_{KQLZ} and t_{OEHZ} is less than t_{OELZ}.
32. This is a synchronous device. All synchronous inputs must meet specified set-up and hold time, except for “don’t care” as defined in the truth table.

Switching Waveforms

Read Timing[33, 34, 35, 36]

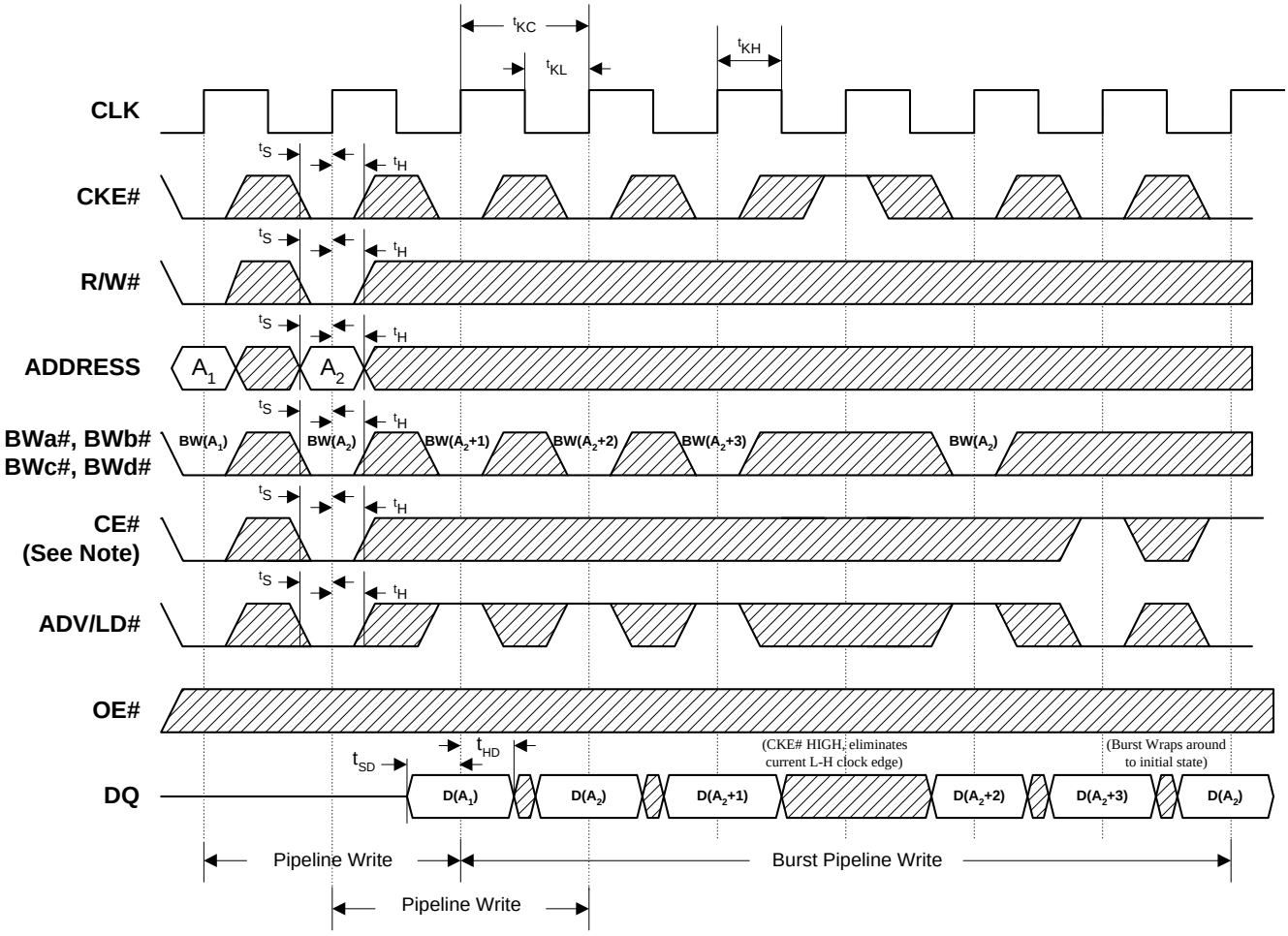


Notes:

33. $Q(A_1)$ represents the first output from the external address A_1. $Q(A_2)$ represents the first output from the external address A_2; $Q(A_2+1)$ represents the next output data in the burst sequence of the base address A_2, etc. where address bits SA0 and SA1 are advancing for the four word burst in the sequence defined by the state of the MODE input.
34. $\overline{CE}_2$ timing transitions are identical to the $\overline{CE}$ signal. For example, when $\overline{CE}$ is LOW on this waveform, $\overline{CE}_2$ is LOW. CE_2 timing transitions are identical but inverted to the $\overline{CE}$ signal. For example, when $\overline{CE}$ is LOW on this waveform, CE_2 is HIGH.
35. Burst ends when new address and control are loaded into the SRAM by sampling ADV/$\overline{LD}$ LOW.
36. R/$\overline{W}$ is “Don’t Care” when the SRAM is bursting (ADV/$\overline{LD}$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/$\overline{W}$ signal when new address and control are loaded into the SRAM.

Switching Waveforms (continued)

Write Timing[34, 35, 36, 37, 38]

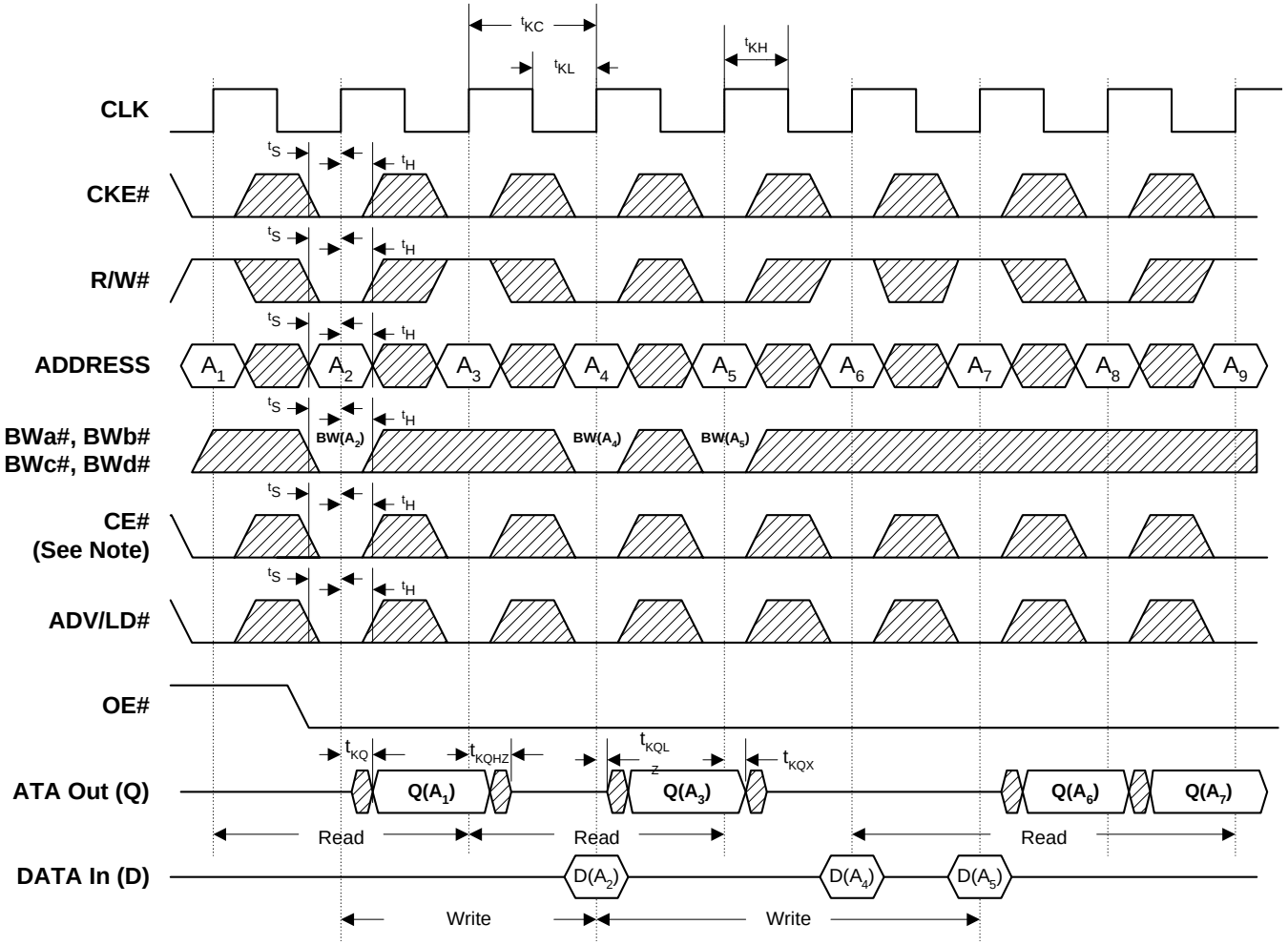


Notes:

37. $D(A_1)$ represents the first input to the external address A1. $D(A_2)$ represents the first input to the external address A_2; $D(A_2+1)$ represents the next input data in the burst sequence of the base address A_2, etc. where address bits SA0 and SA1 are advancing for the four word burst in the sequence defined by the state of the MODE input.
38. Individual Byte Write signals ($\overline{BWx}$) must be valid on all write and burst-write cycles. A write cycle is initiated when R/$\overline{W}$ signal is sampled LOW when ADV/$\overline{LD}$ is sampled LOW. The byte write information comes in one cycle before the actual data is presented to the SRAM.

Switching Waveforms (continued)

Read/Write Timing[34, 38, 39]

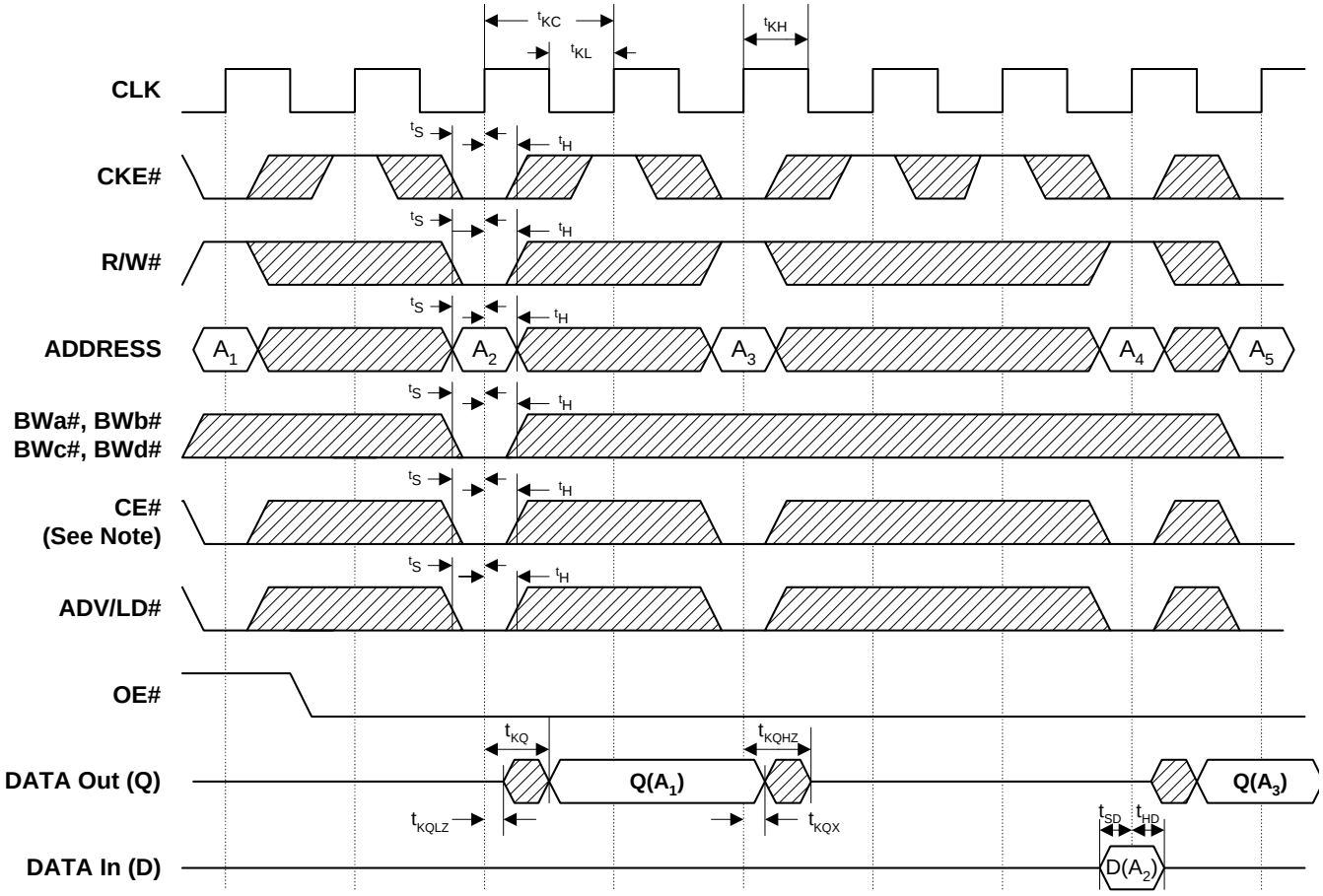


Note:

39. $Q(A_1)$ represents the first output from the external address A_1. $D(A_2)$ represents the input data to the SRAM corresponding to address A_2.

Switching Waveforms (continued)

$\overline{\text{CKE}}$ Timing[34, 38, 39, 40]

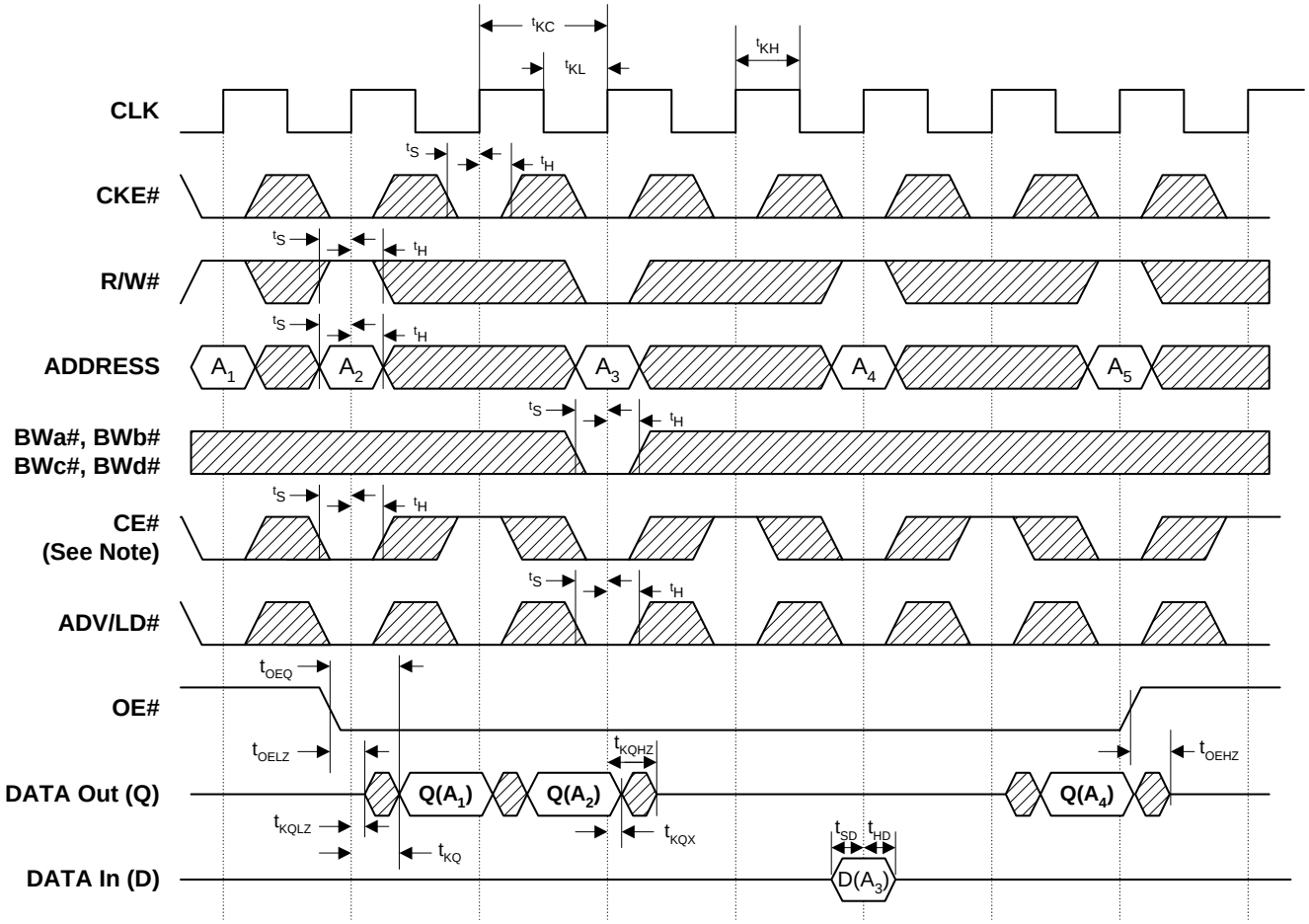


Note:

40. $\overline{\text{CKE}}$ when sampled HIGH on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal register in the SRAM will retain their previous state.

Switching Waveforms (continued)

$\overline{CE}$ Timing[34, 38, 41, 42]



Notes:

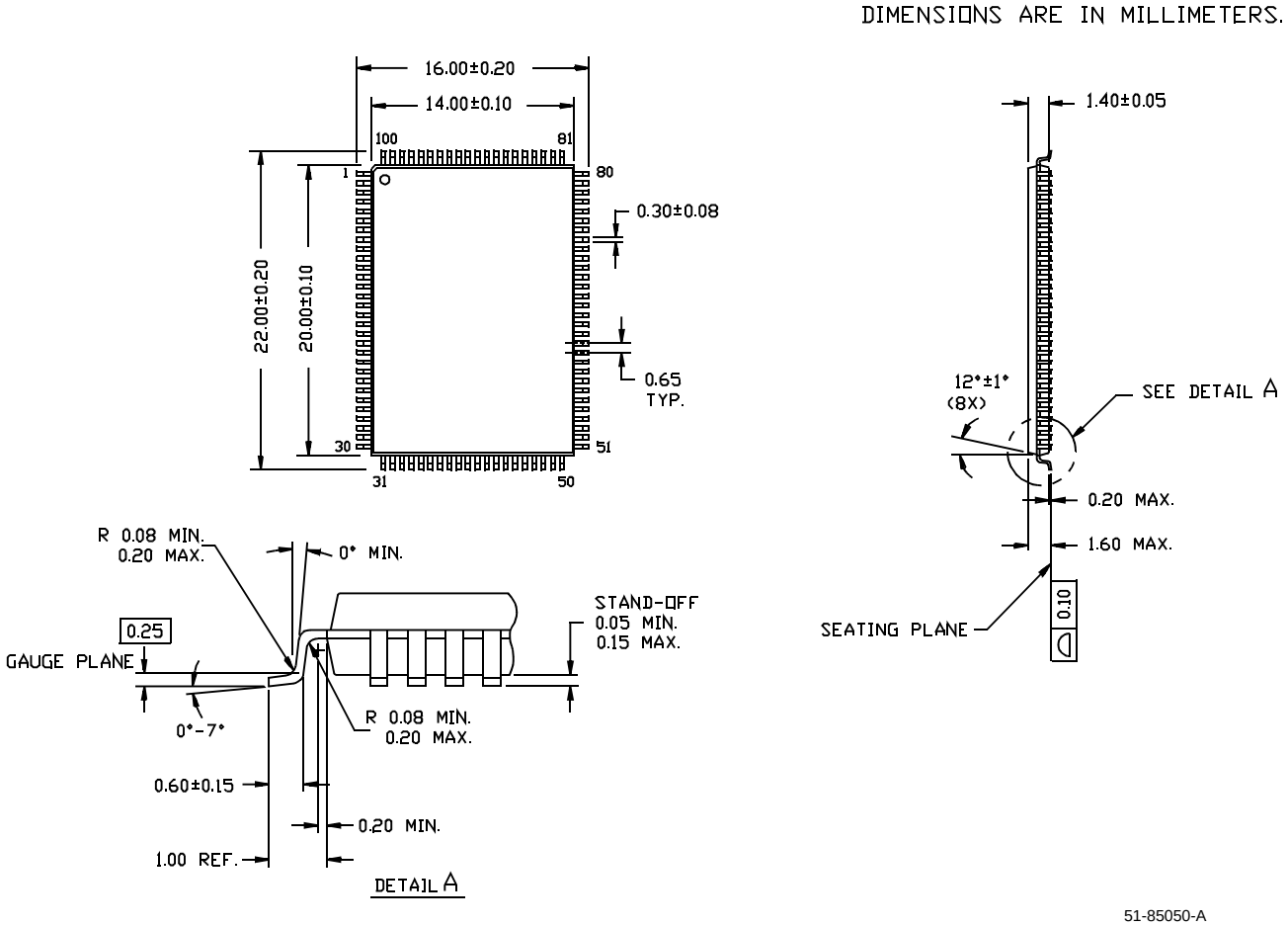
41. $Q(A_1)$ represents the first output from the external address A_1. $D(A_3)$ represents the input data to the SRAM corresponding to address A_3, etc.
42. When either one of the Chip Enables ($\overline{CE}$, CE_2, or $\overline{CE}_2$) is sampled inactive at the rising clock edge, a chip deselect cycle is initiated. The data-bus High-Z one cycle after the initiation of the deselect cycle. This allows for any pending data transfers (reads or writes) to be completed.

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
143	CY7C1350A-143AC/ GVT71128ZC36T-4	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	Commercial
133	CY7C1350A-133AC/ GVT71128ZC36T-5	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
133	CY7C1350A-133AC/ GVT71128ZC36T-6	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	
100	CY7C1350A-100AC/ GVT71128ZC36T-7	A101	100-Lead 14 x 20 x 1.4 mm Thin Quad Flat Pack	

Package Diagram

100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



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REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	108315	09/25/01	BRI	New Cypress data sheet—converted from Galvantech format