

## 32K x 9 Static RAM

### Features

- **High speed**  
— 15 ns
- **Automatic power-down when deselected**
- **Low active power**  
— 660 mW
- **Low standby power**  
— 140 mW
- **CMOS for optimum speed/power**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  features**

### Functional Description

The CY7C188 is a high-performance CMOS static RAM organized as 32,768 words by 9 bits. Easy memory expansion is

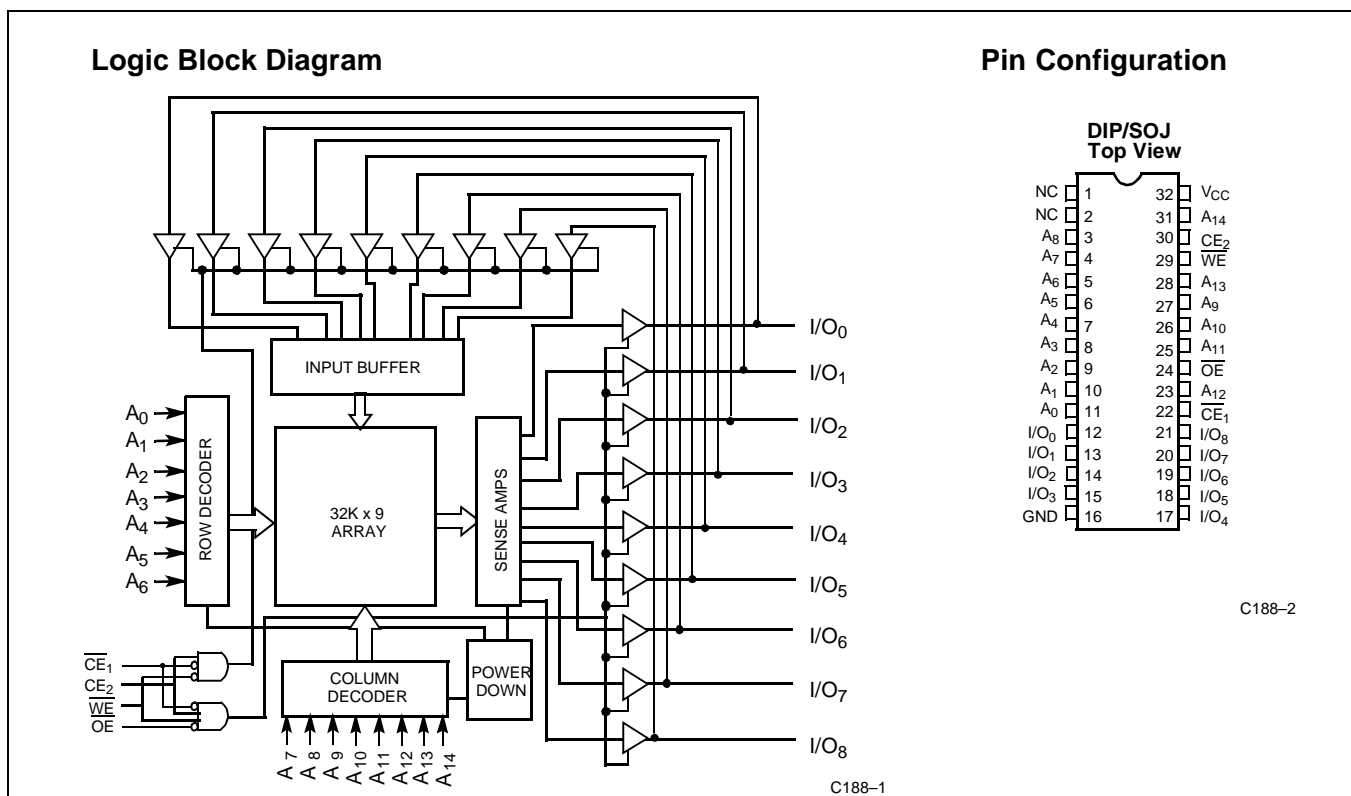
provided by an active-LOW chip enable ( $\overline{CE}_1$ ), an active-HIGH chip enable ( $CE_2$ ), an active-LOW output enable ( $\overline{OE}$ ), and three-state drivers. The device has an automatic power-down feature that reduces power consumption by more than 75% when deselected.

Writing to the device is accomplished by taking  $\overline{CE}_1$  and write enable ( $\overline{WE}$ ) inputs LOW and  $CE_2$  input HIGH. Data on the nine I/O pins ( $I/O_0 - I/O_8$ ) is then written into the location specified on the address pins ( $A_0 - A_{14}$ ).

Reading from the device is accomplished by taking  $\overline{CE}_1$  and  $\overline{OE}$  LOW while forcing  $\overline{WE}$  and  $CE_2$  HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The nine input/output pins ( $I/O_0 - I/O_8$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).

The CY7C188 is available in standard 300-mil-wide SOJs.



C188-2

C188-1

### Selection Guide

	7C188-15	7C188-20	7C188-25	7C188-35
Maximum Access Time (ns)	15	20	25	35
Maximum Operating Current (mA)   Commercial	120	170	165	160
Maximum Standby Current (mA)	35	35	35	30

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied..... -55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> Relative to GND (Pin 32 to Pin 16) ..... -0.5V to + 7.0V  
 DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V

DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V  
 Output Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current..... >200 mA

### Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%

### Electrical Characteristics Over the Operating Range<sup>[2]</sup>

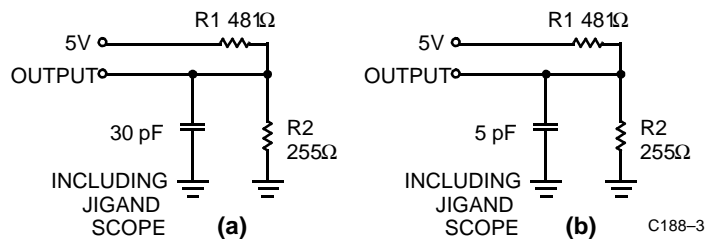
Parameter	Description	Test Conditions	7C188-15		7C188-20		7C188-25		7C188-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	-5	+5	-5	+5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		120		170		165		160	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current—TTL Inputs	Max. V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>IH</sub> or CE <sub>2</sub> ≤ V <sub>IL</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		35		35		35		30	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current—CMOS Inputs	Max. V <sub>CC</sub> , CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.3V or CE <sub>2</sub> ≤ 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0		10		15		15		15	mA

### Capacitance<sup>[4]</sup>

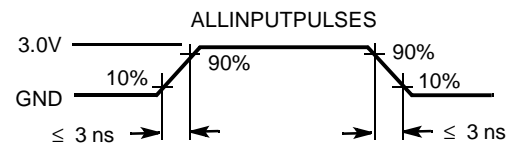
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub> : Addresses	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	6	pF
C <sub>IN</sub> : Controls	Input Capacitance		8	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Notes:**

1. Minimum voltage is equal to -2.0V for pulse durations less than 20 ns.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

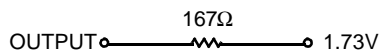
**AC Test Loads and Waveforms<sup>[5, 6]</sup>**


C188-3



C188-4

Equivalent to: THEVENIN EQUIVALENT


**Switching Characteristics Over the Operating Range<sup>[2, 5]</sup>**

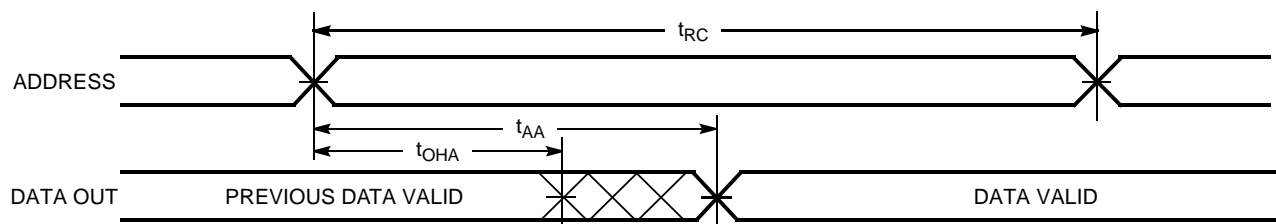
Parameter	Description	7C188-15		7C188-20		7C188-25		7C188-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>										
$t_{RC}$	Read Cycle Time	15		20		25		35		ns
$t_{AA}$	Address to Data Valid		15		20		25		35	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		3		ns
$t_{ACE}$	$\overline{CE}_1$ LOW or $CE_2$ HIGH to Data Valid		15		20		25		35	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		7		9		10		16	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low $Z^{[7]}$	0		0		3		3		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High $Z^{[6,7]}$		7		9		11		15	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW or $CE_2$ HIGH to Low $Z^{[7]}$	3		3		3		3		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to High $Z^{[6,7]}$		7		9		11		15	ns
$t_{PU}$	$\overline{CE}_1$ LOW or $CE_2$ HIGH to Power-Up	0		0		0		0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH or $CE_2$ LOW to Power-Down		15		20		20		20	ns
<b>WRITE CYCLE<sup>[8, 9]</sup></b>										
$t_{WC}$	Write Cycle Time	15		20		25		35		ns
$t_{SCE}$	$\overline{CE}_1$ LOW or $CE_2$ HIGH to Write End	10		15		18		22		ns
$t_{AW}$	Address Set-Up to Write End	10		15		20		30		ns
$t_{HA}$	Address Hold from Write End	0		0		0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	10		15		18		22		ns
$t_{SD}$	Data Set-Up to Write End	8		10		10		15		ns
$t_{HD}$	Data Hold from Write End	0		0		0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High $Z^{[6]}$	0	7	0	7	0	11	0	15	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low $Z^{[6,7]}$	3		3		3		3		ns

**Switching Characteristics** Over the Operating Range<sup>[2, 5]</sup>

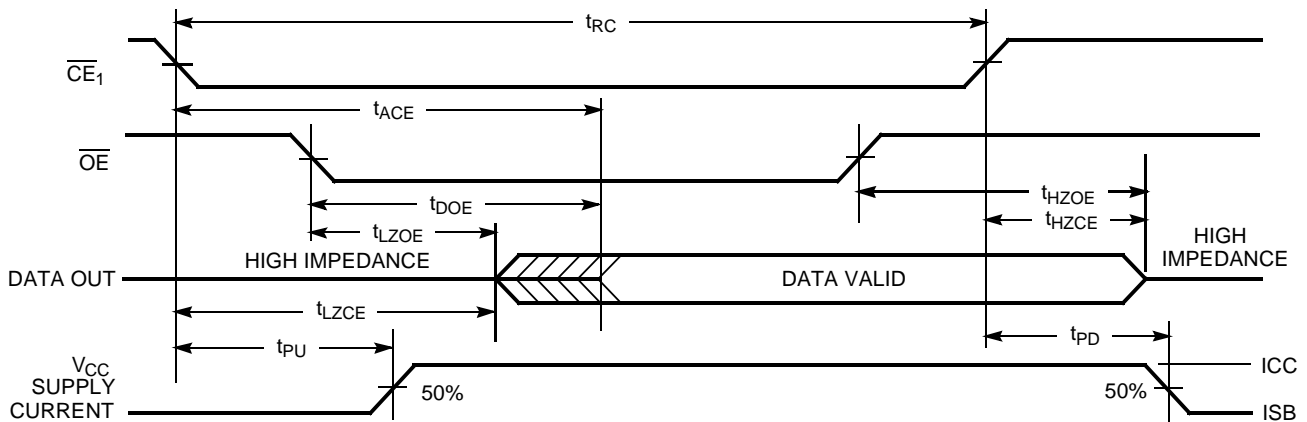
Parameter	Description	7C188-15		7C188-20		7C188-25		7C188-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	

**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}_1$ , LOW,  $CE_2$  HIGH, and WE LOW. All three signals must be asserted to initiate a write and any signal can terminate a write by being deasserted. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

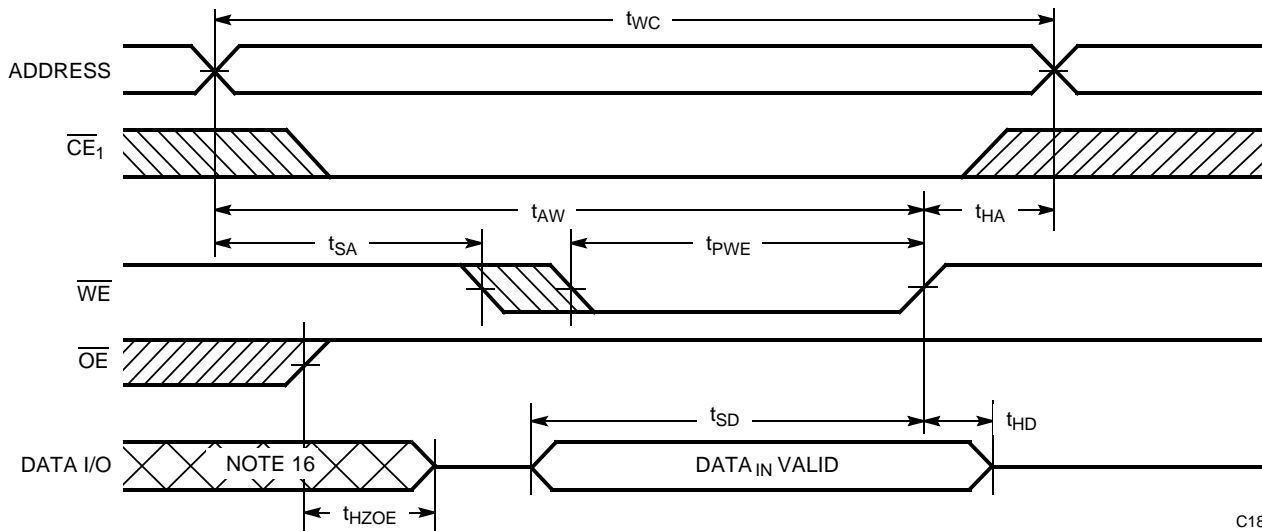
**Switching Waveforms**
**Read Cycle No. 1**<sup>[10,11]</sup>


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**Read Cycle No. 2 (Chip-Enable Controlled)**<sup>[11,12,13]</sup>


C188-6

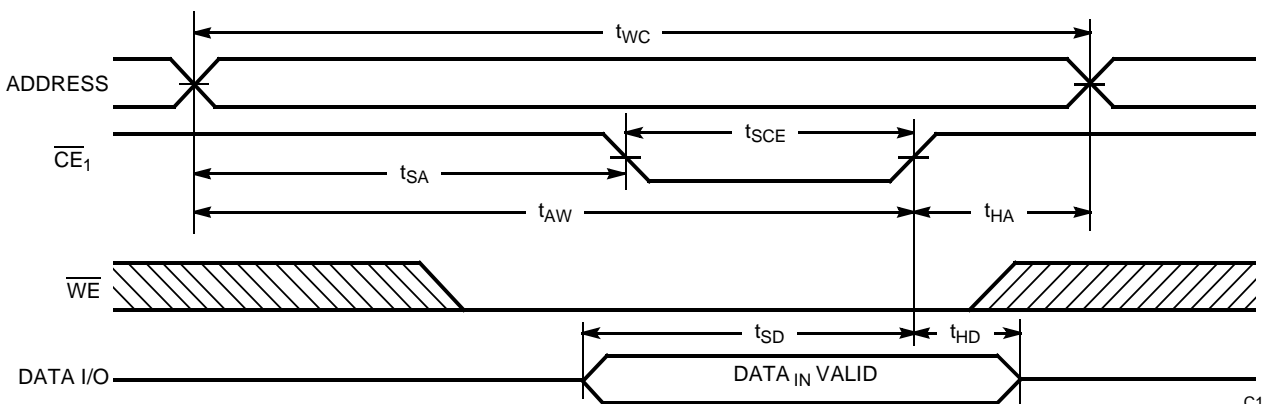
**Write Cycle No. 1 (WE Controlled)**<sup>[8,13,14,15]</sup>

**Switching Waveforms (Continued)**


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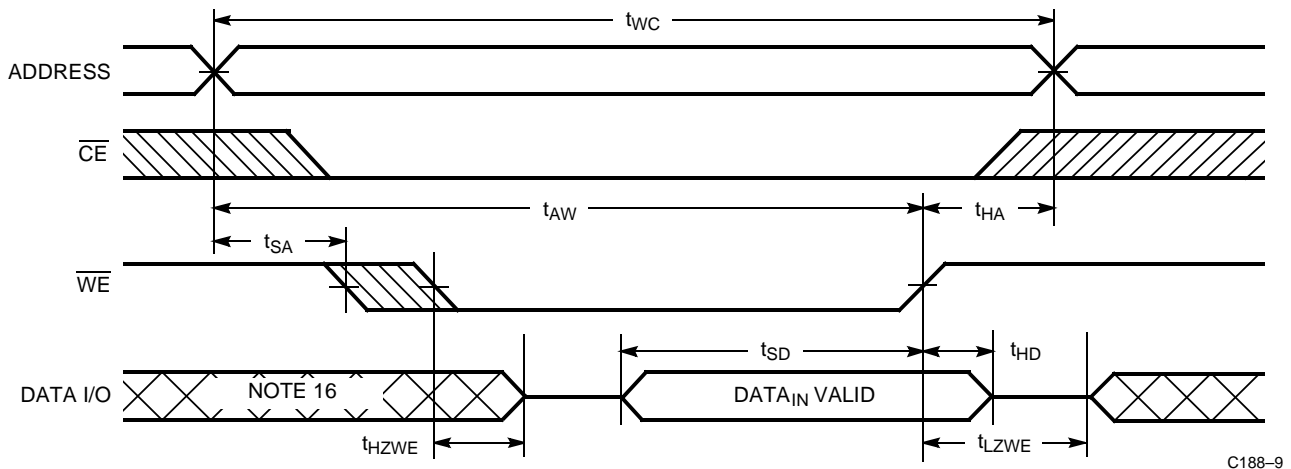
**Notes:**

10. Device is continuously selected.  $\overline{OE}, \overline{CE} = V_{IL}$ .
11.  $\overline{WE}$  is HIGH for read cycle.
12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
13. Timing parameters are the same for all chip enable signals ( $\overline{CE}_1$  and  $\overline{CE}_2$ ), so only the timing for  $\overline{CE}_1$  is shown.
14. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .
15. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.
16. During this period, the I/Os are in the output state and input signals should not be applied.

**Write Cycle No.2 ( $\overline{CE}$  Controlled)<sup>[8,13,14,15]</sup>**


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**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[9,13,15]</sup>**

**Switching Waveforms (Continued)**


C188-9

**Truth Table**

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Deselect, Output Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C188-15VC	V32	32-Lead (300-Mil) Molded SOJ	Commercial
20	CY7C188-20VC	V32	32-Lead (300-Mil) Molded SOJ	
25	CY7C188-25VC	V32	32-Lead (300-Mil) Molded SOJ	
35	CY7C188-35VC	V32	32-Lead (300-Mil) Molded SOJ	

**MILITARY SPECIFICATIONS  
Group A Subgroup Testing**
**DC Characteristics**

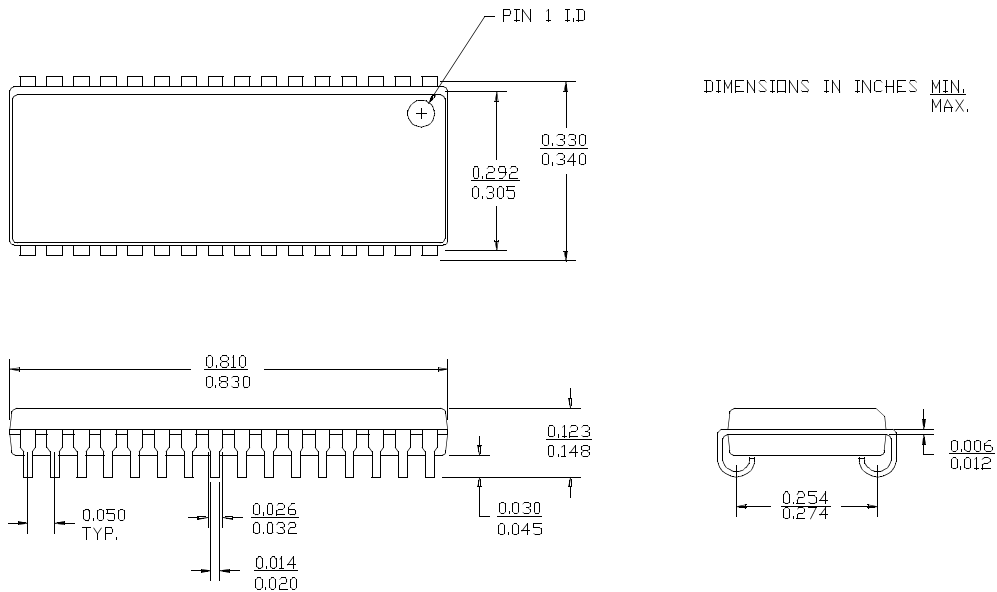
Parameter	Subgroups
$V_{OH}$	1, 2, 3
$V_{OL}$	1, 2, 3
$V_{IH}$	1, 2, 3
$V_{IL}$ Max.	1, 2, 3

**DC Characteristics**

Parameter	Subgroups
$I_{IX}$	1, 2, 3
$I_{OZ}$	1, 2, 3
$I_{CC}$	1, 2, 3
$I_{SB1}$	1, 2, 3
$I_{SB2}$	1, 2, 3

**Switching Characteristics**

Parameter	Subgroups
<b>READ CYCLE</b>	
$t_{RC}$	7, 8, 9, 10, 11
$t_{AA}$	7, 8, 9, 10, 11
$t_{OHA}$	7, 8, 9, 10, 11
$t_{ACE}$	7, 8, 9, 10, 11
$t_{DOE}$	7, 8, 9, 10, 11
<b>WRITE CYCLE</b>	
$t_{WC}$	7, 8, 9, 10, 11
$t_{SCE}$	7, 8, 9, 10, 11
$t_{AW}$	7, 8, 9, 10, 11
$t_{HA}$	7, 8, 9, 10, 11
$t_{SA}$	7, 8, 9, 10, 11
$t_{PWE}$	7, 8, 9, 10, 11
$t_{SD}$	7, 8, 9, 10, 11
$t_{HD}$	7, 8, 9, 10, 11

**Package Diagrams**
**32-Lead (300-Mil) Molded SOJ V32**


<b>Document Title: CY7C188 32K x 9 Static RAM</b> <b>Document Number: 38-05053</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	107155	09/10/01	SZV	Change from Spec number: 38-00220 to 38-05053