Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY62158G/CY62158GE MoBL

8-Mbit (1M × 8-bits) Static RAM with Error-Correcting Code (ECC)

Features

- Ultra-low standby power
  - Typical standby current: 1.4 µA
  - Maximum standby current: 6.5 µA
- High speed: 45 ns
- Embedded error-correcting code (ECC) for single-bit error correction[1, 2]
- Operating voltage range: 2.2 V to 3.6 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Available in Pb-free 48-ball VFBGA and 44-pin TSOP II package

Functional Description

CY62158G/CY62158GE is a high-performance CMOS low-power (MoBL) SRAM device with embedded ECC.

Device is accessed by asserting both chip enable inputs – $\overline{CE}_1$ as LOW and CE_2 as HIGH.

Write to the device is performed by taking Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 (CE_2) HIGH and the Write Enable ($\overline{WE}$) input LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{19}).

Read from the device is performed by taking Chip Enable 1 ($\overline{CE}_1$) and Output Enable ($\overline{OE}$) LOW and Chip Enable 2 (CE_2) HIGH while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

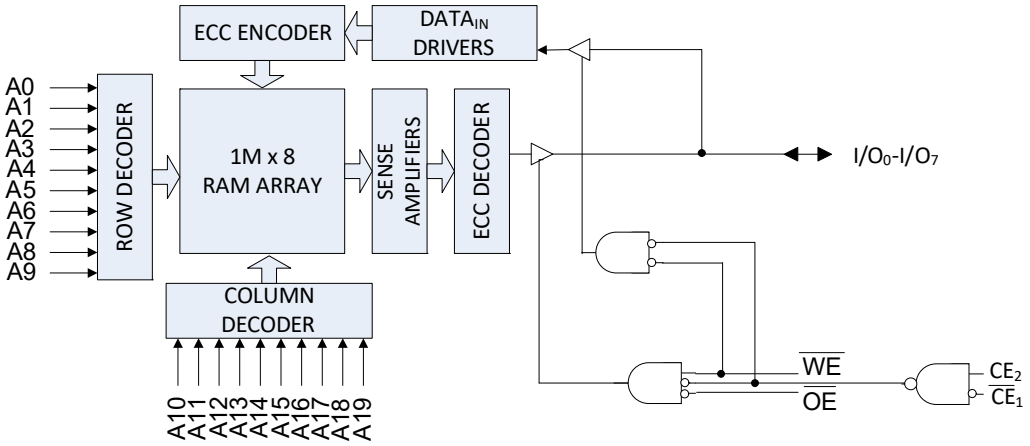
The eight input and output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or a write operation is in progress ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW). See the Truth Table – CY62158G/CY62158GE on page 13 for a complete description of read and write modes.

Product Portfolio

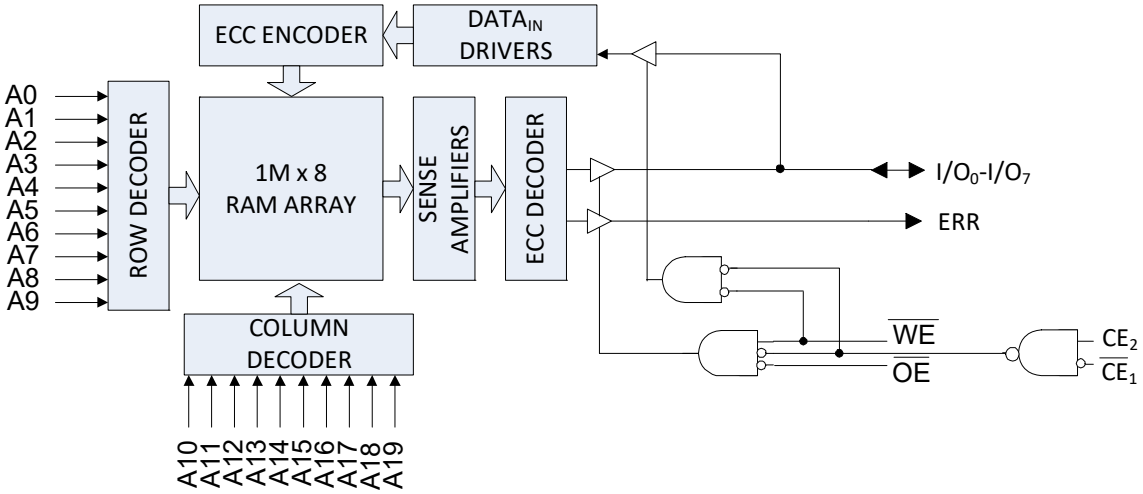
Product	Features and Options (see Pin Configurations – CY62158G)	Range	V_{CC} Range (V)	Speed (ns)	Power Dissipation			
					Operating I_{CC} (mA) f = f_{max}		Standby I_{SB2} (µA)	
					Typ[3]	Max	Typ[3]	Max
CY62158G/CY62158GE	Dual Chip Enable	Industrial	2.2 V–3.6 V	45	18	25	1.4	6.5

Notes
1. This device does not support automatic write-back on error detection.
2. SER FIT Rate <0.1 FIT/Mb. Refer AN88889 for details.
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3V (for V_{CC} range of 2.2V - 3.6V), T_A = 25 °C.

Logic Block Diagram – CY62158G



Logic Block Diagram – CY62158GE



Contents

Pin Configurations – CY62158G

Figure 1. 44-pin TSOP II Pinout[4]

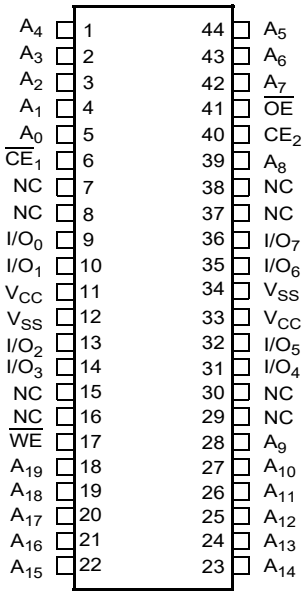
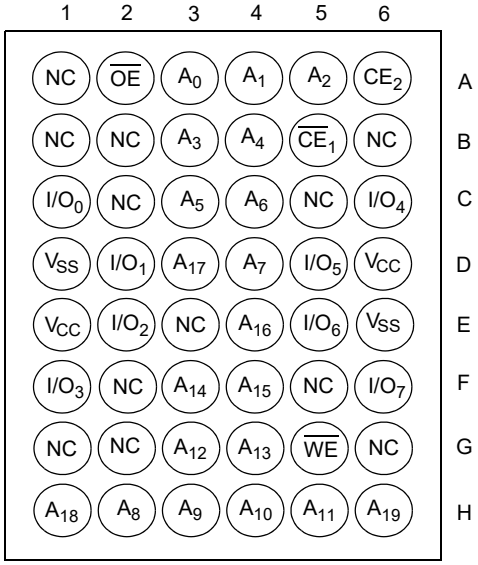


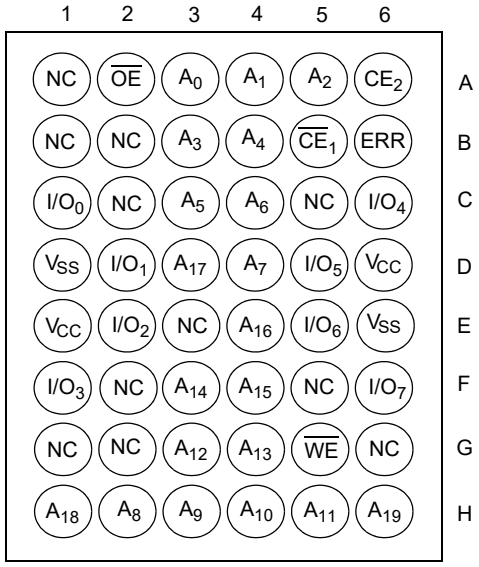
Figure 2. 48-ball VFBGA (6 × 8 × 1 mm) Pinout (without ERR) [4]



Note
4. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

Pin Configurations – CY62158GE

Figure 3. 48-ball VFBGA (6 × 8 × 1 mm) Pinout (with ERR) [5, 6]



Notes

5. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
6. ERR is an Output pin.If not used, this pin should be left floating.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential ..... –0.5 V to V_{CC} + 0.5 V

DC voltage applied to outputs in High Z state[7] ..... –0.5 V to V_{CC} + 0.5 V

DC input voltage[7] ..... –0.5 V to V_{CC} + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}[8]
Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range of –40 °C to 85 °C

Parameter	Description		Test Conditions		45 ns			Unit
					Min	Typ[9]	Max	
V_{OH}	Output HIGH voltage	4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.4	–	–	V
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –0.1 mA		V_{CC} – 0.4[10]	–	–	
V_{OL}	Output LOW voltage	4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	V
V_{IH}[7]	Input HIGH voltage	4.5 V to 5.5 V	–		2.2	–	V_{CC} + 0.5	V
V_{IL}[7]	Input LOW voltage	4.5 V to 5.5 V	–		–0.5	–	0.8	V
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–1.0	–	+1.0	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1.0	–	+1.0	µA
I_{CC}	V_{CC} operating supply current		V_{CC} = Max, I_{OUT} = 0 mA, CMOS levels	f = 22.22 MHz (45 ns)	–	18.0	25.0	mA
				f = 1 MHz	–	6.0	7.0	
I_{SB1}[11]	Automatic power down current – CMOS inputs; V_{CC} = 2.2 to 3.6 V		$\overline{CE_1}$ ≥ V_{CC} – 0.2 V or CE_2 ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), V_{CC} = $V_{CC(max)}$		–	1.4	6.5	µA
I_{SB2}[11]	Automatic power down current – CMOS inputs; V_{CC} = 2.2 to 3.6 V		$\overline{CE_1}$ ≥ V_{CC} – 0.2 V or CE_2 ≤ 0.2 V, or V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = $V_{CC(max)}$	25 °C[12]	–	1.4	2.8	µA
				40 °C[12]	–		3.5	
				70 °C[12]	–		5.5	
				85 °C	–		6.5	

Notes

7. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
8. Full Device AC operation assumes a 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at Vcc = 3V (for V_{CC} range of 2.2 V to 3.6 V), T_A = 25 °C.
10. This parameter is guaranteed by design and not tested.
11. Chip enables ($\overline{CE_1}$ and CE_2) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
12. The I_{SB2} limits at 25 °C, 40 °C, 70 °C and typical limit at 85 °C are guaranteed by design and not 100% tested.

Capacitance

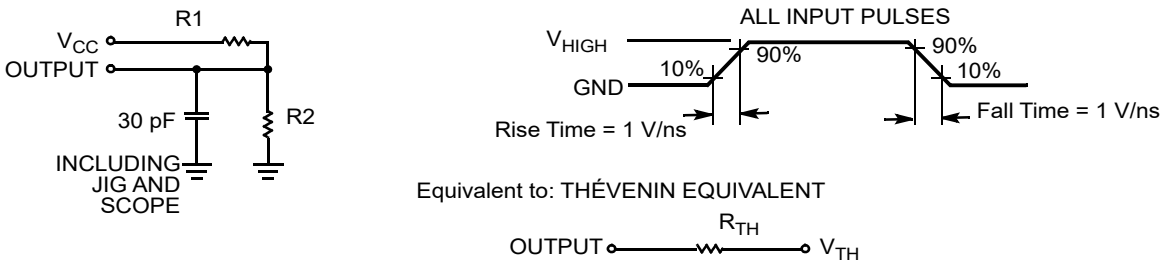
Parameter[13]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter[13]	Description	Test Conditions	48-ball VFBGA	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	36.92	66.93	°C/W
Θ_{JC}	Thermal resistance (junction to case)		13.55	13.09	°C/W

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms



Parameters	5.0 V	Unit
R1	1800	Ω
R2	990	Ω
R_{TH}	639	Ω
V_{TH}	1.77	V
V_{HIGH}	5.0	V

Note
13. Tested initially and after any design or process changes that may affect these parameters.

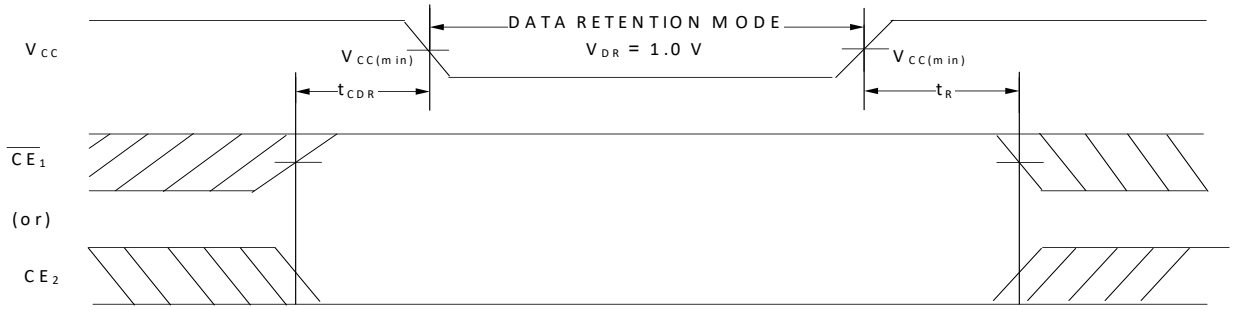
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ[14]	Max	Unit
V_{DR}	V_{CC} for data retention			1.0	–	–	V
I_{CCDR}[14, 15]	Data retention current	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Vcc = 1.2V		4	9	
			Vcc = 1.5V		3.2	8	
			2.2 V < $V_{CC} \leq$ 3.6 V	–	1.4	6.5	µA
t_{CDR}[16]	Chip deselect to data retention time	–		0	–	–	–
t_R[16, 17]	Operation recovery time	–		45	–	–	ns

Data Retention Waveform

Figure 5. Data Retention Waveform



Notes

14. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.
15. Chip enables ($\overline{CE}_1$ and CE_2) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating. I_{CCDR} is guaranteed only after device is first powered up to $V_{CC(min)}$ and brought down to V_{DR}.
16. These parameters are guaranteed by design.
17. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq$ 100 µs or stable at $V_{CC(min)} \geq$ 100 µs.

Switching Characteristics

Parameter[18]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45.0	–	ns
t_{AA}	Address to data valid	–	45.0	ns
t_{OHA}	Data hold from address change	10.0	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid / $\overline{CE}$ LOW to ERR valid	–	45.0	ns
t_{DOE}	$\overline{OE}$ LOW to data valid / $\overline{OE}$ LOW to ERR valid	–	22.0	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[19, 20, 21]	5.0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[19, 20, 21, 22]	–	18.0	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[19, 20, 21]	10.0	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[19, 20, 21, 22]	–	18.0	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up[21]	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power-down[21]	–	45.0	ns
Write Cycle[23, 24]				
t_{WC}	Write cycle time	45.0	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35.0	–	ns
t_{AW}	Address setup to write end	35.0	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35.0	–	ns
t_{SD}	Data setup to write end	25.0	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[19, 20, 21, 22]	–	18.0	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[19, 20, 21]	10.0	–	ns

Notes

18. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
19. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
20. Tested initially and after any design or process changes that may affect these parameters.
21. These parameters are guaranteed by design and are not tested.
22. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
23. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
24. The minimum write cycle pulse width for Write cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ Low) should be equal to he sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 6. Read Cycle No. 1 (Address Transition Controlled)[25, 26]

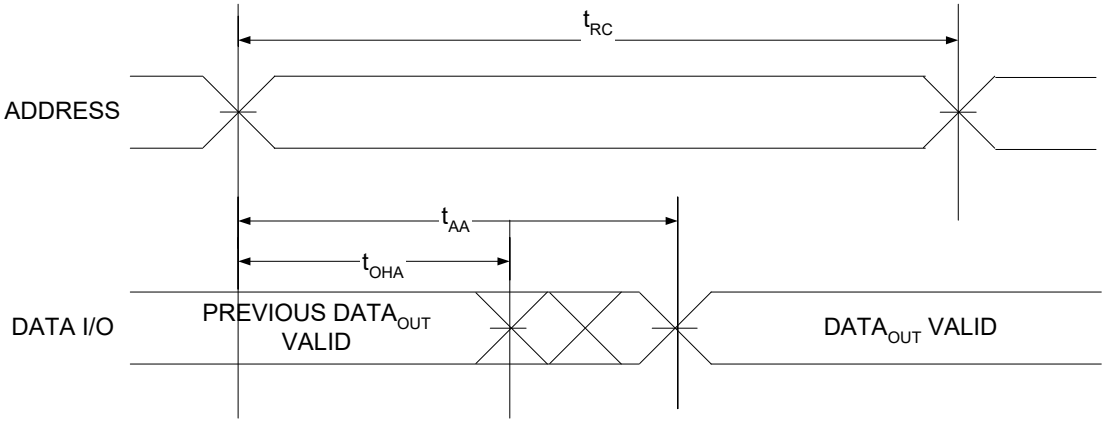
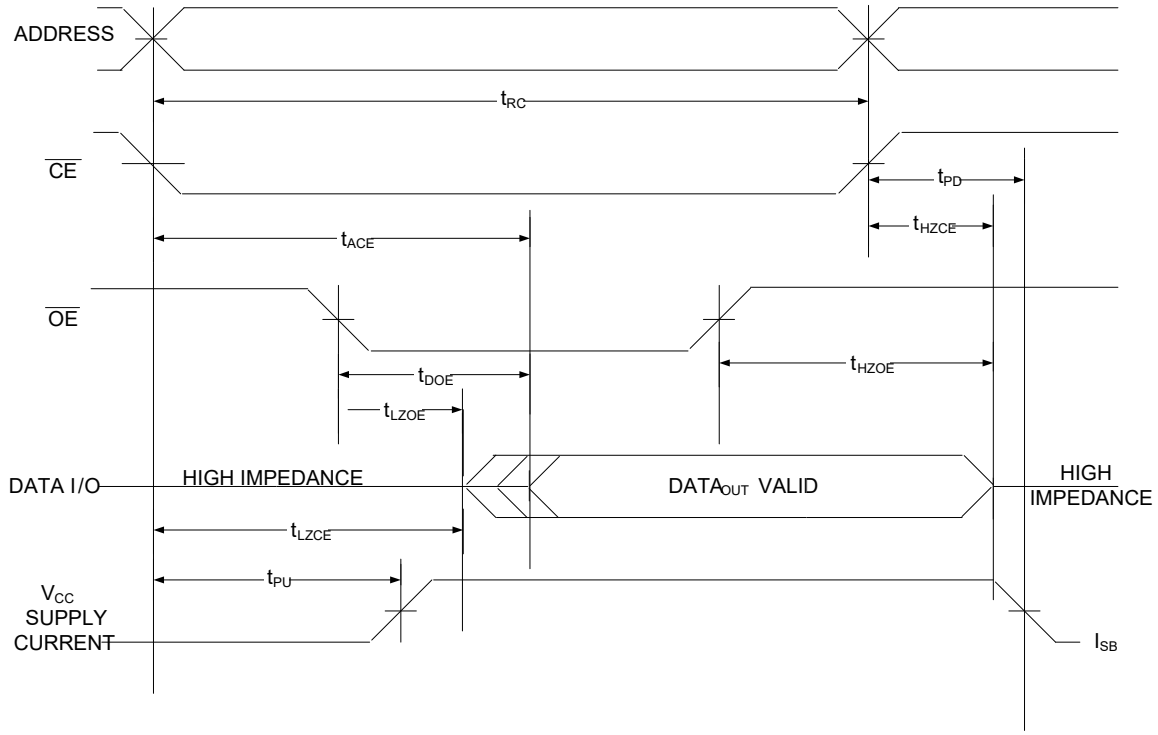


Figure 7. Read Cycle No. 2 ($\overline{OE}$ Controlled)[26, 27, 28]

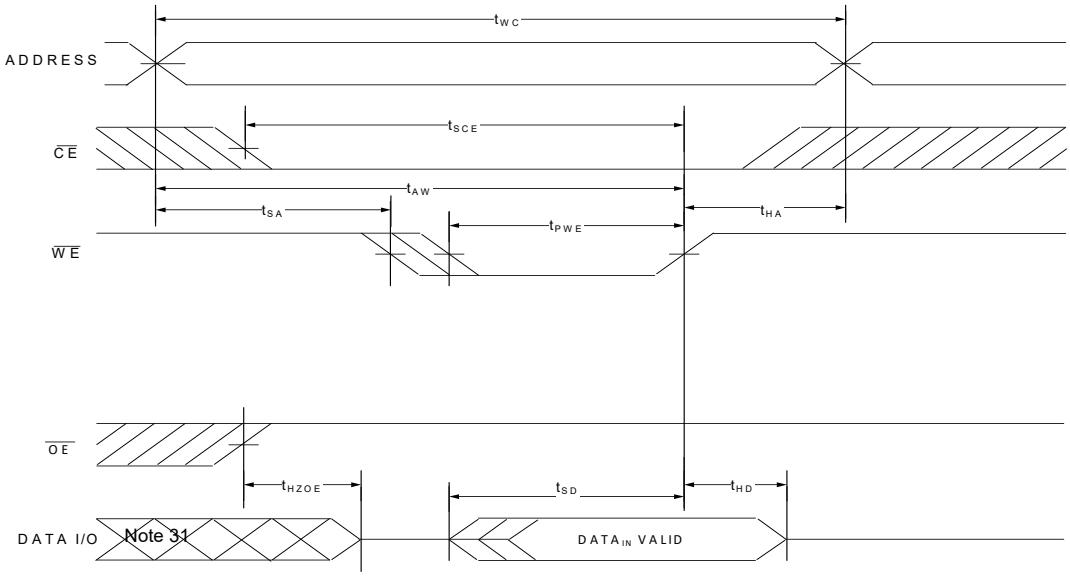


Notes

25. The device is continuously selected. $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IL}.
26. $\overline{WE}$ is HIGH for read cycle.
27. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
28. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ($\overline{WE}$ Controlled)[29, 30 31]



Notes

29. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
30. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}_1$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write. Data I/O is in the high-impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH}.
31. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ Low)[32, 33, 34, 35]

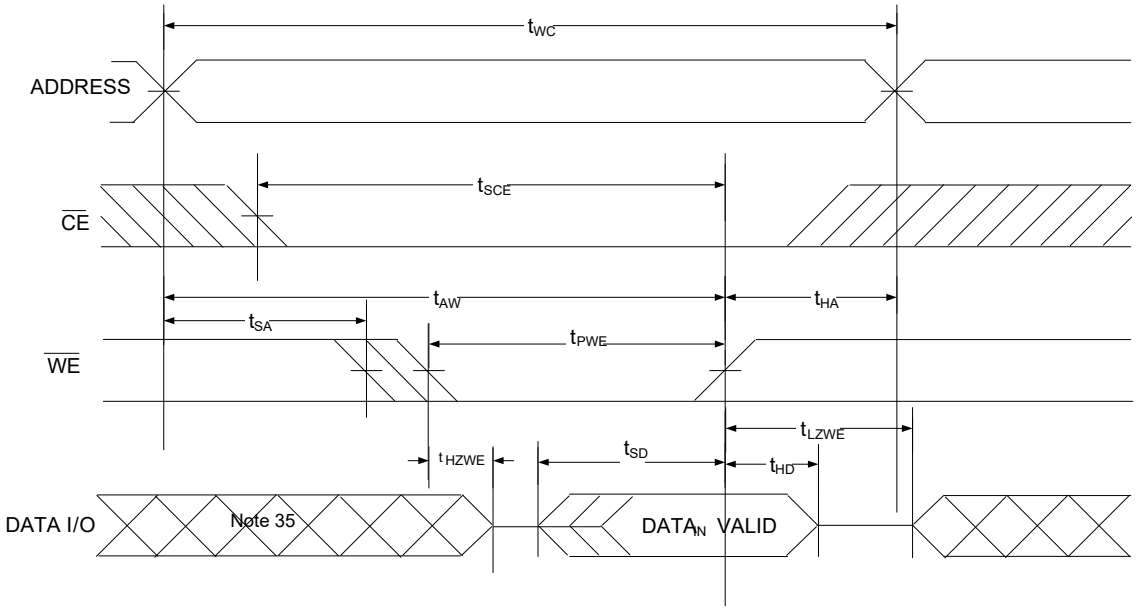
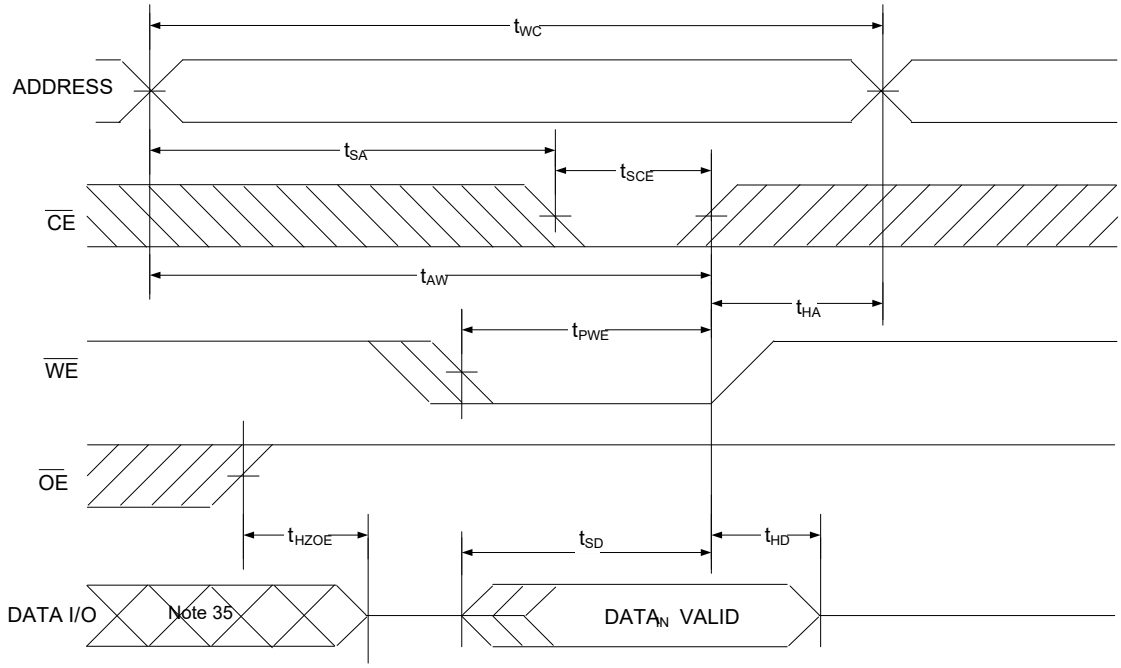


Figure 10. Write Cycle No. 3 ($\overline{CE}$ Controlled)[32, 33, 34]



Notes

32. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
33. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}_1$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write. Data I/O is in high impedance state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH}.
34. The minimum write cycle pulse width should be equal to the sum of the t_{HZWE} and t_{SD}.
35. During this period I/O are in the output state. Do not apply input signals.

Truth Table – CY62158G/CY62158GE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	I/Os	Mode	Power
H	X[36]	X[36]	X[36]	High Z	Deselect / Power down	Standby (I_{SB2})
X[36]	L	X[36]	X[36]	High Z	Deselect / Power down	Standby (I_{SB2})
L	H	H	L	Data Out (I/O_0–I/O_7)	Read	Active (I_{CC})
L	H	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	X	Data In (I/O_0–I/O_7)	Write	Active (I_{CC})

ERR Output – MoBL

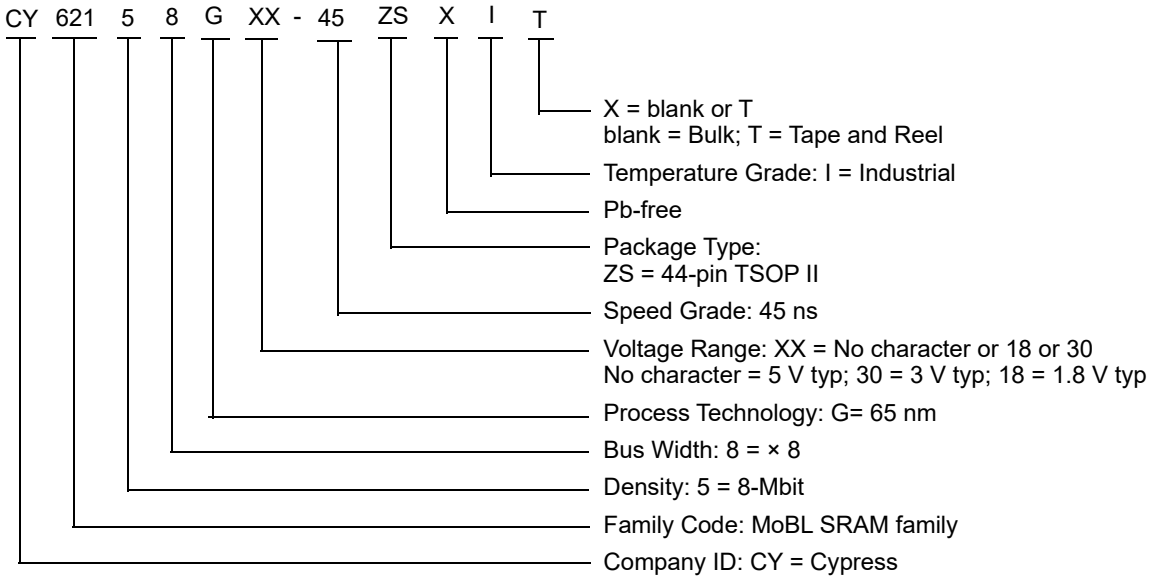
Output[37]	Mode
0	Read operation, no single-bit error in the stored data.
1	Read operation, single-bit error detected and corrected.
High-Z	Device deselected / outputs disabled / Write operation

Notes
36. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.
37. ERR is an Output pin. If not used, this pin should be left floating.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type (all Pb-free)	Operating Range
45	CY62158G30-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	Industrial
	CY62158G30-45ZSXIT			
	CY62158G30-45BVXI	51-85150	48-ball VFBGA	
	CY62158GE30-45BVXI			

Ordering Code Definitions



Package Diagrams

Figure 11. 44-pin TSOP Z44-II Package Outline, 51-85087

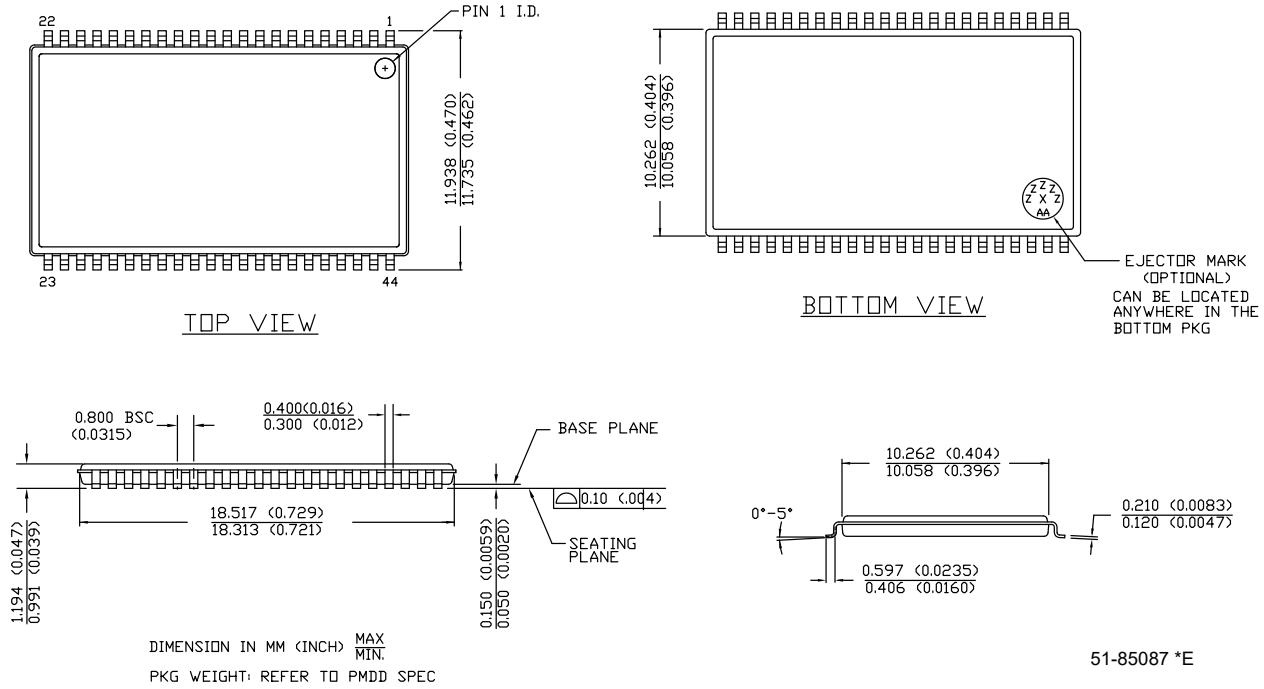
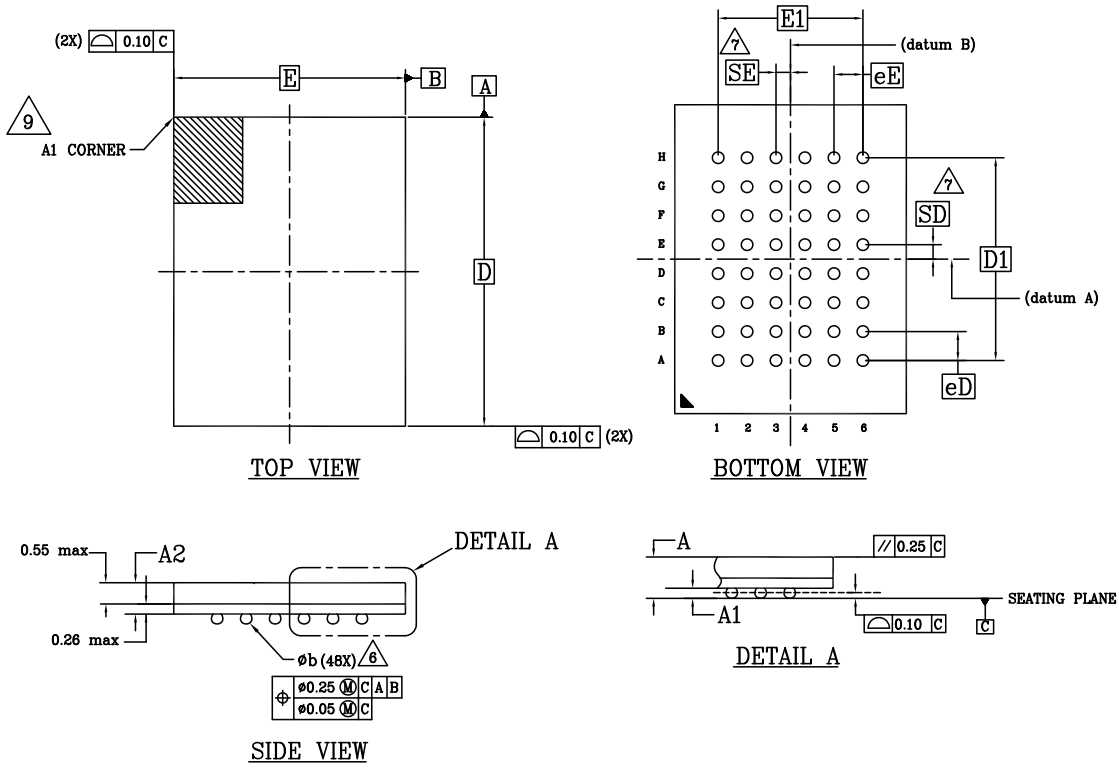


Figure 12. 48-Ball VFBGA 6 × 8 × 1.0 mm BV48/BZ48/VCF048 Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
A2	-	-	0.81
D	8.00 BSC		
E	6.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
MD	8		
ME	6		
n	48		
Ø b	0.25	0.30	0.35
eE	0.75 BSC		
eD	0.75 BSC		
SD	0.375 BSC		
SE	0.375 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *I

Acronyms

Table 1. Acronyms Used in this Document

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable
ECC	Error Correcting Code

Document Conventions

Units of Measure

Table 2. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt

Document History Page

Document Title: CY62158G/CY62158GE MoBL, 8-Mbit (1M × 8-bits) Static RAM with Error-Correcting Code (ECC) Document Number: 002-29691			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*A	6814364	02/28/2020	Release to Web.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

Cypress Developer Community

Community | Code Examples | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support