CY24488-001

Quad-PLL Clock Generator with Two-Wire Serial Interface

Features

- Three output frequencies and reference out
- Programmable output frequencies through two-wire serial interface
- Output frequencies from 27 MHz to 74.25 MHz
- Uses an external 27 MHz crystal
- Programmable output drive strength to minimize EMI
- 16-pin thin-shrink small outline package (TSSOP) package
- 3.3 V operation

Benefits

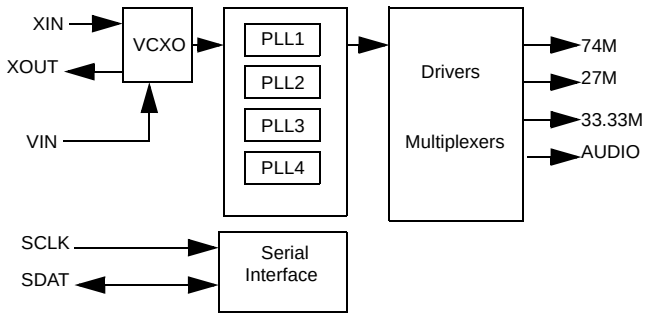
- Meets most digital set top box, DVD recorder, and DTV application requirements
- Multiple high performance phase-locked loops (PLLs) allow synthesis of unrelated frequencies
- Integration eliminates the need for external loop filter components

Functional Description

The CY24488-001 generates up to three independent clock frequencies and a buffered copy of the reference crystal frequency from a single crystal reference input. Four clock output pins are available to drive some frequencies on two or more output pins. Outputs are also individually enabled or disabled. When a CLK output is individually disabled, it drives low.

A serial programming interface (SPI) permits in-system configuration of the device by writing to internal registers. It is used to set the output frequencies. The SPI provides volatile programming. When powered down, the device reverts to its preSPI state. When the system is powered back up, the SPI registers are configured again. Specific configuration details are provided in the following sections of this data sheet.

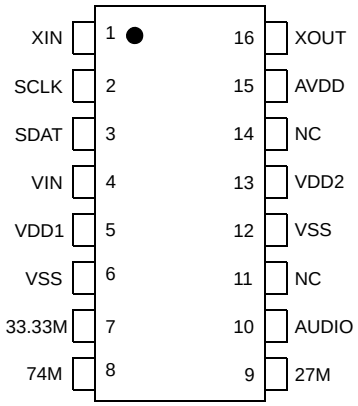
Logic Block Diagram



Contents

Pinouts

Figure 1. 16-pin TSSOP pinout



Pin Definitions

16-pin TSSOP

Pin Name	Pin Number	Pin Description
XIN	1	Crystal reference input
XOUT	16	Crystal output
33.33M	7	33.3333 MHz clock output
74M	8	74.175824/74.25 MHz clock output
27M	9	27 MHz clock output
AUDIO	10	36.864/33.8688/24.576 MHz clock output
NC	11	Unused output, leave floating
SCLK	2	Serial interface clock input
SDAT	3	Serial interface data
VIN	4	Unused input, connect to AVDD
NC	14	Unused input, connect to VSS
AVDD	15	Core and input voltage supply
VDD1	5	Voltage supply for 33.33M output
VDD2	13	Voltage supply for pin 8 - 11 outputs
VSS	6, 12	Ground

Default Startup Configuration

The default state of the device refers to its state at power on. All output clocks are running. For more information, refer Pin Definitions on page 3. Pin 8 outputs 74.17582418 MHz. Pin 10 outputs 36.864 MHz. The serial programming interface is used to configure the device for the desired output frequencies. Because the serial programming memory is volatile, the device reverts to its default configuration when power is cycled.

Serial Programming Interface Protocol and Timing

The CY24488-001 uses pins SDAT and SCLK for a two-wire serial interface that operates up to 400 kbit/s in read or write mode. Except for the data hold time (t_{DH}), it is compliant to the I^2C bus standard. The basic Write protocol follows:

Start Bit; 7-bit Device Address (DA); R/$\overline{W}$ Bit; Slave Clock Acknowledge (ACK); 8-bit Memory Address (MA); ACK; 8-bit Data; ACK; 8-bit Data in MA+1 if desired; ACK; 8-bit Data in MA+2; ACK; and so on, until STOP Bit. The basic serial format is shown in Figure 3.

Figure 2. Data Transfer Sequence on the Serial Bus

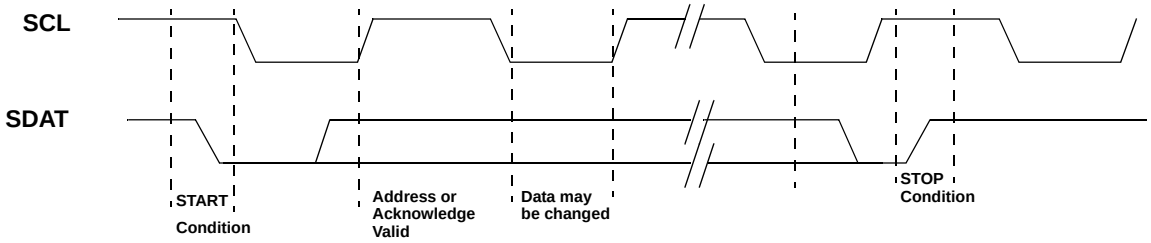
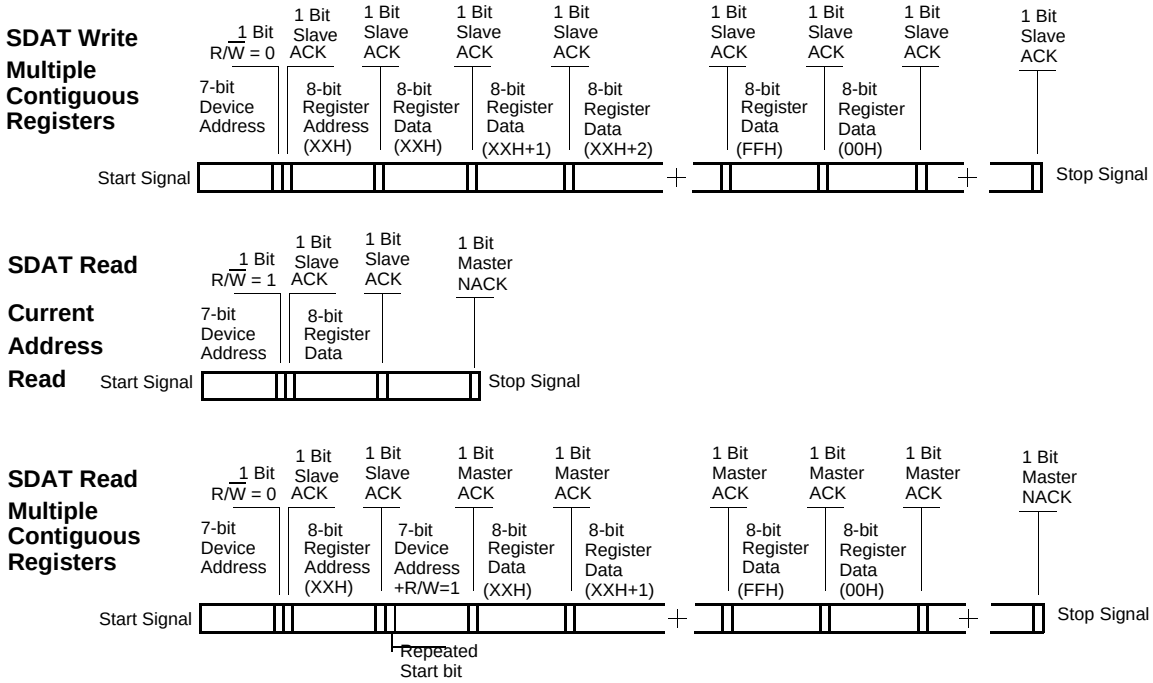


Figure 3. Data Frame Architecture



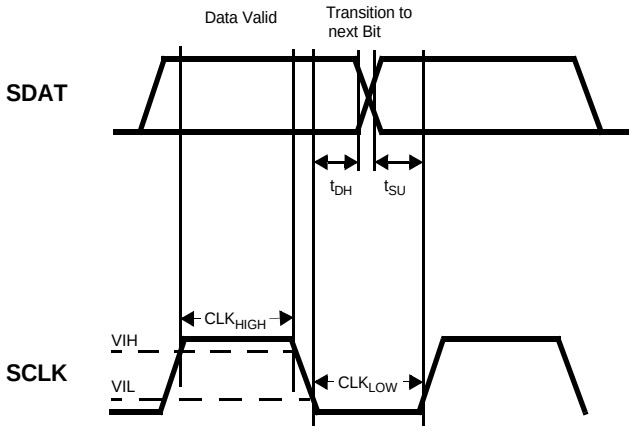
Device Address

The device address is a 7-bit value. The default serial interface address is 47H.

Data Valid

Data is valid when the clock is HIGH and is only transitioned when the clock is LOW, as shown in Figure 4.

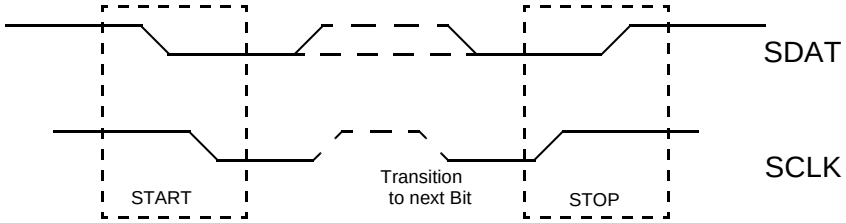
Figure 4. Data Valid and Data Transition Periods



Data Frame

Every new data frame is indicated by a start and stop sequence, as shown in Figure 5.

Figure 5. Start and Stop Frame



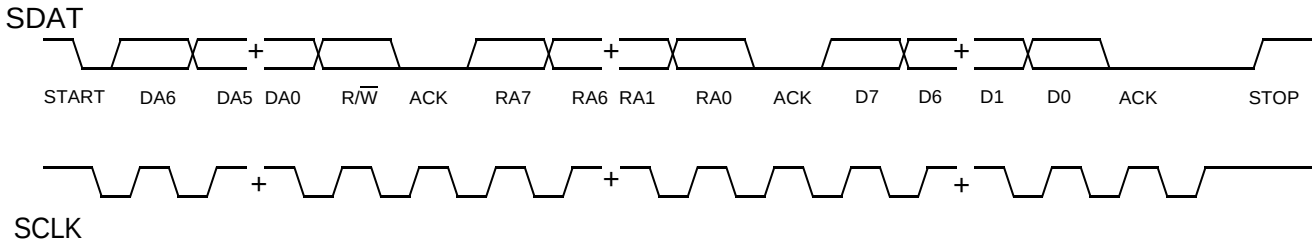
START Sequence: Start frame is indicated by SDAT going LOW when SCLK is HIGH. Every time a start signal is given, the next 8-bit data must be the device address (seven bits) and a R/W bit followed by register address (eight bits) and register data (eight bits).

STOP Sequence: Stop frame is indicated by SDAT going HIGH when SCLK is HIGH. A stop frame frees the bus to write to another part on the same bus or writing to another random register address.

Acknowledge Pulse

During write mode, the CY24488-001 responds with an Acknowledge (ACK) pulse after every eight bits. This is accomplished by pulling the SDAT line LOW during the N*9th clock cycle as shown in Figure 6 (N = the number of bytes transmitted). During read mode, the acknowledge pulse is generated by the master, after the data packet is sent.

Figure 6. Frame Format (Device Address, R/$\overline{W}$, Register Address, Register Data)



Write Operations

Writing Individual Bytes

A valid write operation has a full 8-bit register address after the device address word from the master followed by an acknowledge bit from the slave (SDAT = 0/LOW). The next eight bits contain the data word intended for storage. After the data word is received, the slave responds with another acknowledge bit (SDAT = 0/LOW) and the master ends the write sequence with a STOP condition.

Writing Multiple Bytes

To write more than one byte at a time, the master does not end the write sequence with a STOP condition. Instead, the master sends multiple contiguous bytes of data for storage. After each byte, the slave responds with an acknowledge bit. It is the same as the first byte and accepts data until the acknowledge bit responds to the STOP condition. When receiving multiple bytes, the CY24488-001 internally increments the register address.

Read Operations

Read operations are initiated in the same method as write operations, except that the R/W bit of the slave address is set to ‘1’ (HIGH). There are three basic read operations:

- Current address read
- Random read
- Sequential read

Current Address Read

The CY24488-001 has an onboard address counter that retains ‘1’ more than the address of the last word access. If the last word written or read was word ‘n’, then a current address read operation returns the value stored in location ‘n+1’. When the CY24488-001 receives the slave address with the R/W bit set to a ‘1’, the CY24488-001 issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer but generates a STOP condition that causes the CY24488-001 to stop transmission.

Random Read

Through random read operations, the master accesses any memory location. To perform this type of read operation, first set the word address, then send the address to the CY24488-001 as part of a write operation. After the word address is sent, the master generates a START condition following the acknowledge. This terminates the write operation before any data is stored in the address, but not before the internal address pointer is set. Next, the master reissues the control byte with the R/W byte set to ‘1’. The CY24488-001 then issues an acknowledge and transmits the 8-bit word. The master device does not acknowledge the transfer, but generates a STOP condition that causes the CY24488-001 to stop transmission.

Sequential Read

Sequential read operations follow the same process as random reads, except that the master issues an acknowledge instead of a STOP condition after transmission of the first 8-bit data word. This action results in an incrementing of the internal address pointer and subsequent output of the next 8-bit data word. By continuing to issue acknowledges instead of STOP conditions, the master serially reads the entire contents of the slave device memory. Note that register addresses outside of 0AH to 17H and 40H to 57H are read from, but are not real registers and do not contain configuration information. When the internal address pointer points to the FFH register, after the next increment, the pointer points to the 00H register.

Table 1. Register Settings for AUDIO (Pin 10) Output Frequency

Address	Frequency		
	36.864 (Default)	33.8688	24.576
13H	07H	26H	10H
14H	04H	16H	06H
15H	E0H	F2H	E4H

Table 2. Register Settings for 74M (Pin 8) Output Frequency

Address	Frequency	
	74.17582418 (Default)	74.25
0AH	59H	00H
0BH	F8H	03H
0CH	D8H	C2H

Table 3. Register Settings for 74M Output Control (On/Off)

Address	Pin 8 (74M)	
	On (Default)	Off (Low)
50H	14H	0CH

Table 4. Register Settings for AUDIO Output Control (On/Off)

Address	Pin 10 (AUDIO)	
	On (Default)	Off (Low)
55H	D3H	CFH

Serial Programming Interface Timing

Table 5. Serial Programming Interface Timing Specifications

Parameter	Description	Min	Max	Unit
f_{SCLK}	Frequency of SCLK	–	400	kHz
	Start mode time from SDA LOW to SCL LOW	0.6	–	ms
CLK_{LOW}	SCLK LOW period	1.3	–	ms
CLK_{HIGH}	SCLK HIGH period	0.6	–	ms
t_{SU}	Data transition to SCLK HIGH	100	–	ns
t_{DH}	Data hold (SCLK LOW to data transition)	100	–	ns
	Rise time of SCLK and SDAT	–	300	ns
	Fall time of SCLK and SDAT	–	300	ns
	Stop mode time from SCLK HIGH to SDAT HIGH	0.6	–	ms
	Stop mode to start mode	1.3	–	ms

Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 6. Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
$AV_{DD}/V_{DD1}/V_{DD2}$	Core supply voltage		–0.5	4.6	V
V_{IN}	Input voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, storage	Nonfunctional	–65	+125	°C
ESD_{HBM}	ESD protection (Human Body Model)	JEDEC STD 22-A114-B	2000	–	V
UL-94	Flammability rating	V-0 at 1/8 in.	–	10	ppm
MSL	Moisture sensitivity level	16-pin TSSOP	1		

Crystal Specifications

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{NOM}	AT-cut crystal	Parallel resonance, fundamental mode	–	27	–	MHz
C_{LNOM}	Nominal load capacitance		–	11.5	–	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode (CL = Series)	–	–	40	Ω
DL	Crystal drive level	Nominal V_{DD} at 25 °C	–	–	300	µW

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
AV_{DD}	Core operating voltage	3.0	3.3	3.6	V
V_{DD1}/V_{DD2}	Output operating voltage	3.0	3.3	3.6	V
T_A	Ambient temperature	–10	–	70	°C
C_{LOAD}	Maximum load capacitance	–	–	15	pF
t_{PU}	Power-up time for all V_{DD}'s reach minimum specified voltage (power ramps are monotonic)	0.05	–	500	ms

DC Parameters

Parameter [1]	Description	Conditions	Min	Typ	Max	Unit
I_{OH}	Output high current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3$ V	12	–	–	mA
I_{OL}	Output low current	$V_{OL} = 0.5$, $V_{DD} = 3.3$ V	12	–	–	mA
I_{IH}	Input high current	$V_{IH} = V_{DD}$, excluding XIN/CLKIN	–	5	10	µA
I_{IL}	Input low current	$V_{IL} = 0$ V, excluding XIN/CLKIN	–	5	10	µA
V_{IH}	Input high voltage		0.7 × AV_{DD}	–	–	V
V_{IL}	Input low voltage		–	–	0.3 × AV_{DD}	V
I_{VDD}	Supply current	V_{DD} current	–	40	60	mA

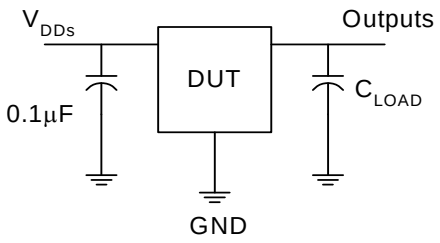
AC Parameters

Parameter [1]	Description	Conditions	Min	Typ	Max	Units
DC_1	Output duty cycle (excluding 27M)	Duty cycle is defined in Figure 8 on page 10; t_2/t_1, 50% of V_{DD} External reference duty cycle between 40% and 60% measured at $V_{DD}/2$	45	50	55	%
DC_{27}	Output duty cycle 27M	Duty cycle is defined in Figure 8 on page 10; t_2/t_1, 50% of V_{DD} (XIN/CLKIN duty cycle = 45/55%)	40	50	60	%
ER	Rising edge rate	Output clock edge rate. Measured from 20% to 80% of V_{DD}. C_{LOAD} = 15 pF. See Figure 9 on page 10.	0.75	1.2	–	V/ns
EF	Falling edge rate	Output clock edge rate. Measured from 80% to 20% of V_{DD}. C_{LOAD} = 15 pF. See Figure 9 on page 10.	0.75	1.2	–	V/ns
T_9	Clock jitter	Period jitter; $V_{DD1} = V_{DD2} = 3.3$ V	–	250	–	ps
T_{10}	PLL lock time	From end of serial programming sequence to correct output frequency	–	1	5	ms

Note
1. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs.

Test and Measurement Setup

Figure 7. Test and Measurement Diagram



Voltage and Timing Definitions

Figure 8. Duty Cycle Definition

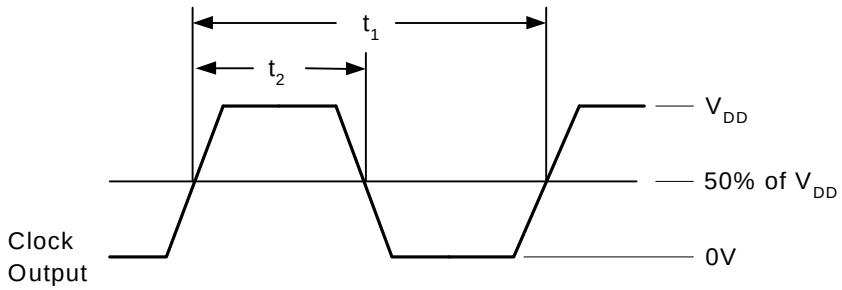
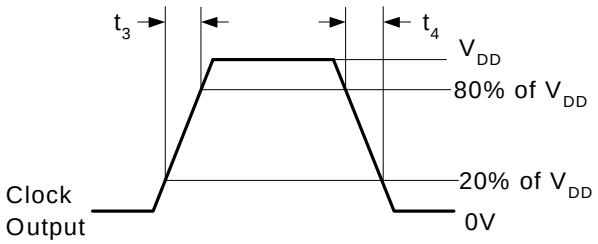


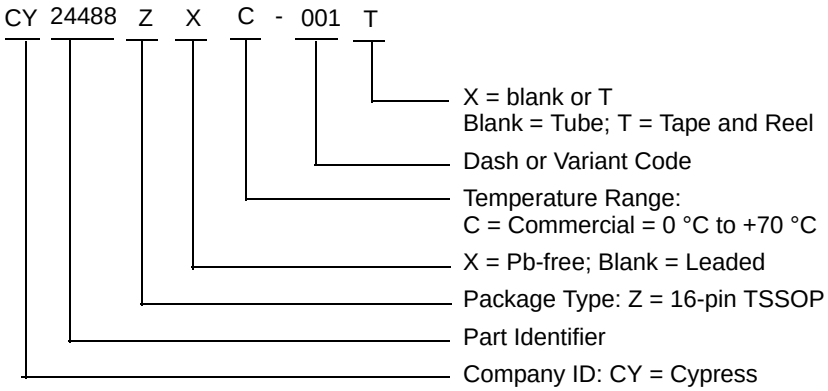
Figure 9. ER = (0.6 × V_{DD})/t_3, EF = (0.6 × V_{DD})/t_4



Ordering Information

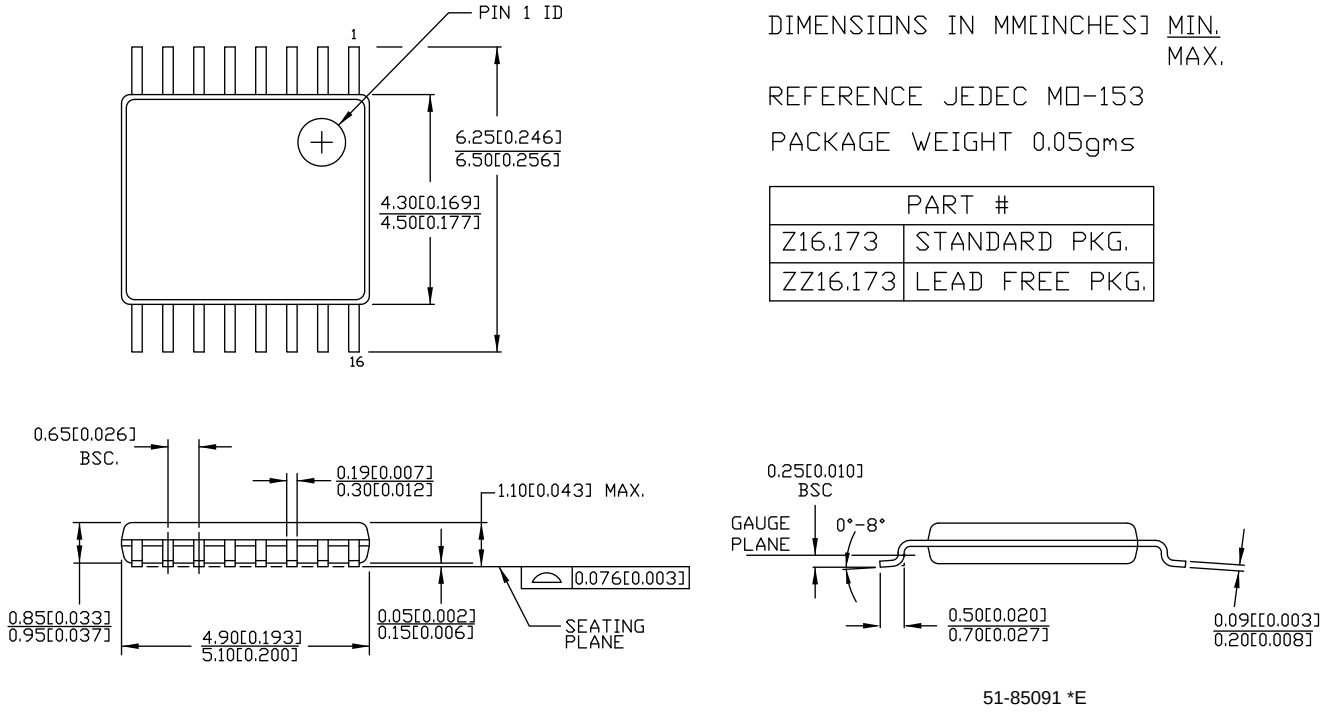
Part Number	Type	Production Flow
Pb-free		
CY24488ZXC-001	16-pin TSSOP	Commercial, 0 °C to +70 °C
CY24488ZXC-001T	16-pin TSSOP – Tape and Reel	Commercial, 0 °C to +70 °C

Ordering Code Definitions



Package Drawing and Dimensions

Figure 10. 16-pin TSSOP (4.40 mm Body) Z16.173/ZZ16.173, 51-85091



Acronyms

Acronym	Description
PLL	Phase-Locked Loop
EMI	Electromagnetic Interference
SPI	Serial Programming Interface
TSSOP	Thin-Shrunk Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Ω	ohm
kΩ	kilohm
kHz	kilohertz
MHz	megahertz
µW	microwatt
µA	microampere
mA	milliampere
ms	millisecond
mW	milliwatt
ns	nanosecond
%	percent
pF	picofarad
ppm	parts per million
ps	picosecond
V	volt

Document History Page

Document Title: CY24488-001, Quad-PLL Clock Generator with Two-Wire Serial Interface Document Number: 001-17448				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	1344564	See ECN	XHT / SFV	Removed VCXO related information in all instances across the document. Updated Logic Block Diagram: Corrected typo (Replaced 36.864M with AUDIO). Updated Pin Definitions: Replaced 36.864 with AUDIO in “Pin Name” column. Added 36.864 MHz in “Pin Description” column corresponding to “AUDIO” pin. Changed I^2C configurations. Deleted unrelated words. Updated Read Operations: Updated Sequential Read: Updated Table 1: Updated I^2C Memory Address. Added AUDIO frequencies. Deleted output frequency. Added Table 3. Added Table 4.
*A	2621905	12/15/2008	KVM / AESA	Updated Document Title to read as “CY24488-001 Quad PLL Clock Generator with 2-Wire Serial Interface”. Replaced “I^2C serial interface” with “2-wire serial interface” in all instances across the document. Updated Serial Programming Interface Timing: Updated Table 5: Changed minimum value of t_{DH} parameter from 0 ns to 100 ns.
*B	3071627	10/26/2010	CXQ	Changed status from Preliminary to Final. Added Ordering Code Definitions under Ordering Information. Updated Package Drawing and Dimensions. Added Acronyms and Units of Measure. Minor edits and updated in new template.
*C	4178019	10/30/2013	CINM	Updated Package Drawing and Dimensions: spec 51-85091 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*D	5534803	11/29/2016	TAVA	Updated Serial Programming Interface Protocol and Timing: Updated Figure 3. Updated Package Drawing and Dimensions: spec 51-85091 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.

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