

Spansion® Analog and Microcontroller Products



The following document contains information on Spansion analog and microcontroller products. Although the document is marked with the name "Fujitsu", the company that originally developed the specification, Spansion will continue to offer these products to new and existing customers.

Continuity of Specifications

There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal document improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

Spansion continues to support existing part numbers beginning with "MB". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local sales office for additional information about Spansion memory, analog, and microcontroller products and solutions.

32-bit ARM™ Cortex™-M3 based Microcontroller

FM3 MB9A100A Series

MB9AF102NA/RA, F104NA/RA, F105NA/RA

■ DESCRIPTION

The MB9A100A Series are a highly integrated 32-bit microcontroller that target for high-performance and cost-sensitive embedded control applications.

The MB9A100A Series are based on the ARM Cortex-M3 Processor and on-chip Flash memory and SRAM, and peripheral functions, including Motor Control Timers, ADCs and Communication Interfaces (UART, CSIO, I²C, LIN).

The products which are described in this data sheet are placed into TYPE0 product categories in "FM3 FAMILY MB9Axxx/MB9Bxxx SERIES PERIPHERAL MANUAL".

Note: ARM and Cortex are the trademarks of ARM Limited in the EU and other countries.



■ FEATURES

● 32-bit ARM Cortex-M3 Core

- Processor version: r2p0
- Up to 40MHz Frequency Operation
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

● On-chip Memories

[Flash memory]

- Up to 384 Kbyte
- Read cycle: 0wait-cycle
- Security function for code protection

[SRAM]

This series contain a total of up to 48Kbyte on-chip SRAM memories. This is composed of two independent SRAM (SRAM0,SRAM1) . SRAM0 is connected to I-code bus or D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: Up to 24 Kbyte.
- SRAM1: Up to 24 Kbyte.

● External Bus Interface

- Supports SRAM, NOR& NAND Flash device
- Up to 8 chip selects
- 8/16-bit Data width
- Up to 25-bit Address bit

● Multi-function Serial Interface (Max. 8channels)

- 4 channels with 16-byte FIFO (ch.4-ch.7), 4 channels without FIFO (ch.0-ch.3)
- Operation mode is selectable from the followings for each channel.
 - UART
 - CSIO
 - LIN
 - I²C

[UART]

- Full-duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[CSIO]

- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detect function available

[LIN]

- LIN protocol Rev.2.1 supported
- Full-duplex double buffer
- Master/Slave mode supported
- LIN break field generate (can be changed 13-16bit length)
- LIN break delimiter generate (can be changed 1-4bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

[²C]

- Standard mode (Max.100kbps) / High-speed mode (Max.400Kbps) supported

● DMA Controller (8channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32bit(4Gbyte)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

● A/D Converter (Max. 16channels)

[12-bit A/D Converter]

- Successive Approximation Register type
- Built-in 3unit
- Conversion time: 1.0μs@5V
- Priority conversion available (priority at 2levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16steps, for Priority conversion: 4steps)

● Base Timer (Max. 8channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

● General Purpose I/O Port

This series can use its pins as I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 100 fast I/O Ports@120pin Package

● Multi-function Timer (Max. 2unit)

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3ch/unit
- Input capture × 4ch/unit
- Output compare × 6ch/unit
- A/D activating compare × 3ch/unit
- Waveform generator × 3ch/unit
- 16-bit PPG timer × 3ch/unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

● Quadrature Position/Revolution Counter (QPRC) (Max. 2unit)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

● Dual Timer (Two 32/16bit Down Counter)

The Dual Timer consists of two programmable 32/16-bit down counters. Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

● Watch Counter

The Watch counter is used for wake up from power saving mode.

- Interval timer: up to 64s(Max.)@ Sub Clock : 32.768kHz

● External Interrupt Controller Unit

- Up to 16 external vectors
- Include one non-maskable interrupt(NMI)

● Watch dog Timer (2channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

"Hardware" watchdog timer is clocked by low speed CR oscillator. Therefore, "Hardware" watchdog is active in any power saving mode except STOP.

● CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

● Clock and Reset

[Clocks]

Five clock sources (2 ext. osc, 2 CR osc, and Main PLL) that are dynamically selectable.

- Main Clock : 4MHz to 48MHz
- Sub Clock : 32.768kHz
- High-speed CR Clock : 4MHz
- Low-speed CR Clock : 100kHz
- Main PLL Clock

[Resets]

Reset requests from INITX pins, Power on reset, Software reset, watchdog timers reset, low voltage detector reset and clock supervisor reset.

● Clock Super Visor (CSV)

Clocks generated by CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

● Low Voltage Detector (LVD)

This series include 2-stage monitoring of voltage on the VCC. When the voltage falls below the voltage has been set, Low Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

● Low Power Mode

Three power saving modes supported.

- SLEEP
- TIMER
- STOP

● Debug

- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

● Power Supply

- VCC = 2.7V to 5.5V: Correspond to the wide range voltage.

MB9A100A Series

■ PRODUCT LINEUP

● Memory size

Product device	MB9AF102NA/RA	MB9AF104NA/RA	MB9AF105NA/RA
On-chip Flash	128Kbyte	256Kbyte	384Kbyte
On-chip SRAM	16Kbyte	32Kbyte	48Kbyte

● Function

Product device			MB9AF102NA MB9AF104NA MB9AF105NA	MB9AF102RA MB9AF104RA MB9AF105RA
Pin count			100	120
CPU			Cortex-M3	
	Freq.		40MHz	
Power supply voltage range			2.7V to 5.5V	
DMAC			8ch	
External Bus Interface			Addr:25bit (Max.) Data:8/16 bit CS:5(Max.) Support: SRAM, NOR Flash	Addr:25bit (Max.) Data:8/16 bit CS:8(Max.) Support: SRAM, NOR & NAND Flash
MF Serial Interface (UART/CSIO/LIN/I ² C)			8ch (Max.)	
Base Timer (PWC/Reload timer/PWM/PPG)			8ch (Max.)	
MF-Timer	A/D activation compare	3ch	2 units (Max.)	
	Input capture	4ch		
	Free-run timer	3ch		
	Output compare	6ch		
	Waveform generator	3ch		
	PPG	3ch		
QPRC			2ch (Max.)	
Dual Timer			1 unit	
Watch Counter			1 unit	
CRC Accelerator			Yes	
Watchdog timer			1ch(SW) + 1ch(HW)	
External Interrupts			16pins (Max.)+ NMI × 1	
I/O ports			80pins (Max.)	100pins (Max.)
12 bit A/D converter			16ch (3 units)	
CSV (Clock Super Visor)			Yes	
LVD (Low Voltage Detector)			2ch	
Internal OSC	High-speed		4MHz (± 2%)	
	Low-speed		100kHz (Typ)	
Debug Function			SWJ-DP/ETM	

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.
It is necessary to use the port relocate function of the General I/O port according to your function use.

MB9A100A Series

■ PACKAGES

Package \ Product name	MB9AF102NA MB9AF104NA MB9AF105NA	MB9AF102RA MB9AF104RA MB9AF105RA
LQFP: FPT-100P-M20*/M23	○	-
LQFP: FPT-120P-M21/M37	-	○
QFP: FPT-100P-M06	○	-
BGA: BGA-112P-M04	○	-

○ : Supported

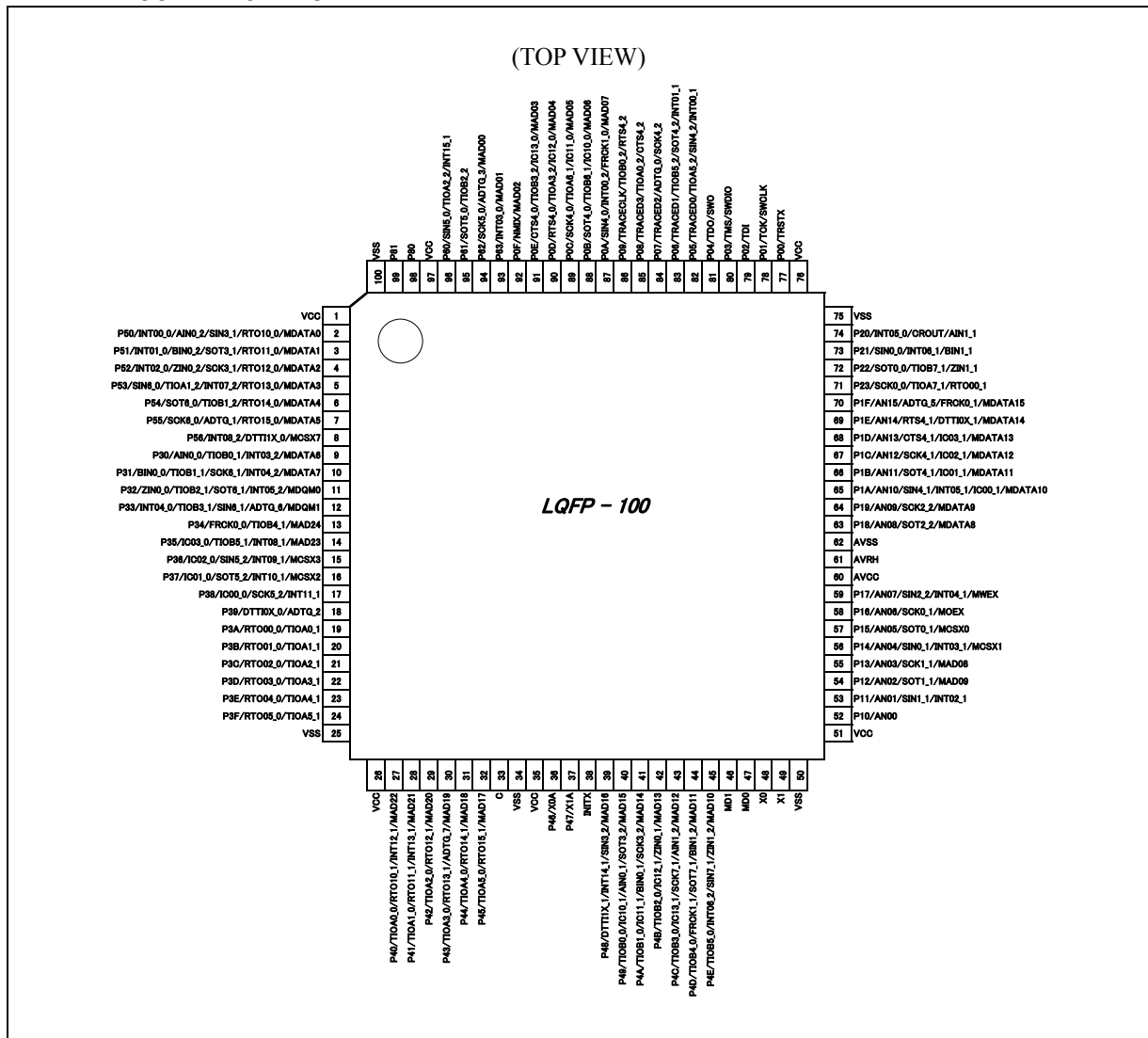
* : ES product only

Note : Refer to "■PACKAGE DIMENSIONS" for detailed information on each package.

MB9A100A Series

■ PIN ASSIGNMENT

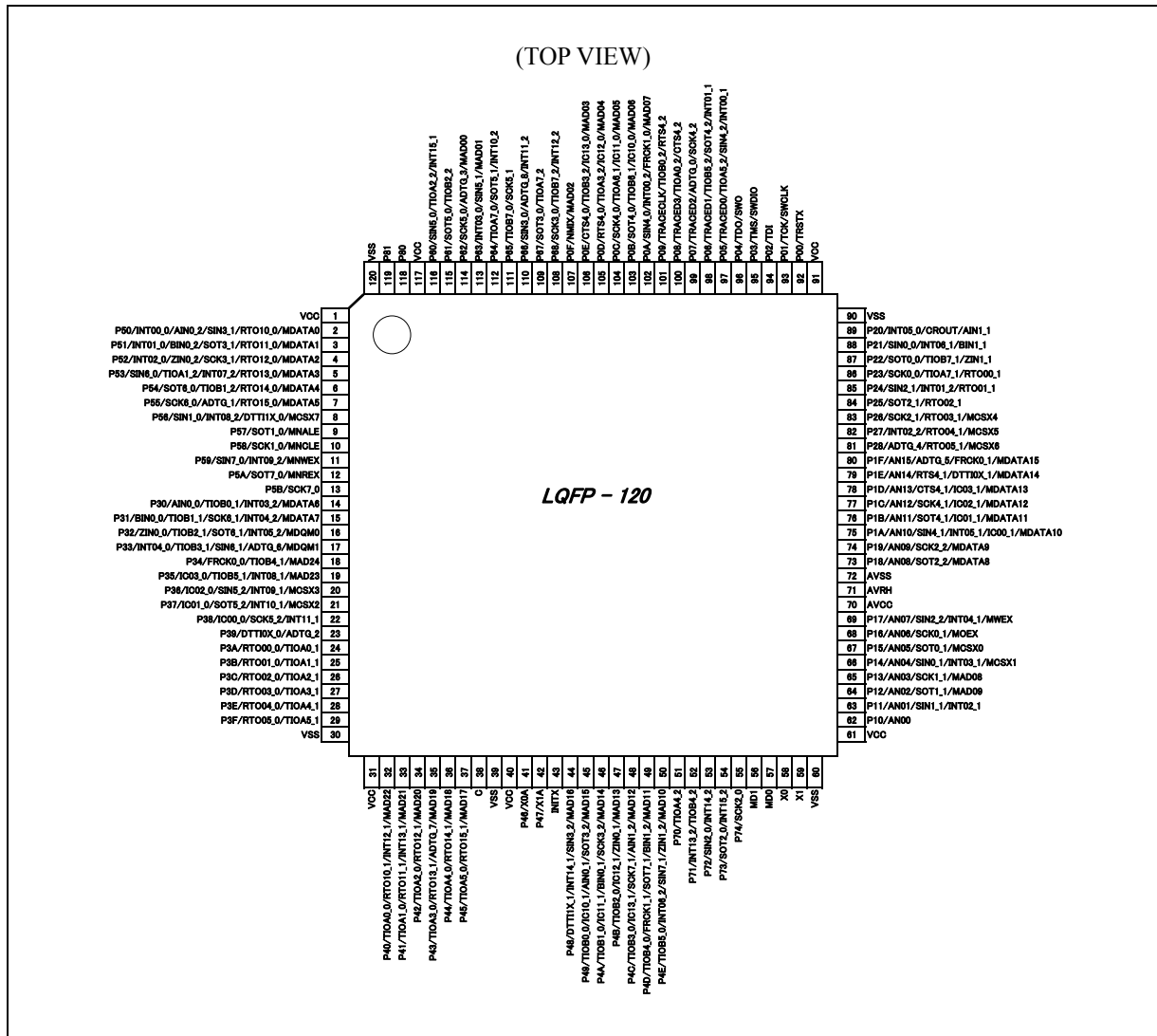
● FPT-100P-M20/M23



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

● FPT-120P-M21/M37

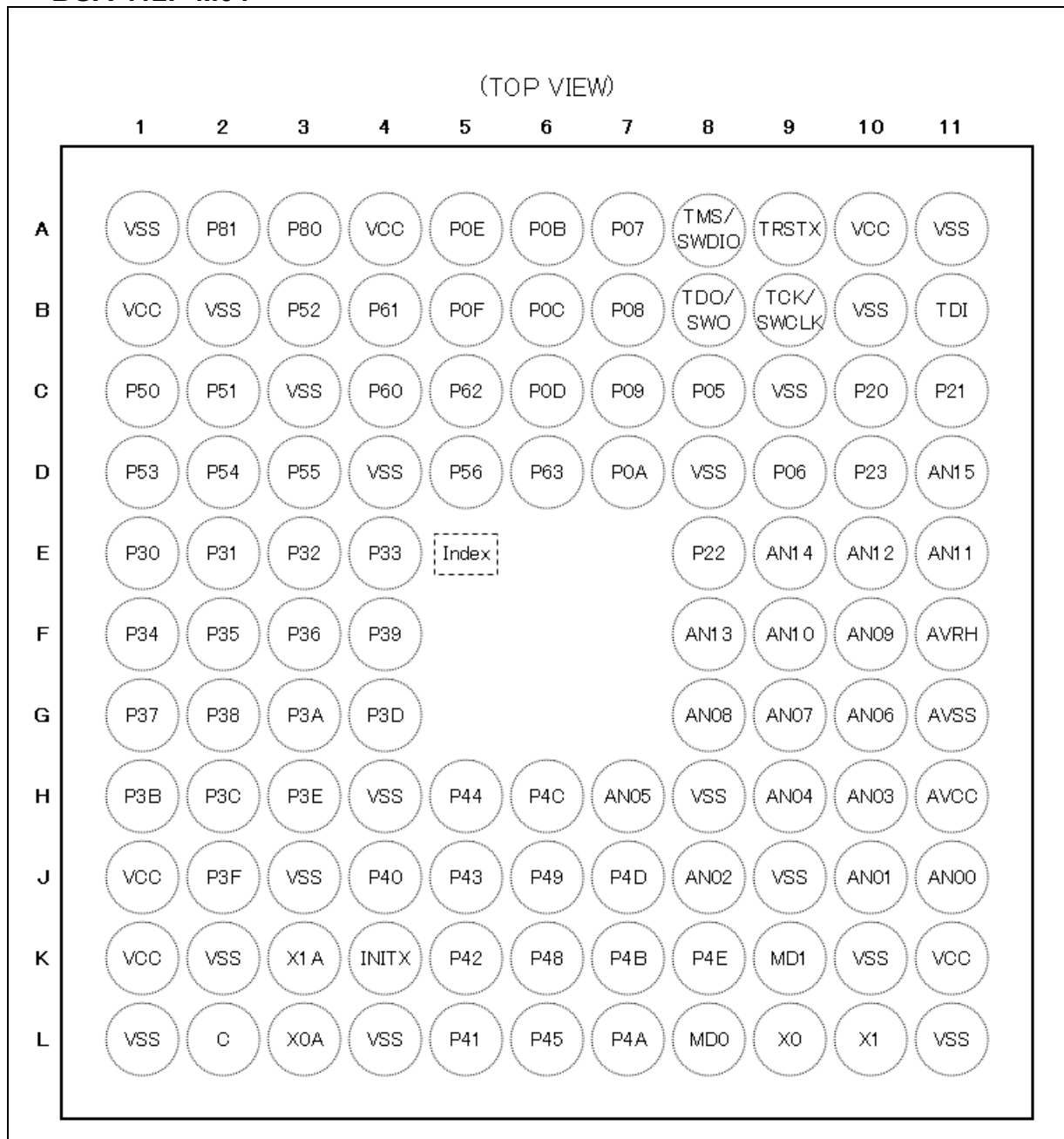


<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

MB9A100A Series

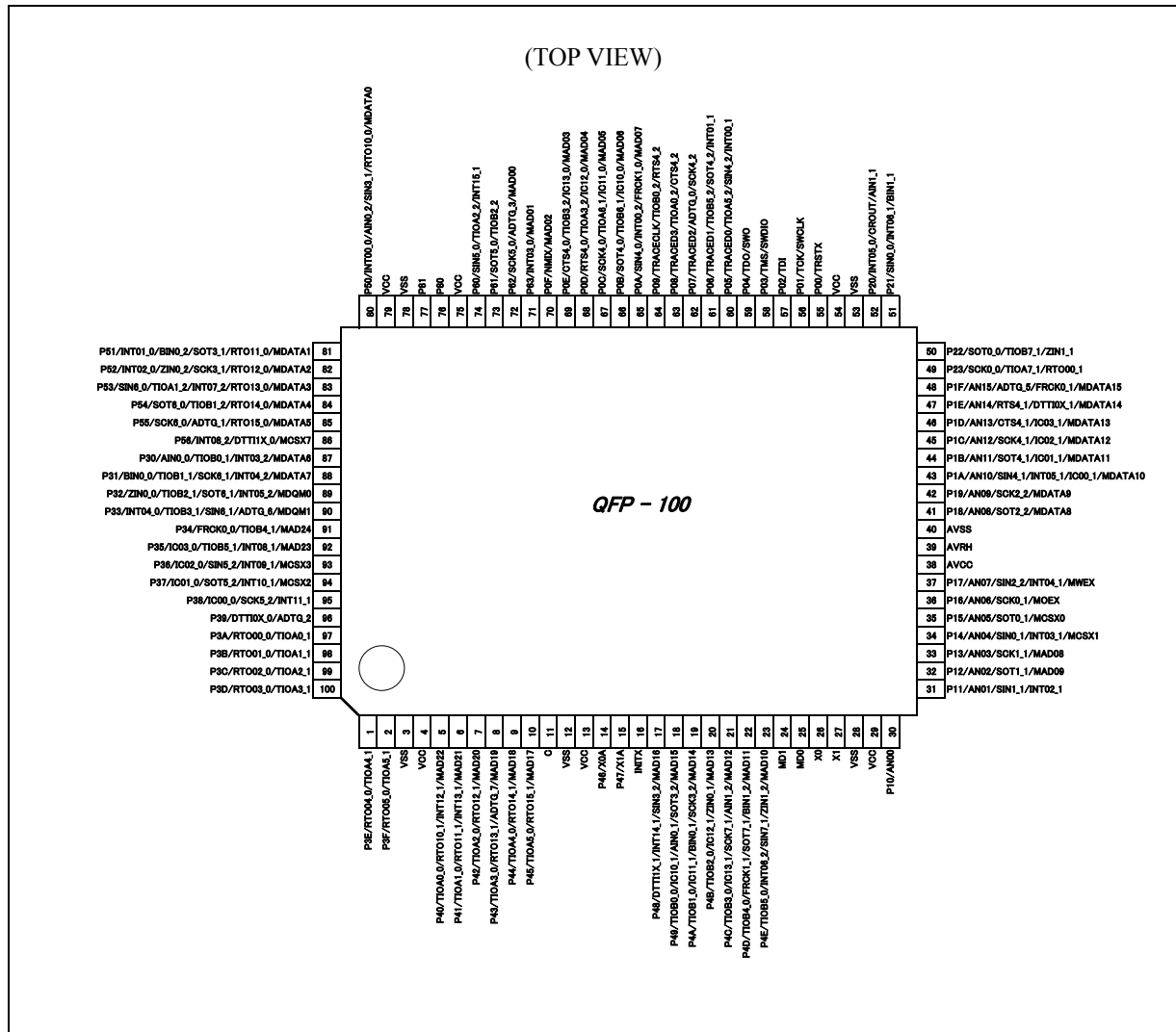
● BGA-112P-M04



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

● FPT-100P-M06



<Note>

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

MB9A100A Series

■ PIN DESCRIPTION

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin no.				Pin name	I/O circuit type	Pin state type
QFP-100	LQFP-100	BGA-112	LQFP-120			
79	1	B1	1	VCC	-	
80	2	C1	2	P50	E	H
				INT00_0		
				AIN0_2		
				SIN3_1		
				RTO10_0 (PPG10_0)		
				MDATA0		
81	3	C2	3	P51	E	H
				INT01_0		
				BIN0_2		
				SOT3_1 (SDA3_1)		
				RTO11_0 (PPG10_0)		
				MDATA1		
82	4	B3	4	P52	E	H
				INT02_0		
				ZIN0_2		
				SCK3_1 (SCL3_1)		
				RTO12_0 (PPG12_0)		
				MDATA2		
83	5	D1	5	P53	E	H
				SIN6_0		
				TIOA1_2		
				INT07_2		
				RTO13_0 (PPG12_0)		
				MDATA3		
84	6	D2	6	P54	E	I
				SOT6_0 (SDA6_0)		
				TIOB1_2		
				RTO14_0 (PPG14_0)		
				MDATA4		

MB9A100A Series

Pin no.				Pin name	I/O circuit type	Pin state type
QFP-100	LQFP-100	BGA-112	LQFP-120			
85	7	D3	7	P55	E	I
				SCK6_0 (SCL6_0)		
				ADTG_1		
				RTO15_0 (PPG14_0)		
				MDATA5		
86	8	D5	8	P56	E	H
				SIN1_0 (120pin only)		
				INT08_2		
				DTTIX_0		
				MCSX7		
-	-	-	9	P57	E	I
				SOT1_0 (SDA1_0)		
				MNALE		
-	-	-	10	P58	E	I
				SCK1_0 (SCL1_0)		
				MNCLE		
-	-	-	11	P59	E	H
				SIN7_0		
				INT09_2		
				MNWEX		
-	-	-	12	P5A	E	I
				SOT7_0 (SDA7_0)		
				MNREX		
-	-	-	13	P5B	E	I
				SCK7_0 (SCL7_0)		
87	9	E1	14	P30	E	H
				AIN0_0		
				TIOB0_1		
				INT03_2		
				MDATA6		
88	10	E2	15	P31	E	H
				BIN0_0		
				TIOB1_1		
				SCK6_1 (SCL6_1)		
				INT04_2		
				MDATA7		

MB9A100A Series

Pin no.				Pin name	I/O circuit type	Pin state type
QFP-100	LQFP-100	BGA-112	LQFP-120			
89	11	E3	16	P32	E	H
				ZIN0_0		
				TIOB2_1		
				SOT6_1 (SDA6_1)		
				INT05_2		
				MDQM0		
90	12	E4	17	P33	E	H
				INT04_0		
				TIOB3_1		
				SIN6_1		
				ADTG_6		
				MDQM1		
91	13	F1	18	P34	E	I
				FRCK0_0		
				TIOB4_1		
				MAD24		
92	14	F2	19	P35	E	H
				IC03_0		
				TIOB5_1		
				INT08_1		
				MAD23		
93	15	F3	20	P36	E	H
				IC02_0		
				SIN5_2		
				INT09_1		
				MCSX3		
94	16	G1	21	P37	E	H
				IC01_0		
				SOT5_2 (SDA5_2)		
				INT10_1		
				MCSX2		
95	17	G2	22	P38	E	H
				IC00_0		
				SCK5_2 (SCL5_2)		
				INT11_1		
96	18	F4	23	P39	E	I
				DTTI0X_0		
				ADTG_2		
97	19	G3	24	P3A	G	I
				RTO00_0 (PPG00_0)		
				TIOA0_1		
-	-	B2	-	VSS	-	-

MB9A100A Series

Pin no.				Pin name	I/O circuit type	Pin state type
QFP-100	LQFP-100	BGA-112	LQFP-120			
98	20	H1	25	P3B	G	I
				RTO01_0 (PPG00_0)		
				TIOA1_1		
99	21	H2	26	P3C	G	I
				RTO02_0 (PPG02_0)		
				TIOA2_1		
100	22	G4	27	P3D	G	I
				RTO03_0 (PPG02_0)		
				TIOA3_1		
1	23	H3	28	P3E	G	I
				RTO04_0 (PPG04_0)		
				TIOA4_1		
2	24	J2	29	P3F	G	I
				RTO05_0 (PPG04_0)		
				TIOA5_1		
3	25	L1	30	VSS	-	
4	26	J1	31	VCC	-	
5	27	J4	32	P40	G	H
				TIOA0_0		
				RTO10_1 (PPG10_1)		
				INT12_1		
				MAD22		
6	28	L5	33	P41	G	H
				TIOA1_0		
				RTO11_1 (PPG10_1)		
				INT13_1		
				MAD21		
7	29	K5	34	P42	G	I
				TIOA2_0		
				RTO12_1 (PPG12_1)		
				MAD20		
8	30	J5	35	P43	G	I
				TIOA3_0		
				RTO13_1 (PPG12_1)		
				ADTG_7		
				MAD19		
-	-	K2	-	VSS	-	
-	-	J3	-	VSS	-	

MB9A100A Series

Pin no.				Pin name	I/O circuit type	Pin state type
QFP-100	LQFP-100	BGA-112	LQFP-120			
-	-	H4	-	VSS	-	
9	31	H5	36	P44	G	I
				TIOA4_0		
				RTO14_1 (PPG14_1)		
				MAD18		
10	32	L6	37	P45	G	I
				TIOA5_0		
				RTO15_1 (PPG14_1)		
				MAD17		
11	33	L2	38	C	-	
12	34	L4	39	VSS	-	
13	35	K1	40	VCC	-	
14	36	L3	41	P46	D	M
				X0A		
15	37	K3	42	P47	D	N
				X1A		
16	38	K4	43	INITX	B	C
17	39	K6	44	P48	E	H
				DTT1IX_1		
				INT14_1		
				SIN3_2		
				MAD16		
18	40	J6	45	P49	E	I
				TIOB0_0		
				IC10_1		
				AIN0_1		
				SOT3_2 (SDA3_2)		
				MAD15		
19	41	L7	46	P4A	E	I
				TIOB1_0		
				IC11_1		
				BIN0_1		
				SCK3_2 (SCL3_2)		
				MAD14		
20	42	K7	47	P4B	E	I
				TIOB2_0		
				IC12_1		
				ZIN0_1		
				MAD13		

MB9A100A Series

Pin no.				Pin name	I/O circuit type	Pin state type
QFP-100	LQFP-100	BGA-112	LQFP-120			
21	43	H6	48	P4C	E	I
				TIOB3_0		
				IC13_1		
				SCK7_1 (SCL7_1)		
				AIN1_2		
				MAD12		
22	44	J7	49	P4D	E	I
				TIOB4_0		
				FRCK1_1		
				SOT7_1 (SDA7_1)		
				BIN1_2		
				MAD11		
23	45	K8	50	P4E	E	I
				TIOB5_0		
				INT06_2		
				SIN7_1		
				ZIN1_2		
				MAD10		
-	-	-	51	P70	E	I
				TIOA4_2		
-	-	-	52	P71	E	H
				INT13_2		
				TIOB4_2		
-	-	-	53	P72	E	H
				SIN2_0		
				INT14_2		
-	-	-	54	P73	E	H
				SOT2_0 (SDA2_0)		
				INT15_2		
-	-	-	55	P74	E	I
				SCK2_0 (SCL2_0)		
24	46	K9	56	MD1	C	D
25	47	L8	57	MD0	C	D
26	48	L9	58	X0	A	A
27	49	L10	59	X1	A	B
28	50	L11	60	VSS	-	
29	51	K11	61	VCC	-	
30	52	J11	62	P10	F	K
				AN00		

MB9A100A Series

Pin no.				Pin name	I/O circuit type	Pin state type
QFP-100	LQFP-100	BGA-112	LQFP-120			
31	53	J10	63	P11	F	L
				AN01		
				SIN1_1		
				INT02_1		
-	-	K10	-	VSS	-	
-	-	J9	-	VSS	-	
32	54	J8	64	P12	F	K
				AN02		
				SOT1_1 (SDA1_1)		
				MAD09		
33	55	H10	65	P13	F	K
				AN03		
				SCK1_1 (SCL1_1)		
				MAD08		
34	56	H9	66	P14	F	L
				AN04		
				SIN0_1		
				INT03_1		
				MCSX1		
35	57	H7	67	P15	F	K
				AN05		
				SOT0_1 (SDA0_1)		
				MCSX0		
36	58	G10	68	P16	F	K
				AN06		
				SCK0_1 (SCL0_1)		
				MOEX		
37	59	G9	69	P17	F	L
				AN07		
				SIN2_2		
				INT04_1		
				MWEX		
38	60	H11	70	AVCC	-	
39	61	F11	71	AVRH	-	
40	62	G11	72	AVSS	-	
41	63	G8	73	P18	F	K
				AN08		
				SOT2_2 (SDA2_2)		
				MDATA8		

MB9A100A Series

Pin no.				Pin name	I/O circuit type	Pin state type
QFP-100	LQFP-100	BGA-112	LQFP-120			
42	64	F10	74	P19	F	K
				AN09		
				SCK2_2 (SCL2_2)		
				MDATA9		
43	65	F9	75	P1A	F	L
				AN10		
				SIN4_1		
				INT05_1		
				IC00_1		
				MDATA10		
-	-	H8	-	VSS	-	
44	66	E11	76	P1B	F	K
				AN11		
				SOT4_1 (SDA4_1)		
				IC01_1		
				MDATA11		
45	67	E10	77	P1C	F	K
				AN12		
				SCK4_1 (SCL4_1)		
				IC02_1		
				MDATA12		
46	68	F8	78	P1D	F	K
				AN13		
				CTS4_1		
				IC03_1		
				MDATA13		
47	69	E9	79	P1E	F	K
				AN14		
				RTS4_1		
				DTTI0X_1		
				MDATA14		
48	70	D11	80	P1F	F	K
				AN15		
				ADTG_5		
				FRCK0_1		
				MDATA15		
-	-	-	81	P28	E	I
				ADTG_4		
				RTO05_1 (PPG04_1)		
				MCSX6		

MB9A100A Series

Pin no.				Pin name	I/O circuit type	Pin state type
QFP-100	LQFP-100	BGA-112	LQFP-120			
-	-	-	82	P27	E	H
				INT02_2		
				RTO04_1 (PPG04_1)		
				MCSX5		
-	-	-	83	P26	E	I
				SCK2_1 (SCL2_1)		
				RTO03_1 (PPG02_1)		
				MCSX4		
-	-	-	84	P25	E	I
				SOT2_1 (SDA2_1)		
				RTO02_1 (PPG02_1)		
-	-	B10	-	VSS	-	
-	-	C9	-	VSS	-	
-	-	-	85	P24	E	H
				SIN2_1		
				INT01_2		
				RTO01_1 (PPG00_1)		
49	71	D10	86	P23	E	I
				SCK0_0 (SCL0_0)		
				TIOA7_1		
				RTO00_1 (PPG00_1)		
50	72	E8	87	P22	E	I
				SOT0_0 (SDA0_0)		
				TIOB7_1		
				ZIN1_1		
51	73	C11	88	P21	E	H
				SIN0_0		
				INT06_1		
				BIN1_1		
52	74	C10	89	P20	E	H
				INT05_0		
				CROUT		
				AIN1_1		
53	75	A11	90	VSS	-	
54	76	A10	91	VCC	-	

MB9A100A Series

Pin no.				Pin name	I/O circuit type	Pin state type
QFP-100	LQFP-100	BGA-112	LQFP-120			
55	77	A9	92	P00	E	E
				TRSTX		
56	78	B9	93	P01	E	E
				TCK		
				SWCLK		
57	79	B11	94	P02	E	E
				TDI		
58	80	A8	95	P03	E	E
				TMS		
				SWDIO		
59	81	B8	96	P04	E	E
				TDO		
				SWO		
60	82	C8	97	P05	E	F
				TRACED0		
				TIOA5_2		
				SIN4_2		
				INT00_1		
-	-	D8	-	VSS	-	
61	83	D9	98	P06	E	F
				TRACED1		
				TIOB5_2		
				SOT4_2 (SDA4_2)		
				INT01_1		
62	84	A7	99	P07	E	G
				TRACED2		
				ADTG_0		
				SCK4_2 (SCL4_2)		
63	85	B7	100	P08	E	G
				TRACED3		
				TIOA0_2		
				CTS4_2		
64	86	C7	101	P09	E	G
				TRACECLK		
				TIOB0_2		
				RTS4_2		
65	87	D7	102	P0A	E	H
				SIN4_0		
				INT00_2		
				FRCK1_0		
				MAD07		

MB9A100A Series

Pin no.				Pin name	I/O circuit type	Pin state type
QFP-100	LQFP-100	BGA-112	LQFP-120			
66	88	A6	103	P0B	E	I
				SOT4_0 (SDA4_0)		
				TIOB6_1		
				IC10_0		
				MAD06		
67	89	B6	104	P0C	E	I
				SCK4_0 (SCL4_0)		
				TIOA6_1		
				IC11_0		
				MAD05		
68	90	C6	105	P0D	E	I
				RTS4_0		
				TIOA3_2		
				IC12_0		
				MAD04		
69	91	A5	106	P0E	E	I
				CTS4_0		
				TIOB3_2		
				IC13_0		
				MAD03		
-	-	D4	-	VSS	-	
-	-	C3	-	VSS	-	
70	92	B5	107	P0F	E	J
				NMIX		
				MAD02		
-	-	-	108	P68	E	H
				SCK3_0 (SCL3_0)		
				TIOB7_2		
				INT12_2		
-	-	-	109	P67	E	I
				SOT3_0 (SDA3_0)		
				TIOA7_2		
-	-	-	110	P66	E	H
				SIN3_0		
				ADTG_8		
				INT11_2		
-	-	-	111	P65	E	I
				TIOB7_0		
				SCK5_1 (SCL5_1)		

MB9A100A Series

Pin no.				Pin name	I/O circuit type	Pin state type	
QFP-100	LQFP-100	BGA-112	LQFP-120				
-	-	-	112	P64	E	H	
				TIOA7_0			
				SOT5_1 (SDA5_1)			
				INT10_2			
71	93	D6	113	P63	E	H	
							INT03_0
							MAD01
-	-	-					SIN5_1
72	94	C5	114	P62	E	I	
				SCK5_0 (SCL5_0)			
				ADTG_3			
				MAD00			
73	95	B4	115	P61	E	I	
				SOT5_0 (SDA5_0)			
				TIOB2_2			
74	96	C4	116	P60	E	H	
				SIN5_0			
				TIOA2_2			
				INT15_1			
75	97	A4	117	VCC	-		
76	98	A3	118	P80	H	O	
77	99	A2	119	P81	H	O	
78	100	A1	120	VSS	-		

MB9A100A Series

■ SIGNAL DESCRIPTION

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.			
			QFP-100	LQFP-100	BGA-112	LQFP-120
ADC	ADTG_0	A/D converter external trigger input pin.	62	84	A7	99
	ADTG_1		85	7	D3	7
	ADTG_2		96	18	F4	23
	ADTG_3		72	94	C5	114
	ADTG_4		-	-	-	81
	ADTG_5		48	70	D11	80
	ADTG_6		90	12	E4	17
	ADTG_7		8	30	J5	35
	ADTG_8		-	-	-	110
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	30	52	J11	62
	AN01		31	53	J10	63
	AN02		32	54	J8	64
	AN03		33	55	H10	65
	AN04		34	56	H9	66
	AN05		35	57	H7	67
	AN06		36	58	G10	68
	AN07		37	59	G9	69
	AN08		41	63	G8	73
	AN09		42	64	F10	74
	AN10		43	65	F9	75
	AN11		44	66	E11	76
	AN12		45	67	E10	77
	AN13		46	68	F8	78
	AN14		47	69	E9	79
	AN15		48	70	D11	80
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin.	5	27	J4	32
	TIOA0_1		97	19	G3	24
	TIOA0_2		63	85	B7	100
	TIOB0_0	Base timer ch.0 TIOB pin.	18	40	J6	45
	TIOB0_1		87	9	E1	14
	TIOB0_2		64	86	C7	101
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin.	6	28	L5	33
	TIOA1_1		98	20	H1	25
	TIOA1_2		83	5	D1	5
	TIOB1_0	Base timer ch.1 TIOB pin.	19	41	L7	46
	TIOB1_1		88	10	E2	15
	TIOB1_2		84	6	D2	6
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin.	7	29	K5	34
	TIOA2_1		99	21	H2	26
	TIOA2_2		74	96	C4	116
	TIOB2_0	Base timer ch.2 TIOB pin.	20	42	K7	47
	TIOB2_1		89	11	E3	16
	TIOB2_2		73	95	B4	115

MB9A100A Series

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.			
			QFP-100	LQFP-100	BGA-112	LQFP-120
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin.	8	30	J5	35
	TIOA3_1		100	22	G4	27
	TIOA3_2		68	90	C6	105
	TIOB3_0	Base timer ch.3 TIOB pin.	21	43	H6	48
	TIOB3_1		90	12	E4	17
	TIOB3_2		69	91	A5	106
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin.	9	31	H5	36
	TIOA4_1		1	23	H3	28
	TIOA4_2		-	-	-	51
	TIOB4_0	Base timer ch.4 TIOB pin.	22	44	J7	49
	TIOB4_1		91	13	F1	18
	TIOB4_2		-	-	-	52
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin.	10	32	L6	37
	TIOA5_1		2	24	J2	29
	TIOA5_2		60	82	C8	97
	TIOB5_0	Base timer ch.5 TIOB pin.	23	45	K8	50
	TIOB5_1		92	14	F2	19
	TIOB5_2		61	83	D9	98
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin.	67	89	B6	104
	TIOB6_1	Base timer ch.6 TIOB pin.	66	88	A6	103
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin.	-	-	-	112
	TIOA7_1		49	71	D10	86
	TIOA7_2		-	-	-	109
	TIOB7_0	Base timer ch.7 TIOB pin.	-	-	-	111
	TIOB7_1		50	72	E8	87
	TIOB7_2		-	-	-	108

MB9A100A Series

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.			
			QFP-100	LQFP-100	BGA-112	LQFP-120
Debugger	SWCLK	Serial wire debug interface clock input.	56	78	B9	93
	SWDIO	Serial wire debug interface data input / output.	58	80	A8	95
	SWO	Serial wire viewer output.	59	81	B8	96
	TCK	J-TAG test clock input.	56	78	B9	93
	TDI	J-TAG test data input.	57	79	B11	94
	TDO	J-TAG debug data output.	59	81	B8	96
	TMS	J-TAG test mode state input/output.	58	80	A8	95
	TRACECLK	Trace CLK output of ETM.	64	86	C7	101
	TRACED0	Trace data output of ETM.	60	82	C8	97
	TRACED1		61	83	D9	98
	TRACED2		62	84	A7	99
	TRACED3		63	85	B7	100
	TRSTX	J-TAG test reset Input.	55	77	A9	92
External Bus	MAD00	External bus interface address bus.	72	94	C5	114
	MAD01		71	93	D6	113
	MAD02		70	92	B5	107
	MAD03		69	91	A5	106
	MAD04		68	90	C6	105
	MAD05		67	89	B6	104
	MAD06		66	88	A6	103
	MAD07		65	87	D7	102
	MAD08		33	55	H10	65
	MAD09		32	54	J8	64
	MAD10		23	45	K8	50
	MAD11		22	44	J7	49
	MAD12		21	43	H6	48
	MAD13		20	42	K7	47
	MAD14		19	41	L7	46
	MAD15		18	40	J6	45
	MAD16		17	39	K6	44
	MAD17		10	32	L6	37
	MAD18		9	31	H5	36
	MAD19		8	30	J5	35
	MAD20		7	29	K5	34
	MAD21		6	28	L5	33
	MAD22		5	27	J4	32
	MAD23		92	14	F2	19
	MAD24		91	13	F1	18
	MCSX0	External bus interface chip select output pin.	35	57	H7	67
	MCSX1		34	56	H9	66
	MCSX2		94	16	G1	21
	MCSX3		93	15	F3	20
	MCSX4		-	-	-	83
	MCSX5		-	-	-	82
	MCSX6		-	-	-	81
	MCSX7		86	8	D5	8

MB9A100A Series

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.			
			QFP-100	LQFP-100	BGA-112	LQFP-120
External Bus	MDATA0	External bus interface data bus.	80	2	C1	2
	MDATA1		81	3	C2	3
	MDATA2		82	4	B3	4
	MDATA3		83	5	D1	5
	MDATA4		84	6	D2	6
	MDATA5		85	7	D3	7
	MDATA6		87	9	E1	14
	MDATA7		88	10	E2	15
	MDATA8		41	63	G8	73
	MDATA9		42	64	F10	74
	MDATA10		43	65	F9	75
	MDATA11		44	66	E11	76
	MDATA12		45	67	E10	77
	MDATA13		46	68	F8	78
	MDATA14		47	69	E9	79
	MDATA15		48	70	D11	80
	MDQM0	External bus interface byte mask signal output.	89	11	E3	16
	MDQM1		90	12	E4	17
	MNALE	External bus interface ALE signal to control NAND Flash output pin.	-	-	-	9
	MNCLE	External bus interface CLE signal to control NAND Flash output pin.	-	-	-	10
	MNREX	External bus interface read enable signal to control NAND Flash.	-	-	-	12
	MNWEX	External bus interface write enable signal to control NAND Flash.	-	-	-	11
	MOEX	External bus interface read enable signal for SRAM.	36	58	G10	68
	MWEX	External bus interface write enable signal for SRAM.	37	59	G9	69

MB9A100A Series

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.			
			QFP-100	LQFP-100	BGA-112	LQFP-120
External Interrupt	INT00_0	External interrupt request 00 input pin.	80	2	C1	2
	INT00_1		60	82	C8	97
	INT00_2		65	87	D7	102
	INT01_0	External interrupt request 01 input pin.	81	3	C2	3
	INT01_1		61	83	D9	98
	INT01_2		-	-	-	85
	INT02_0	External interrupt request 02 input pin.	82	4	B3	4
	INT02_1		31	53	J10	63
	INT02_2		-	-	-	82
	INT03_0	External interrupt request 03 input pin.	71	93	D6	113
	INT03_1		34	56	H9	66
	INT03_2		87	9	E1	14
	INT04_0	External interrupt request 04 input pin.	90	12	E4	17
	INT04_1		37	59	G9	69
	INT04_2		88	10	E2	15
	INT05_0	External interrupt request 05 input pin.	52	74	C10	89
	INT05_1		43	65	F9	75
	INT05_2		89	11	E3	16
	INT06_1	External interrupt request 06 input pin.	51	73	C11	88
	INT06_2		23	45	K8	50
	INT07_2	External interrupt request 07 input pin.	83	5	D1	5
	INT08_1	External interrupt request 08 input pin.	92	14	F2	19
	INT08_2		86	8	D5	8
	INT09_1	External interrupt request 09 input pin.	93	15	F3	20
	INT09_2		-	-	-	11
	INT10_1	External interrupt request 10 input pin.	94	16	G1	21
	INT10_2		-	-	-	112
	INT11_1	External interrupt request 11 input pin.	95	17	G2	22
	INT11_2		-	-	-	110
	INT12_1	External interrupt request 12 input pin.	5	27	J4	32
	INT12_2		-	-	-	108
	INT13_1	External interrupt request 13 input pin.	6	28	L5	33
	INT13_2		-	-	-	52
	INT14_1	External interrupt request 14 input pin.	17	39	K6	44
	INT14_2		-	-	-	53
	INT15_1	External interrupt request 15 input pin.	74	96	C4	116
	INT15_2		-	-	-	54
	NMIX	Non-Maskable Interrupt input.	70	92	B5	107

MB9A100A Series

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.			
			QFP-100	LQFP-100	BGA-112	LQFP-120
GPIO	P00	General-purpose I/O port 0.	55	77	A9	92
	P01		56	78	B9	93
	P02		57	79	B11	94
	P03		58	80	A8	95
	P04		59	81	B8	96
	P05		60	82	C8	97
	P06		61	83	D9	98
	P07		62	84	A7	99
	P08		63	85	B7	100
	P09		64	86	C7	101
	P0A		65	87	D7	102
	P0B		66	88	A6	103
	P0C		67	89	B6	104
	P0D		68	90	C6	105
	P0E		69	91	A5	106
	P0F		70	92	B5	107
	P10	General-purpose I/O port 1.	30	52	J11	62
	P11		31	53	J10	63
	P12		32	54	J8	64
	P13		33	55	H10	65
	P14		34	56	H9	66
	P15		35	57	H7	67
	P16		36	58	G10	68
	P17		37	59	G9	69
	P18		41	63	G8	73
	P19		42	64	F10	74
	P1A		43	65	F9	75
	P1B		44	66	E11	76
	P1C		45	67	E10	77
	P1D		46	68	F8	78
	P1E		47	69	E9	79
	P1F		48	70	D11	80
	P20	General-purpose I/O port 2.	52	74	C10	89
	P21		51	73	C11	88
	P22		50	72	E8	87
	P23		49	71	D10	86
	P24		-	-	-	85
	P25		-	-	-	84
	P26		-	-	-	83
	P27		-	-	-	82
	P28		-	-	-	81

MB9A100A Series

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.			
			QFP-100	LQFP-100	BGA-112	LQFP-120
GPIO	P30	General-purpose I/O port 3.	87	9	E1	14
	P31		88	10	E2	15
	P32		89	11	E3	16
	P33		90	12	E4	17
	P34		91	13	F1	18
	P35		92	14	F2	19
	P36		93	15	F3	20
	P37		94	16	G1	21
	P38		95	17	G2	22
	P39		96	18	F4	23
	P3A		97	19	G3	24
	P3B		98	20	H1	25
	P3C		99	21	H2	26
	P3D		100	22	G4	27
	P3E		1	23	H3	28
	P3F		2	24	J2	29
	P40	General-purpose I/O port 4.	5	27	J4	32
	P41		6	28	L5	33
	P42		7	29	K5	34
	P43		8	30	J5	35
	P44		9	31	H5	36
	P45		10	32	L6	37
	P46		14	36	L3	41
	P47		15	37	K3	42
	P48		17	39	K6	44
	P49		18	40	J6	45
	P4A		19	41	L7	46
	P4B		20	42	K7	47
	P4C		21	43	H6	48
	P4D		22	44	J7	49
	P4E		23	45	K8	50
	P50	General-purpose I/O port 5.	80	2	C1	2
	P51		81	3	C2	3
	P52		82	4	B3	4
	P53		83	5	D1	5
	P54		84	6	D2	6
	P55		85	7	D3	7
	P56		86	8	D5	8
	P57		-	-	-	9
	P58		-	-	-	10
	P59		-	-	-	11
	P5A		-	-	-	12
	P5B		-	-	-	13

MB9A100A Series

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.			
			QFP-100	LQFP-100	BGA-112	LQFP-120
GPIO	P60	General-purpose I/O port 6.	74	96	C4	116
	P61		73	95	B4	115
	P62		72	94	C5	114
	P63		71	93	D6	113
	P64		-	-	-	112
	P65		-	-	-	111
	P66		-	-	-	110
	P67		-	-	-	109
	P68		-	-	-	108
	P70	General-purpose I/O port 7.	-	-	-	51
	P71		-	-	-	52
	P72		-	-	-	53
	P73		-	-	-	54
	P74		-	-	-	55
	P80	General-purpose I/O port 8.	76	98	A3	118
	P81		77	99	A2	119
Multi Function Serial 0	SIN0_0	Multifunction serial interface ch.0 input pin.	51	73	C11	88
	SIN0_1		34	56	H9	66
	SOT0_0 (SDA0_0)	Multifunction serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA0 when it is used in an I ² C (operation mode 4).	50	72	E8	87
	SOT0_1 (SDA0_1)		35	57	H7	67
	SCK0_0 (SCL0_0)	Multifunction serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL0 when it is used in an I ² C (operation mode 4).	49	71	D10	86
	SCK0_1 (SCL0_1)		36	58	G10	68
Multi Function Serial 1	SIN1_0	Multifunction serial interface ch.1 input pin.	-	-	-	8
	SIN1_1		31	53	J10	63
	SOT1_0 (SDA1_0)	Multifunction serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA1 when it is used in an I ² C (operation mode 4).	-	-	-	9
	SOT1_1 (SDA1_1)		32	54	J8	64
	SCK1_0 (SCL1_0)	Multifunction serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1 when it is used in an I ² C (operation mode 4).	-	-	-	10
	SCK1_1 (SCL1_1)		33	55	H10	65

MB9A100A Series

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.			
			QFP-100	LQFP-100	BGA-112	LQFP-120
Multi Function Serial 2	SIN2_0	Multifunction serial interface ch.2 input pin.	-	-	-	53
	SIN2_1		-	-	-	85
	SIN2_2		37	59	G9	69
	SOT2_0 (SDA2_0)	Multifunction serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA2 when it is used in an I ² C (operation mode 4).	-	-	-	54
	SOT2_1 (SDA2_1)		-	-	-	84
	SOT2_2 (SDA2_2)		41	63	G8	73
	SCK2_0 (SCL2_0)	Multifunction serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an I ² C (operation mode 4).	-	-	-	55
	SCK2_1 (SCL2_1)		-	-	-	83
	SCK2_2 (SCL2_2)		42	64	F10	74
Multi Function Serial 3	SIN3_0	Multifunction serial interface ch.3 input pin.	-	-	-	110
	SIN3_1		80	2	C1	2
	SIN3_2		17	39	K6	44
	SOT3_0 (SDA3_0)	Multifunction serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA3 when it is used in an I ² C (operation mode 4).	-	-	-	109
	SOT3_1 (SDA3_1)		81	3	C2	3
	SOT3_2 (SDA3_2)		18	40	J6	45
	SCK3_0 (SCL3_0)	Multifunction serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3 when it is used in an I ² C (operation mode 4).	-	-	-	108
	SCK3_1 (SCL3_1)		82	4	B3	4
	SCK3_2 (SCL3_2)		19	41	L7	46

MB9A100A Series

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.			
			QFP-100	LQFP-100	BGA-112	LQFP-120
Multi Function Serial 4	SIN4_0	Multifunction serial interface ch.4 input pin.	65	87	D7	102
	SIN4_1		43	65	F9	75
	SIN4_2		60	82	C8	97
	SOT4_0 (SDA4_0)	Multifunction serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA4 when it is used in an I ² C (operation mode 4).	66	88	A6	103
	SOT4_1 (SDA4_1)		44	66	E11	76
	SOT4_2 (SDA4_2)		61	83	D9	98
	SCK4_0 (SCL4_0)	Multifunction serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4 when it is used in an I ² C (operation mode 4).	67	89	B6	104
	SCK4_1 (SCL4_1)		45	67	E10	77
	SCK4_2 (SCL4_2)		62	84	A7	99
	RTS4_0	Multifunction serial interface ch.4 RTS output pin.	68	90	C6	105
	RTS4_1		47	69	E9	79
	RTS4_2		64	86	C7	101
	CTS4_0	Multifunction serial interface ch.4 CTS input pin.	69	91	A5	106
	CTS4_1		46	68	F8	78
	CTS4_2		63	85	B7	100
Multi Function Serial 5	SIN5_0	Multifunction serial interface ch.5 input pin.	74	96	C4	116
	SIN5_1		-	-	-	113
	SIN5_2		93	15	F3	20
	SOT5_0 (SDA5_0)	Multifunction serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA5 when it is used in an I ² C (operation mode 4).	73	95	B4	115
	SOT5_1 (SDA5_1)		-	-	-	112
	SOT5_2 (SDA5_2)		94	16	G1	21
	SCK5_0 (SCL5_0)	Multifunction serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5 when it is used in an I ² C (operation mode 4).	72	94	C5	114
	SCK5_1 (SCL5_1)		-	-	-	111
	SCK5_2 (SCL5_2)		95	17	G2	22

MB9A100A Series

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.			
			QFP-100	LQFP-100	BGA-112	LQFP-120
Multi Function Serial 6	SIN6_0	Multifunction serial interface ch.6 input pin.	83	5	D1	5
	SIN6_1		90	12	E4	17
	SOT6_0 (SDA6_0)	Multifunction serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6 when it is used in an I ² C (operation mode 4).	84	6	D2	6
	SOT6_1 (SDA6_1)		89	11	E3	16
	SCK6_0 (SCL6_0)	Multifunction serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I ² C (operation mode 4).	85	7	D3	7
	SCK6_1 (SCL6_1)		88	10	E2	15
Multi Function Serial 7	SIN7_0	Multifunction serial interface ch.7 input pin.	-	-	-	11
	SIN7_1		23	45	K8	50
	SOT7_0 (SDA7_0)	Multifunction serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA7 when it is used in an I ² C (operation mode 4).	-	-	-	12
	SOT7_1 (SDA7_1)		22	44	J7	49
	SCK7_0 (SCL7_0)	Multifunction serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I ² C (operation mode 4).	-	-	-	13
	SCK7_1 (SCL7_1)		21	43	H6	48

MB9A100A Series

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.			
			QFP-100	LQFP-100	BGA-112	LQFP-120
Multi Function Timer 0	DTTI0X_0	Input signal controlling wave form generator outputs RTO00 to RTO05 of multi-function timer 0.	96	18	F4	23
	DTTI0X_1		47	69	E9	79
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin.	91	13	F1	18
	FRCK0_1		48	70	D11	80
	IC00_0	16-bit input capture ch.0 input pin of multi-function timer 0. ICxx describes channel number.	95	17	G2	22
	IC00_1		43	65	F9	75
	IC01_0		94	16	G1	21
	IC01_1		44	66	E11	76
	IC02_0		93	15	F3	20
	IC02_1		45	67	E10	77
	IC03_0		92	14	F2	19
	IC03_1		46	68	F8	78
	RTO00_0 (PPG00_0)	Wave form generator output of multi-function timer 0.	97	19	G3	24
	RTO00_1 (PPG00_1)	This pin operates as PPG00 when it is used in PPG 0 output modes.	49	71	D10	86
	RTO01_0 (PPG00_0)	Wave form generator output of multi-function timer 0.	98	20	H1	25
	RTO01_1 (PPG00_1)	This pin operates as PPG00 when it is used in PPG 0 output modes.	-	-	-	85
	RTO02_0 (PPG02_0)	Wave form generator output of multi-function timer 0.	99	21	H2	26
	RTO02_1 (PPG02_1)	This pin operates as PPG02 when it is used in PPG 0 output modes.	-	-	-	84
	RTO03_0 (PPG02_0)	Wave form generator output of multi-function timer 0.	100	22	G4	27
	RTO03_1 (PPG02_1)	This pin operates as PPG02 when it is used in PPG 0 output modes.	-	-	-	83
	RTO04_0 (PPG04_0)	Wave form generator output of multi-function timer 0.	1	23	H3	28
	RTO04_1 (PPG04_1)	This pin operates as PPG04 when it is used in PPG 0 output modes.	-	-	-	82
	RTO05_0 (PPG04_0)	Wave form generator output of multi-function timer 0.	2	24	J2	29
	RTO05_1 (PPG04_1)	This pin operates as PPG04 when it is used in PPG 0 output modes.	-	-	-	81

MB9A100A Series

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Module	Pin name	Function	Pin No.			
			QFP-100	LQFP-100	BGA-112	LQFP-120
Multi Function Timer 1	DTT1X_0	Input signal controlling wave form generator outputs RTO10 to RTO15 of multi-function timer 1.	86	8	D5	8
	DTT1X_1		17	39	K6	44
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin.	65	87	D7	102
	FRCK1_1		22	44	J7	49
	IC10_0	16-bit input capture ch.0 input pin of multi-function timer 1. ICxx describes channel number.	66	88	A6	103
	IC10_1		18	40	J6	45
	IC11_0		67	89	B6	104
	IC11_1		19	41	L7	46
	IC12_0		68	90	C6	105
	IC12_1		20	42	K7	47
	IC13_0		69	91	A5	106
	IC13_1		21	43	H6	48
	RTO10_0 (PPG10_0)	Wave form generator output of multi-function timer 1.	80	2	C1	2
	RTO10_1 (PPG10_1)	This pin operates as PPG10 when it is used in PPG 1 output modes.	5	27	J4	32
	RTO11_0 (PPG10_0)	Wave form generator output of multi-function timer 1.	81	3	C2	3
	RTO11_1 (PPG10_1)	This pin operates as PPG10 when it is used in PPG 1 output modes.	6	28	L5	33
	RTO12_0 (PPG12_0)	Wave form generator output of multi-function timer 1.	82	4	B3	4
	RTO12_1 (PPG12_1)	This pin operates as PPG12 when it is used in PPG 1 output modes.	7	29	K5	34
	RTO13_0 (PPG12_0)	Wave form generator output of multi-function timer 1.	83	5	D1	5
	RTO13_1 (PPG12_1)	This pin operates as PPG12 when it is used in PPG 1 output modes.	8	30	J5	35
	RTO14_0 (PPG14_0)	Wave form generator output of multi-function timer 1.	84	6	D2	6
	RTO14_1 (PPG14_1)	This pin operates as PPG14 when it is used in PPG 1 output modes.	9	31	H5	36
	RTO15_0 (PPG14_0)	Wave form generator output of multi-function timer 1.	85	7	D3	7
	RTO15_1 (PPG14_1)	This pin operates as PPG14 when it is used in PPG 1 output modes.	10	32	L6	37

MB9A100A Series

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

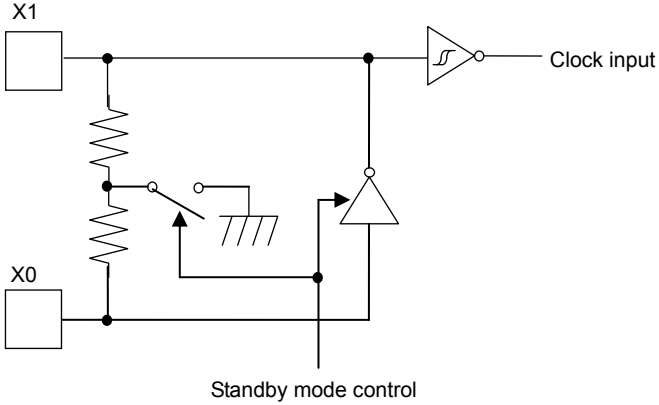
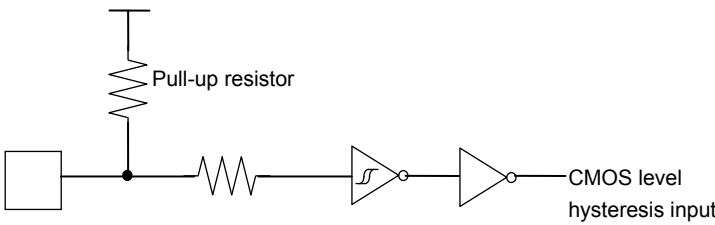
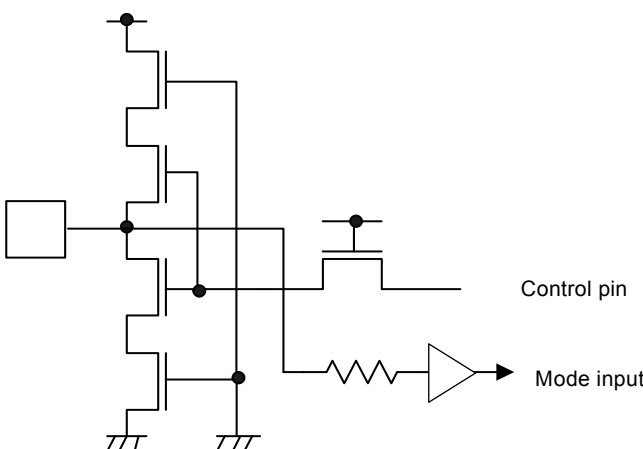
Module	Pin name	Function	Pin No.			
			QFP-100	LQFP-100	BGA-112	LQFP-120
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin.	87	9	E1	14
	AIN0_1		18	40	J6	45
	AIN0_2		80	2	C1	2
	BIN0_0	QPRC ch.0 BIN input pin.	88	10	E2	15
	BIN0_1		19	41	L7	46
	BIN0_2		81	3	C2	3
	ZIN0_0	QPRC ch.0 ZIN input pin.	89	11	E3	16
	ZIN0_1		20	42	K7	47
	ZIN0_2		82	4	B3	4
Quadrature Position/ Revolution Counter 1	AIN1_1	QPRC ch.1 AIN input pin.	52	74	C10	89
	AIN1_2		21	43	H6	48
	BIN1_1	QPRC ch.1 BIN input pin.	51	73	C11	88
	BIN1_2		22	44	J7	49
	ZIN1_1	QPRC ch.1 ZIN input pin.	50	72	E8	87
	ZIN1_2		23	45	K8	50

MB9A100A Series

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

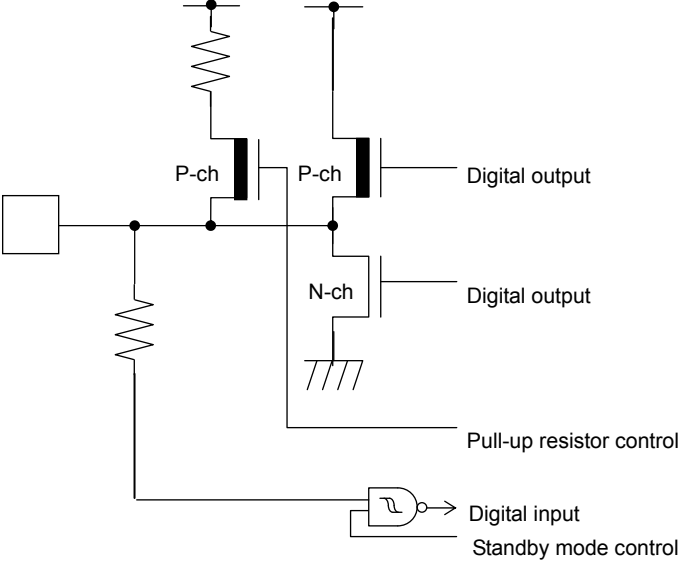
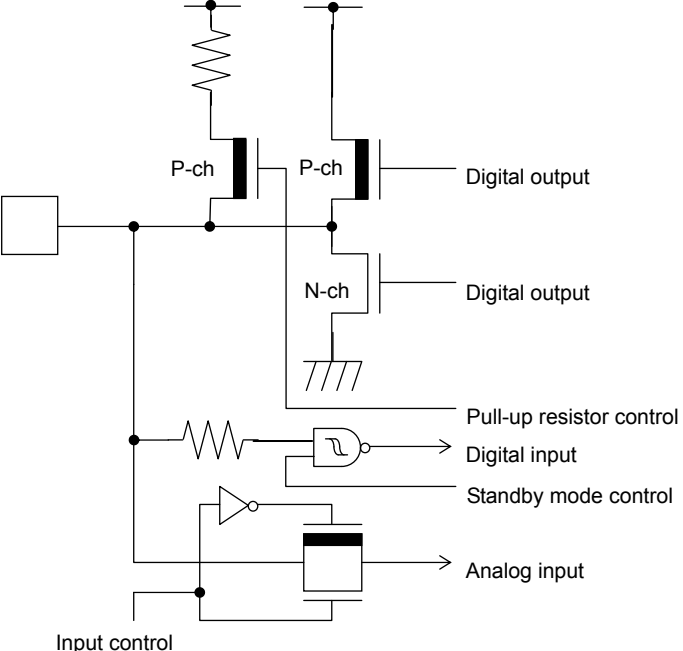
Module	Pin name	Function	Pin No.			
			QFP-100	LQFP-100	BGA-112	LQFP-120
RESET	INITX	External Reset Input. A reset is valid when INITX=L.	16	38	K4	43
Mode	MD0	Mode 0 pin. During normal operation, MD0=L must be input. During serial programming to flash memory, MD0=H must be input.	25	47	L8	57
	MD1	Mode 1 pin. Input must always be at the "L" level.	24	46	K9	56
POWER	VCC	Power Pin.	79	1	B1	1
	VCC	Power Pin.	4	26	J1	31
	VCC	Power pin.	13	35	K1	40
	VCC	Power pin.	29	51	K11	61
	VCC	Power pin.	54	76	A10	91
	VCC	Power pin.	75	97	A4	117
GND	VSS	GND Pin.	-	-	B2	-
	VSS	GND pin.	3	25	L1	30
	VSS	GND pin.	-	-	K2	-
	VSS	GND pin.	-	-	J3	-
	VSS	GND pin.	-	-	H4	-
	VSS	GND pin.	12	34	L4	39
	VSS	GND pin.	28	50	L11	60
	VSS	GND pin.	-	-	K10	-
	VSS	GND pin.	-	-	J9	-
	VSS	GND pin.	-	-	H8	-
	VSS	GND pin.	-	-	B10	-
	VSS	GND pin.	-	-	C9	-
	VSS	GND pin.	53	75	A11	90
	VSS	GND pin.	-	-	D8	-
	VSS	GND pin.	-	-	D4	-
	VSS	GND pin.	-	-	C3	-
	VSS	GND pin.	78	100	A1	120
CLOCK	X0	Main clock (oscillation) input pin.	26	48	L9	58
	X0A	Sub clock (oscillation) input pin.	14	36	L3	41
	X1	Main clock (oscillation) I/O pin.	27	49	L10	59
	X1A	Sub clock (oscillation) I/O pin.	15	37	K3	42
	CROUT	Internal CR-osc clock output port.	52	74	C10	89
ADC POWER	AVCC	A/D converter analog power pin.	38	60	H11	70
	AVRH	A/D converter analog reference voltage input pin.	39	61	F11	71
ADC GND	AVSS	A/D converter GND pin.	40	62	G11	72
C-pin	C	Power stabilization capacity pin.	11	33	L2	38

I/O CIRCUIT TYPE

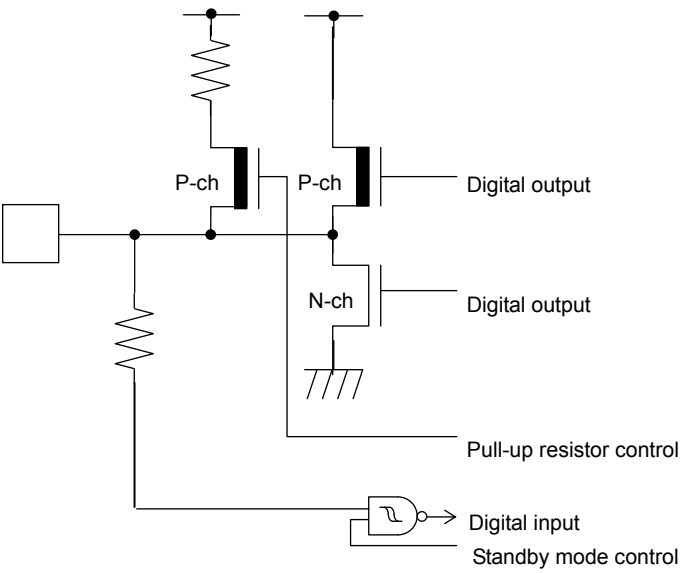
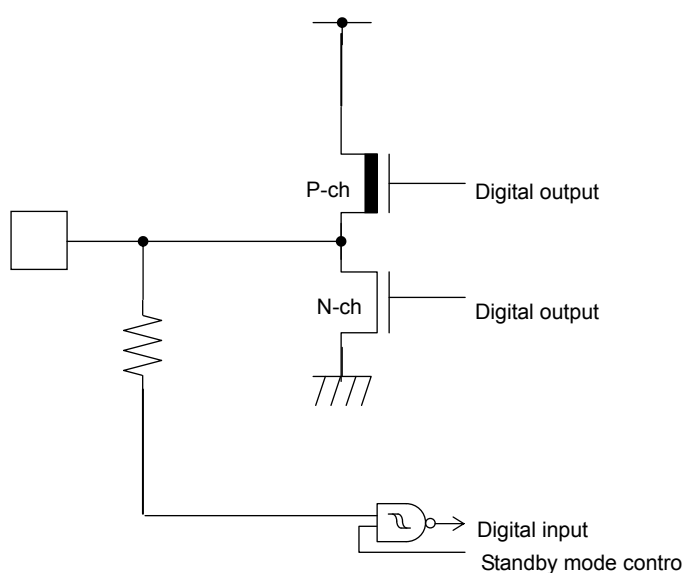
Type	Circuit	Remarks
A	 Clock input Standby mode control	• Oscillation feedback resistor : Approximately 1MΩ • With Standby mode control
B	 Pull-up resistor CMOS level hysteresis input	• CMOS level hysteresis input • pull-up resistor : Approximately 50kΩ
C	 Control pin Mode input	• CMOS level input

MB9A100A Series

Type	Circuit	Remarks
D	The diagram illustrates the internal circuitry for two channels, X1A and X0A, of the MB9A100A Series. Each channel consists of a pull-up resistor (R) connected to a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET's gate is connected to a digital input, and its source is connected to a pull-up resistor control signal. The N-ch MOSFET's gate is connected to a standby mode control signal, and its source is connected to ground. The X1A section also includes a clock input and a digital input. The X0A section includes a digital input and a standby mode control signal. The circuit is designed to support both low-speed oscillation and GPIO functions.	• It is possible to select the low speed oscillation / GPIO function. When the low speed oscillation is selected. • Oscillation feedback resistor : Approximately 20MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • pull-up resistor : Approximately 50kΩ • $I_{OH}=-4mA$, $I_{OL}=4mA$

Type	Circuit	Remarks
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • pull-up resistor : Approximately 50kΩ • $I_{OH}=4mA$, $I_{OL}=4mA$
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • pull-up resistor : Approximately 50kΩ • $I_{OH}=4mA$, $I_{OL}=4mA$

MB9A100A Series

Type	Circuit	Remarks
G		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • pull-up resistor : Approximately 50kΩ • I_{OH}=12mA, I_{OL}=12mA
H		• CMOS level output • CMOS level hysteresis input • With standby mode control • I_{OH}=25.3mA, I_{OL}=19.7mA

■ HANDLING PRECAUTIONS

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU SEMICONDUCTOR semiconductor devices.

1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- **Absolute Maximum Ratings**

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- **Recommended Operating Conditions**

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- **Processing and Protection of Pins**

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

- (1) **Preventing Over-Voltage and Over-Current Conditions**

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

- (2) **Protection of Output Pins**

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

- (3) **Handling of Unused Input Pins**

Unconnected input pins with very high impedance levels can adversely affect stability of operation.

Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- **Latch-up**

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

- (2) Be sure that abnormal current flows do not occur during the power-on sequence.

- **Observance of Safety Regulations and Standards**

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

- **Fail-Safe Design**

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

- **Precautions Related to Usage of Devices**

FUJITSU SEMICONDUCTOR semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under FUJITSU SEMICONDUCTOR's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- **Lead Insertion Type**

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to FUJITSU SEMICONDUCTOR recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- **Surface Mount Type**

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. FUJITSU SEMICONDUCTOR recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with FUJITSU SEMICONDUCTOR ranking of recommended conditions.

- **Lead-Free Packaging**

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- **Storage of Semiconductor Devices**

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- (3) When necessary, FUJITSU SEMICONDUCTOR packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- **Baking**

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU SEMICONDUCTOR recommended conditions for baking.

Condition: 125°C/24 h

- **Static Electricity**

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of FUJITSU SEMICONDUCTOR products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.

<http://edevic.fujitsu.com/fj/handling-e.pdf>

■ HANDLING DEVICES

● Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with the VCC and VSS pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 μF be connected as a bypass capacitor between VCC and VSS near this device.

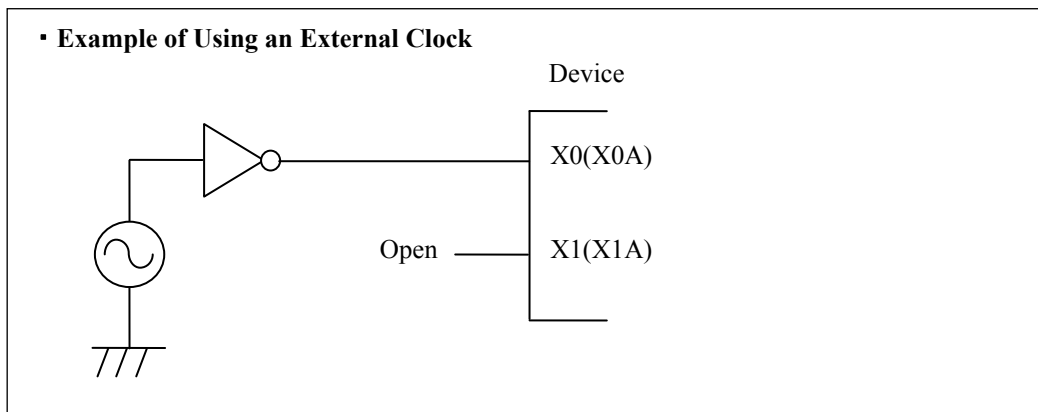
● Crystal oscillator circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

● Using an external clock

When using an external clock, the clock signal should be input to the X0,X0A pin only and the X1,X1A pin should be kept open.



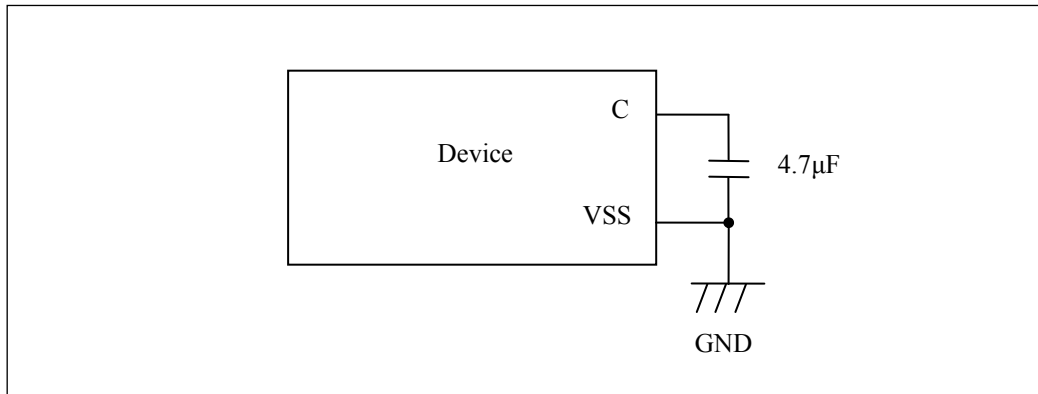
● Handling when using Multi function serial pin as I²C pin

If it is using multi function serial pin as I²C pins, P-ch transistor of digital output is always disable. However, I²C pins need to keep the electrical characteristic like other pins and not to connect to external I²C bus system with power OFF.

MB9A100A Series

● C Pin

As this series includes an internal regulator, always connect a bypass capacitor of approximately 4.7 μF to the C pin for use by the regulator.



● Mode pins (MD0, MD1)

Connect the MD pin (MD0, MD1) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

● Notes on power-on

Turn power on/off in the following order or at the same time.

If not using the A/D converter, connect AVCC = VCC and AVSS = VSS.

Turning on : VCC $\rightarrow$ AVCC $\rightarrow$ AVRH

Turning off : AVRH $\rightarrow$ AVCC $\rightarrow$ VCC

● Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise.

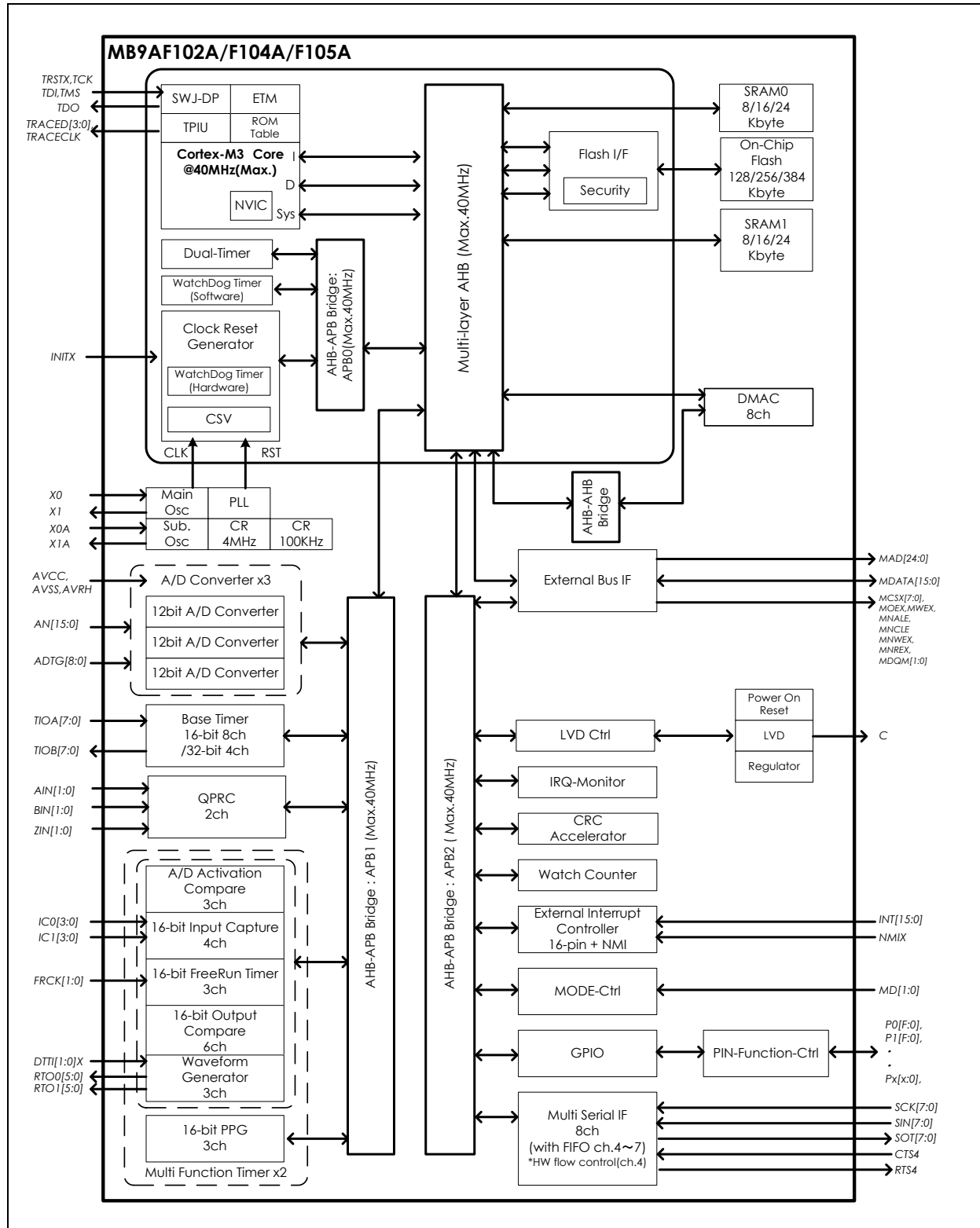
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

● Differences in features among the products with different memory sizes and between FLASH products and MASK products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between FLASH products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

■ BLOCK DIAGRAM

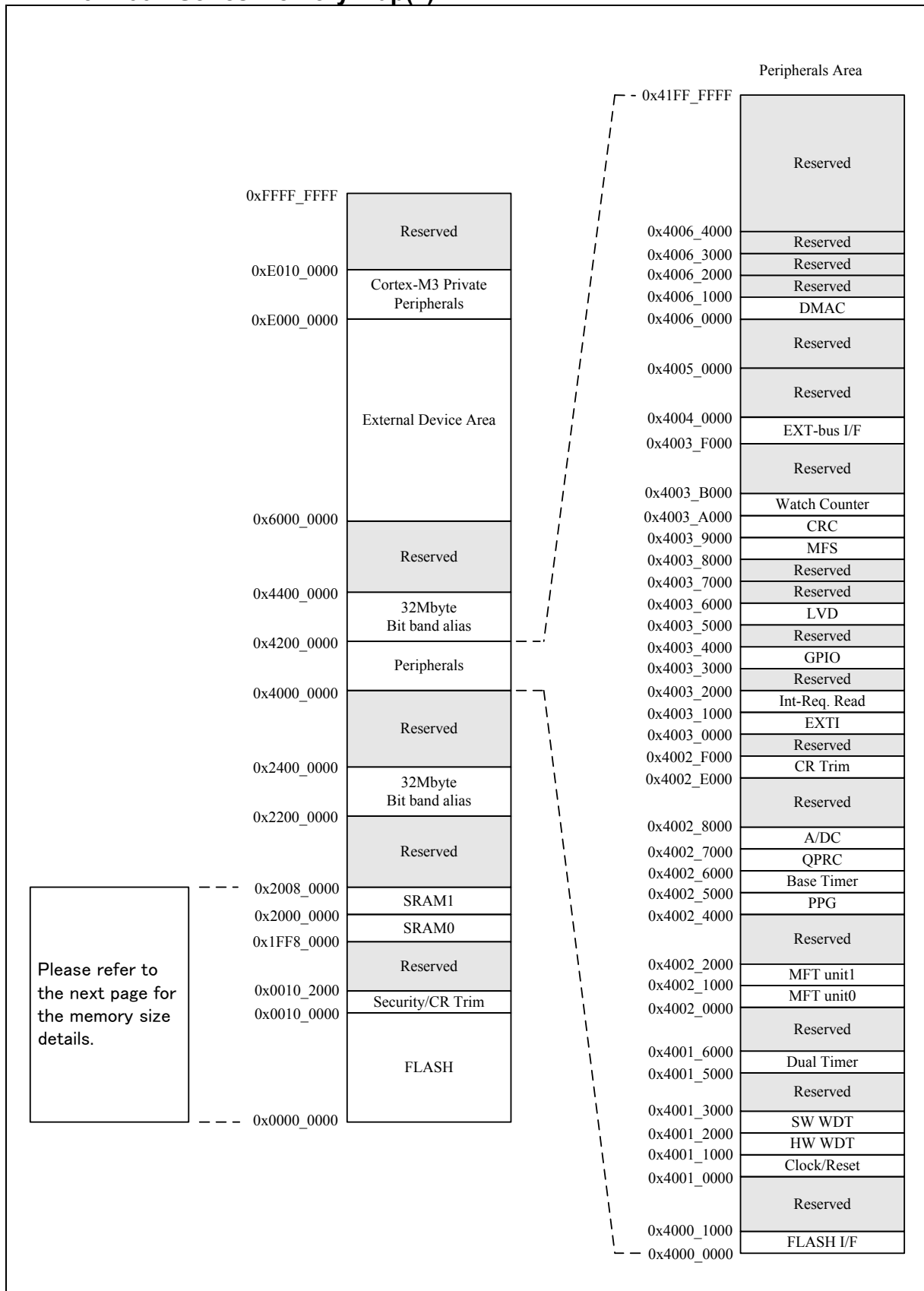


Product device	MB9AF102A	MB9AF104A	MB9AF105A
On-Chip Flash	128Kbyte	256Kbyte	384Kbyte
SRAM0	8Kbyte	16Kbyte	24Kbyte
SRAM1	8Kbyte	16Kbyte	24Kbyte

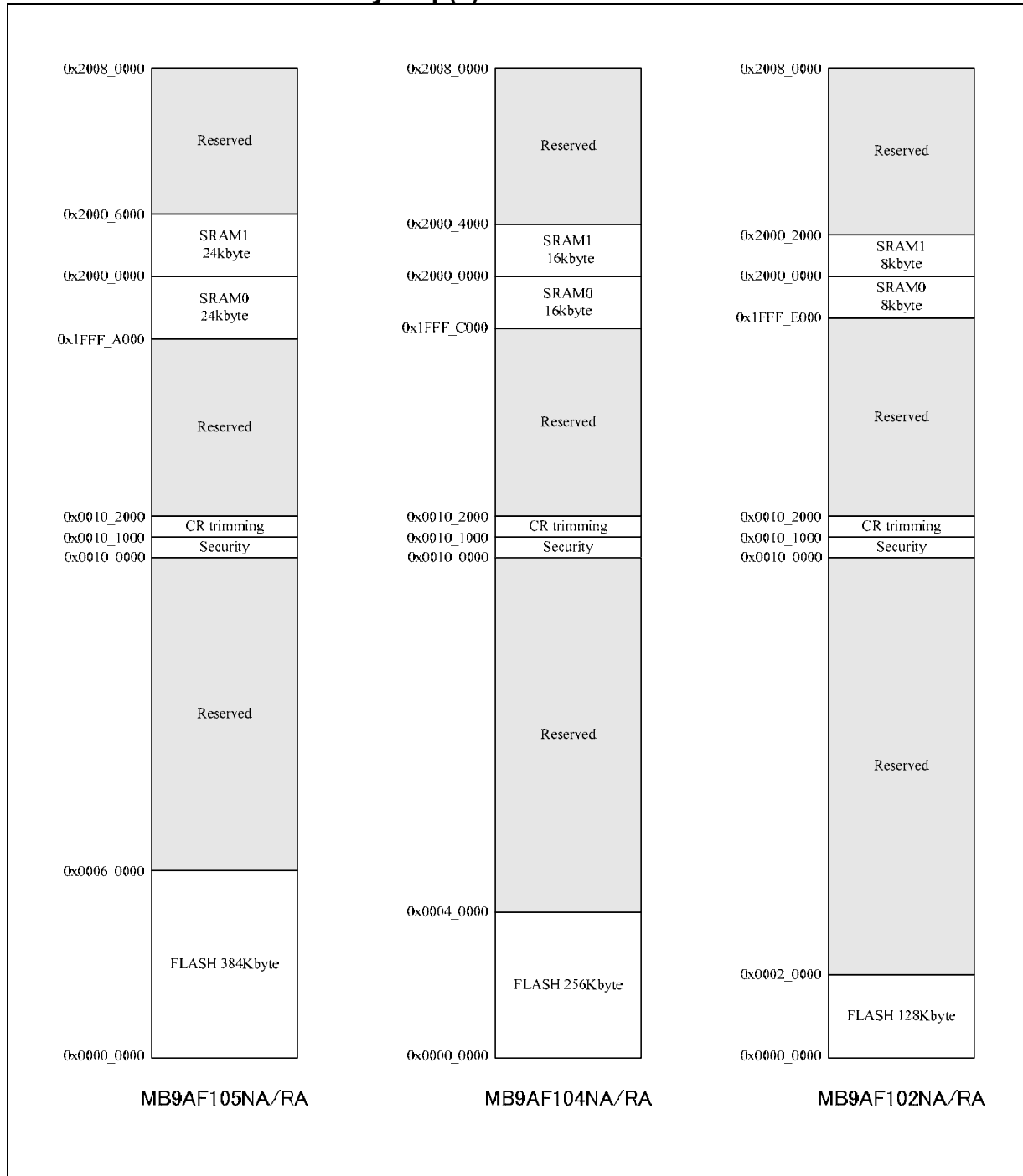
MB9A100A Series

■ MEMORY MAP

● MB9A100A Series Memory Map(1)



● MB9A100A Series Memory Map(2)



MB9A100A Series

● Peripheral Address Map

Start address	End address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	Flash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Multi-function timer unit1
0x4002_2000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		GPIO
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_5FFF		Low Voltage Detector
0x4003_6000	0x4003_6FFF		Reserved
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External Memory interface
0x4004_0000	0x4004_FFFF	AHB	Reserved
0x4005_0000	0x4005_FFFF		Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		Reserved
0x4006_2000	0x4006_2FFF		Reserved
0x4006_3000	0x4006_3FFF		Reserved
0x4006_4000	0x41FF_FFFF		Reserved

■ PIN STATUS IN EACH CPU STATE

The terms used for pin status have the following meanings.

- INITX=0
This is the period when the INITX pin is the "L" level.
- INITX=1
This is the period when the INITX pin is the "H" level.
- SPL=0
This is the status that standby pin level setting bit (SPL) in standby mode control register (STB_CTL) is set to "0".
- SPL=1
This is the status that standby pin level setting bit (SPL) in standby mode control register (STB_CTL) is set to "1".
- Input enabled
Indicates that the input function can be used.
- Internal input fixed at "0"
This is the status that the input function cannot be used. Internal input is fixed at "L".
- Hi-Z
Indicates that the output drive transistor is disabled and the pin is put in the Hi-Z state.
- Setting disabled
Indicates that the setting is disabled.
- Maintain previous state
Maintains the state that was immediately prior to entering the current mode.
If a built-in peripheral function is operating, the output follows the peripheral function.
If the pin is being used as a port, that output is maintained.
- Analog input is enabled
Indicates that the analog input is enabled.
- Trace output
Indicates that the trace function can be used.

MB9A100A Series

● LIST OF PIN STATUS

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
A	Main crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	Main crystal oscillator output pin	H output/ Internal input fixed at "0"/ or Input enabled	H output/ Internal input fixed at "0"	H output/ Internal input fixed at "0"	Maintain previous state/ H output at oscillation stop (*1)/ Internal input fixed at "0"	Maintain previous state/ H output at oscillation stop (*1)/ Internal input fixed at "0"	Maintain previous state/ H output at oscillation stop (*1)/ Internal input fixed at "0"
C	INITX input pin	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	JTAG selected	Hi-Z	Pull-up/ Input enabled	Pull-up/ Input enabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Output Hi-Z/ Internal input fixed at "0"
F	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	External interrupt enabled selected						Maintain previous state
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"

MB9A100A Series

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
G	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
H	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"
I	GPIO selected, resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
J	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected, or other than above resource selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled			Hi-Z/ Internal input fixed at "0"

MB9A100A Series

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
K	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or other than above resource selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
L	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state
	Analog input selected	Hi-Z	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled	Hi-Z/ Internal input fixed at "0"/ Analog input enabled
	GPIO selected, or other than above resource selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ Internal input fixed at "0"
M	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

MB9A100A Series

Pin status type	Function group	Power-on reset or low voltage detection state	INITX input state	Device internal reset state	Run mode or sleep mode state	Timer mode or sleep mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1	
		-	-	-	-	SPL=0	SPL=1
N	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"
	Sub crystal oscillator output pin	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Hi-Z/ Internal input fixed at "0"	Maintain previous state	Maintain previous state/ Hi-Z at oscillation stop (*2)/ Internal input fixed at "0"	Maintain previous state/ Hi-Z at oscillation stop (*2)/ Internal input fixed at "0"
O	GPIO selected	Hi-Z	Hi-Z/ Input enabled	Hi-Z/ Input enabled	Maintain previous state	Maintain previous state	Output Hi-Z/ Internal input fixed at "0"

*1 : Oscillation is stopped at sub timer mode, Low speed CR timer mode, and stop mode.

*2 : Oscillation is stopped at stop mode.

MB9A100A Series

■ ELECTRICAL CHARACTERISTICS

This section describes the electrical characteristics of MB9A100A series.

● Absolute Maximum Ratings / Recommended Operating Conditions

The following tables show the absolute maximum ratings and recommended operating conditions.

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1,*2	V _{CC}	V _{SS} - 0.5	V _{SS} + 6.5	V	
Analog power supply voltage*1,*3	AV _{CC}	V _{SS} - 0.5	V _{SS} + 6.5	V	
Analog reference voltage*1,*3	AV _{RH}	V _{SS} - 0.5	V _{SS} + 6.5	V	
Input voltage*1	V _I	V _{SS} - 0.5	V _{CC} + 0.5 (≤ 6.5V)	V	
Analog pin input voltage*1	V _{IA}	V _{SS} - 0.5	AV _{CC} + 0.5 (≤ 6.5V)	V	
Output voltage*1	V _O	V _{SS} - 0.5	V _{CC} + 0.5 (≤ 6.5V)	V	
"L" level maximum output current*4	I _{OL}	-	10	mA	4mA type
			20	mA	12mA type
"L" level average output current*5	I _{OLAV}	-	4	mA	4mA type
			12	mA	12mA type
"L" level total maximum output current	∑I _{OL}	-	100	mA	
"L" level total average output current*6	∑I _{OLAV}	-	50	mA	
"H" level maximum output current*4	I _{OH}	-	- 10	mA	4mA type
			- 20	mA	12mA type
"H" level average output current*5	I _{OHAV}	-	- 4	mA	4mA type
			- 12	mA	12mA type
"H" level total maximum output current	∑I _{OH}	-	- 100	mA	
"H" level total average output current*6	∑I _{OHAV}	-	- 50	mA	
Power consumption	P _D	-	480	mW	
Storage temperature	T _{STG}	- 55	+ 150	°C	

*1 : These parameters are based on the condition that V_{SS} = AV_{SS} = 0.0V.

*2 : V_{CC} must not drop below V_{SS} - 0.5V.

*3 : Be careful not to exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*4 : The maximum output current is the peak value for a single pin.

*5 : The average output is the average current for a single pin over a period of 100 ms.

*6 : The total average output current is the average current for all pins over a period of 100 ms.

<WARNING>

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0V)

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		Vcc	-	2.7	5.5	V	
Analog power supply voltage		AVcc	-	2.7	5.5	V	AVcc = Vcc
Analog reference voltage		AVRH	-	AVss	AVcc	V	
Operating Temperature	FPT-120P-M21 FPT-120P-M37 FPT-100P-M20 FPT-100P-M23 BGA-112P-M04	Ta	-	- 40	+ 85	°C	
	FPT-100P-M06		When mounted on four-layer PCB	- 40	+ 85	°C	
			When mounted on double-sided single-layer PCB	- 40	+ 85		Icc ≤ 74mA
				- 40	+ 70		Icc > 74mA

<WARNING>

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

MB9A100A Series

● DC Characteristics

The following tables show the DC characteristics.

1. Current rating

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	Icc	Vcc	Normal operation (PLL)	-	60	74	mA	CPU : 40MHz, Peripheral : 40MHz, FLASH 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *1
				-	44	55	mA	CPU : 40MHz, Peripheral : 40MHz, FLASH 3Wait FRWTR.RWT = 00 FSYNDN.SD = 011 *1
			Normal operation (built-in high-speed CR)	-	6.0	9.2	mA	CPU/ Peripheral : 4MHz *1, *2 FLASH 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000
			Normal operation (sub oscillation)	-	0.2	2.24	mA	CPU/ Peripheral : 32kHz FLASH 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *1
			Normal operation (built-in low-speed CR)	-	0.3	2.36	mA	CPU/ Peripheral : 100kHz FLASH 0Wait FRWTR.RWT = 00 FSYNDN.SD = 000 *1
	Iccs		SLEEP operation (PLL)	-	33	42	mA	Peripheral : 40MHz *1
			SLEEP operation (built-in high-speed CR)	-	3.5	6.2	mA	Peripheral : 4MHz *1, *2
			SLEEP operation (sub oscillation)	-	0.15	2.18	mA	Peripheral : 32kHz *1
			SLEEP operation (built in low-speed CR)	-	0.22	2.27	mA	Peripheral : 100kHz *1

(Continued)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I _{CCH}	V _{CC}	STOP mode	-	50	200	μA	Ta = + 25°C, When LVD is off *1
				-	-	2	mA	Ta = + 85°C, When LVD is off *1
	Timer mode (sub oscillation)		-	110	300	μA	Ta = + 25°C, When LVD is off *1	
			-	-	2.2	mA	Ta = + 85°C, When LVD is off *1	
Low voltage detection circuit (LVD) power supply current	I _{CCLVD}		At operation	-	2	10	μA	for occurrence of interrupt

*1: When all ports are fixed.

*2: When setting it to 4MHz by trimming.

MB9A100A Series

2. Pin Characteristics

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$ $T_a = -40^{\circ}C$ to $+85^{\circ}C$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0,1	-	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	
"L" level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0,1	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
"H" level output voltage	V_{OH}	4mA type	$V_{CC} \geq 4.5 V$ $I_{OH} = -4mA$	$V_{CC} - 0.5$	-	V_{CC}	V	
			$V_{CC} < 4.5 V$ $I_{OH} = -2mA$					
		12mA type	$V_{CC} \geq 4.5 V$ $I_{OH} = -12mA$	$V_{CC} - 0.5$	-	V_{CC}	V	
			$V_{CC} < 4.5 V$ $I_{OH} = -8mA$					
		P80, P81	$V_{CC} \geq 4.5 V$ $I_{OH} = -25.3mA$	$V_{CC} - 0.4$	-	V_{CC}	V	
			$V_{CC} < 4.5 V$ $I_{OH} = -13.4mA$					
"L" level output voltage	V_{OL}	4mA type	$V_{CC} \geq 4.5 V$ $I_{OL} = 4mA$	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5 V$ $I_{OL} = 2mA$					
		12mA type	$V_{CC} \geq 4.5 V$ $I_{OL} = 12mA$	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5 V$ $I_{OL} = 8mA$					
		P80, P81	$V_{CC} \geq 4.5 V$ $I_{OL} = 19.7mA$	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5 V$ $I_{OL} = 11.9mA$					
Input leak current	I_{IL}	-	-	- 5	-	5	μA	
Pull-up resistance value	R_{PU}	Pull-up pin	$V_{CC} \geq 4.5 V$	25	50	100	k Ω	
			$V_{CC} < 4.5 V$	30	80	200		
Input capacitance	C_{IN}	Other than V_{CC} , V_{SS} , AV_{CC} , AV_{SS} , AV_{RH}	-	-	5	15	pF	

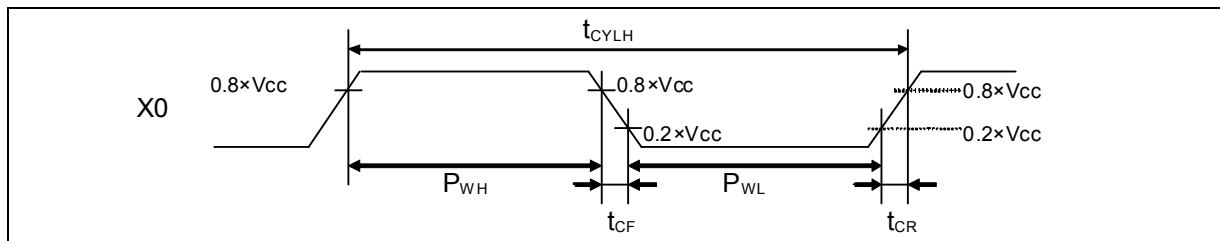
● AC Characteristics

The following tables show the AC characteristics.

(1) Main Clock Input Characteristics

(Vcc = 2.7V to 5.5V, Vss = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	F _{CH}	X0 X1	V _{CC} ≥ 4.5V	4	48	MHz	When crystal oscillator is connected
			V _{CC} < 4.5V	4	20		
			V _{CC} ≥ 4.5V	4	48	MHz	When using external clock
			V _{CC} < 4.5V	4	20		
Input clock cycle	t _{CY_{LH}}		V _{CC} ≥ 4.5V	20.83	250	ns	When using external clock
			V _{CC} < 4.5V	50	250		
Input clock pulse width	-		P _{WH} /t _{CY_{LH}} P _{WL} /t _{CY_{LH}}	45	55	%	When using external clock
Input clock rise time and fall time	t _{CF} t _{CR}		-	-	5	ns	When using external clock
Internal operating clock frequency	F _{CC}	-	-	-	40	MHz	Base clock (HCLK/FCLK)
	F _{CP0}	-	-	-	40	MHz	APB0 bus clock (PCLK0)
	F _{CP1}	-	-	-	40	MHz	APB1 bus clock (PCLK1)
	F _{CP2}	-	-	-	40	MHz	APB2 bus clock (PCLK2)
Internal operating clock cycle time	t _{CY_{CC}}	-	-	25	-	ns	Base clock (HCLK/FCLK)
	t _{CY_{CP0}}	-	-	25	-	ns	APB0 bus clock (PCLK0)
	t _{CY_{CP1}}	-	-	25	-	ns	APB1 bus clock (PCLK1)
	t _{CY_{CP2}}	-	-	25	-	ns	APB2 bus clock (PCLK2)



Note: Please see the block diagram to refer the APB bus which peripherals connected.

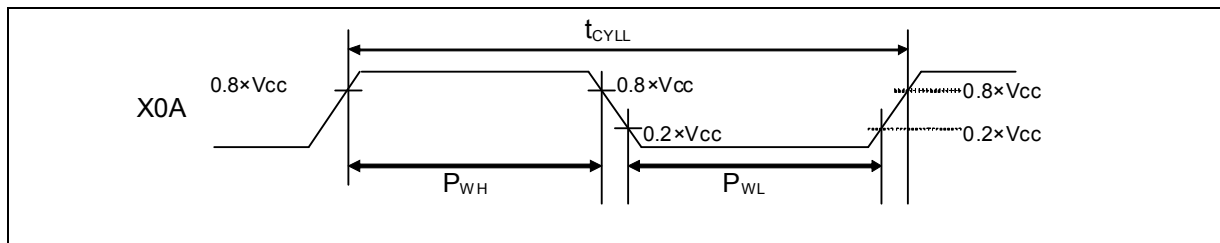
Please see the clock chapter of peripheral manual to refer the detail of internal operating clock.

MB9A100A Series

(2) Sub Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	F _{CL}	X0A X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t _{CYLL}		-	10	-	31.25	μs	When using external clock
Input clock pulse width	-		P _{WH} /t _{CYLL} P _{WL} /t _{CYLL}	45	-	55	%	When using external clock



(3) Built-in CR Oscillation Characteristics

- Built-in high-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F _{CRH}	Ta = + 25°C	3.92	4	4.08	MHz	When trimming*
		Ta = 0°C to + 70°C	3.84	4	4.16		
		Ta = - 40°C to + 85°C	3.8	4	4.2		
		Ta = - 40°C to + 85°C	3	4	5		When not trimming

*: In the case of using the values in CR trimming area of FLASH memory at shipment for frequency trimming.

- Built-in low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	F _{CRL}	-	50	100	150	kHz	

(4-1) Operating Conditions of Main PLL(In the case of using main clock for input of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)*	t _{LOCK}	100	-	-	μs	
PLL input clock frequency	f _{PLL}	4	-	30	MHz	
PLL multiple rate	-	4	-	30	multiple	
PLL macro oscillation clock frequency	f _{PLLO}	60	-	120	MHz	

*: Time from when the PLL starts operating until the oscillation stabilizes.

(4-2) Operating Conditions of Main PLL(In the case of using built-in high speed CR)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)*	t _{LOCK}	100	-	-	μs	
PLL input clock frequency	f _{PLL}	3.8	4	4.2	MHz	
PLL multiple rate	-	15	-	28	multiple	
PLL macro oscillation clock frequency	f _{PLLO}	57	-	120	MHz	

*: Time from when the PLL starts operating until the oscillation stabilizes.

Note:It needs to input to PLL after trimming.

(5) Reset Input Characteristics

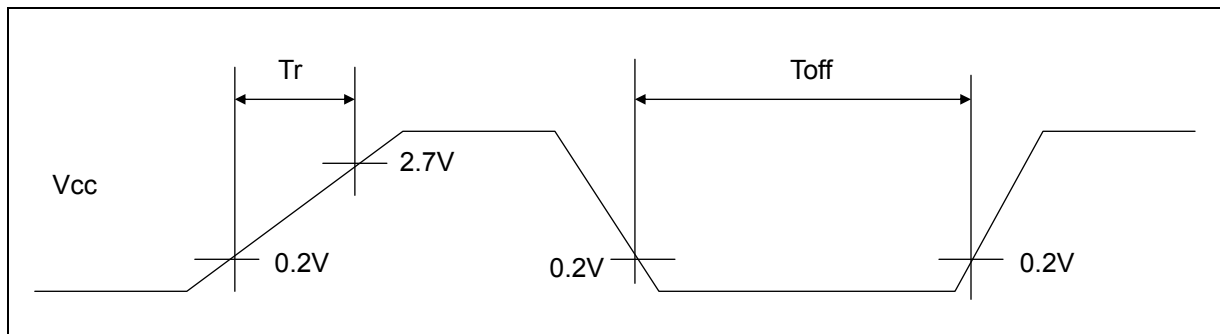
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t _{INITX}	INITX	-	500	-	ns	

(6) Power-on Reset Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	Tr	V _{CC}	0	-	ms	
Power supply shut down time	Toff		1	-	ms	



MB9A100A Series

(7) External Bus Timing

• Asynchronous SRAM Mode

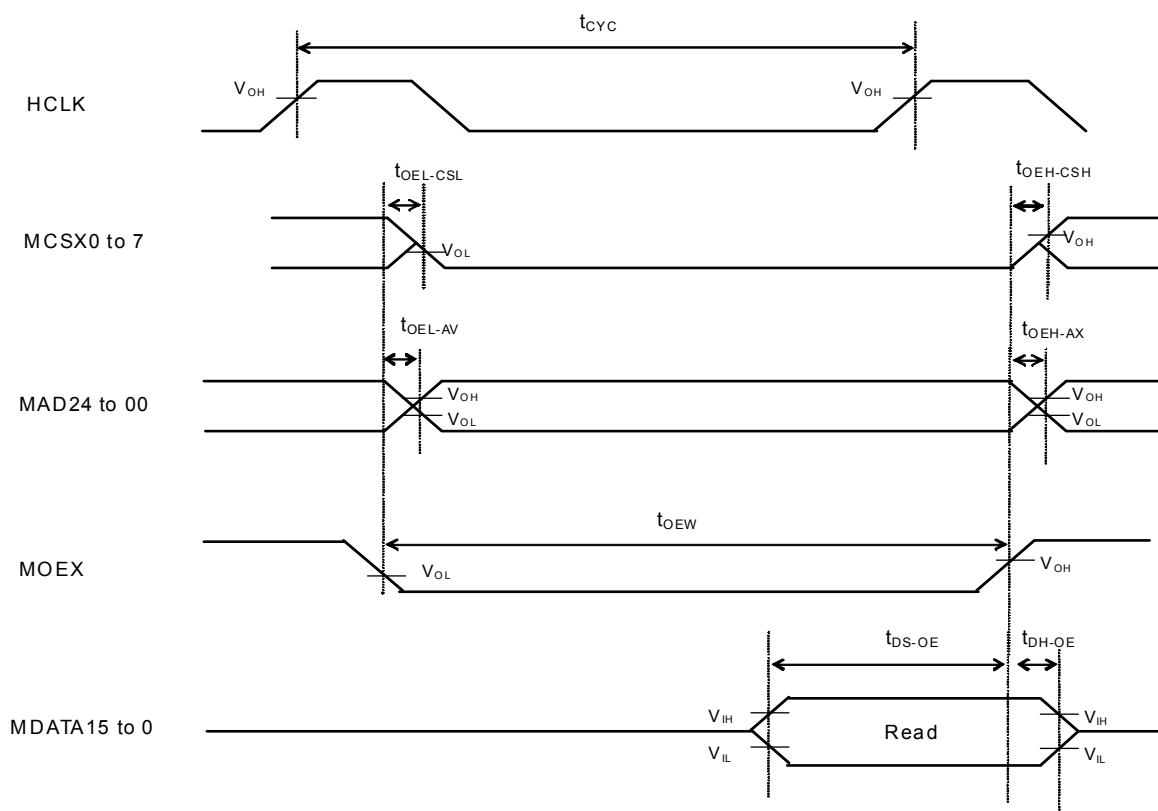
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MOEX Min pulse width	t _{OEW}	MOEX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} × 1 - 3	-	ns	
MOEX ↓ ⇒ Address delay time	t _{OEL - AV}	MOEX MAD24 to 00	V _{CC} ≥ 4.5V V _{CC} < 4.5V	0 0	10 20	ns	
MOEX ↑ ⇒ Address delay time	t _{OEH - AX}	MOEX MAD24 to 00	V _{CC} ≥ 4.5V V _{CC} < 4.5V	0 0	10 20	ns	
MOEX ↓ ⇒ MCSX ↓ delay time	t _{OEL - CSL}	MOEX MCSX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	0	10	ns	
MOEX ↑ ⇒ MCSX ↑ delay time	t _{OEH - CSH}	MOEX MCSX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	0	10	ns	
Data set up ⇒ MOEX ↑ time	t _{DS - OE}	MOEX MDATA15 to 0	V _{CC} ≥ 4.5V V _{CC} < 4.5V	20 38	- -	ns	
MOEX ↑ ⇒ Data hold time	t _{DH - OE}	MOEX MDATA15 to 0	V _{CC} ≥ 4.5V V _{CC} < 4.5V	0	-	ns	
MCSX ↓ ⇒ MWEX ↓ delay time	t _{CSL - WEL}	MCSX MWEX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} × 1 - 5 T _{HCLK} × 1 - 10	- -	ns	
MWEX ↑ ⇒ MCSX ↑ delay time	t _{WEH - CSH}	MCSX MWEX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} × 1 - 5 T _{HCLK} × 1 - 10	- -	ns	
Address ⇒ MWEX ↓ delay time	t _{AV - WEL}	MWEX MAD24 to 00	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} × 1 - 5 T _{HCLK} × 1 - 15	- -	ns	
MWEX ↑ ⇒ Address delay time	t _{WEH - AX}	MWEX MAD24 to 00	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} × 1 - 5 T _{HCLK} × 1 - 15	- -	ns	
MWEX ↓ ⇒ MDQM ↓ delay time	t _{WEL - DQML}	MWEX MDQM0 to 1	V _{CC} ≥ 4.5V V _{CC} < 4.5V	0 0	5 10	ns	
MWEX ↑ ⇒ MDQM ↑ delay time	t _{WEH - DQMH}	MWEX MDQM0 to 1	V _{CC} ≥ 4.5V V _{CC} < 4.5V	0 0	5 10	ns	
MWEX Min pulse width	t _{WEW}	MWEX	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} × 1 - 3	-	ns	
MWEX ↓ ⇒ Data delay time	t _{WEL - DV}	MWEX MDATA15 to 0	V _{CC} ≥ 4.5V V _{CC} < 4.5V	- 5 -15	5 15	ns	
MWEX ↑ ⇒ Data delay time	t _{WEH - DX}	MWEX MDATA15 to 0	V _{CC} ≥ 4.5V V _{CC} < 4.5V	T _{HCLK} × 1 - 5 T _{HCLK} × 1 - 15	- -	ns	

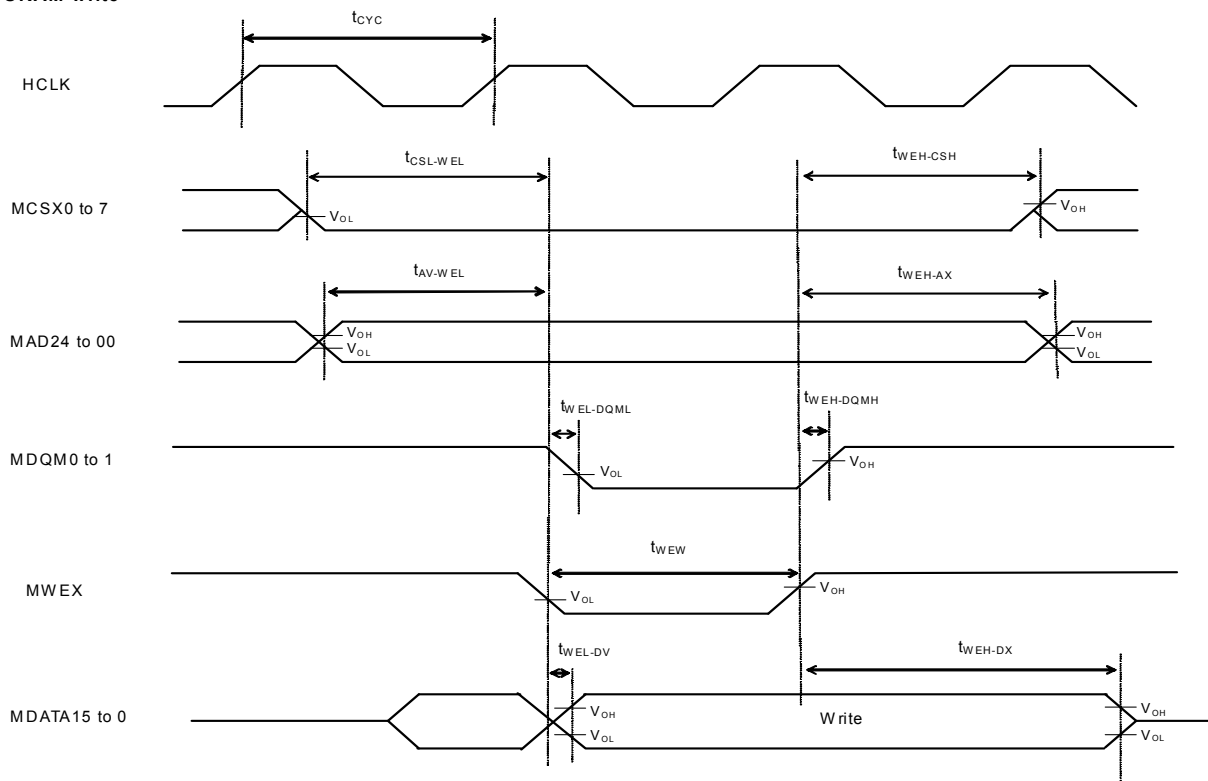
Note: When the external load capacitance = 50pF.

(Continued)

SRAM read



SRAM write



MB9A100A Series

• NAND FLASH mode

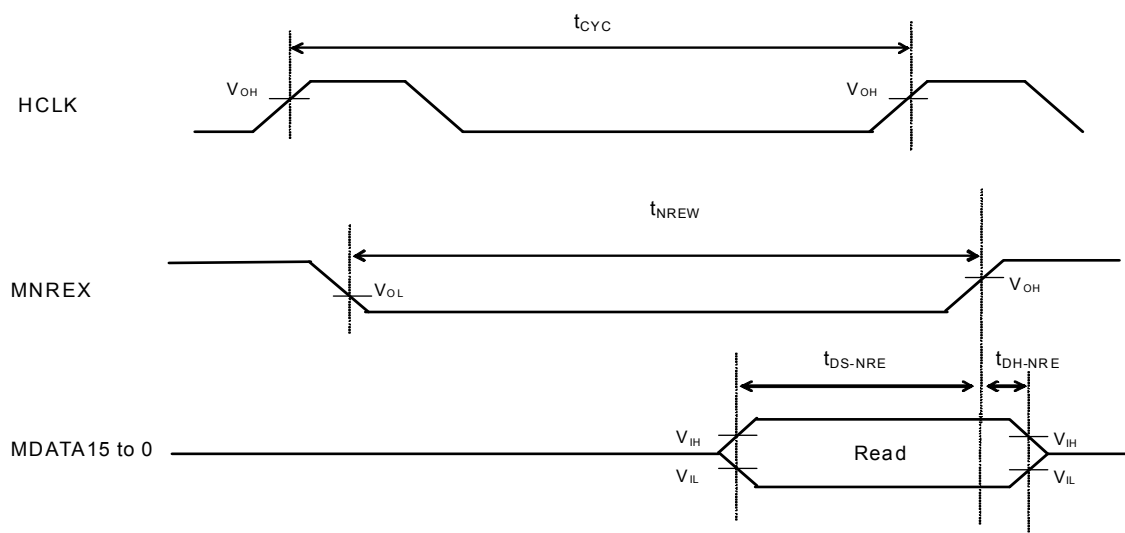
(Vcc = 2.7V to 5.5V, Vss = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
MNREX Min pulse width	t _{NREW}	MNREX	Vcc ≥ 4.5V Vcc < 4.5V	T _{HCLK} ×1 - 3	-	ns	
Data set up ⇒ MNREX ↑ time	t _{DS - NRE}	MNREX MDATA15 to 0	Vcc ≥ 4.5V Vcc < 4.5V	20 38	- -	ns	
MNREX ↑ ⇒ Data hold time	t _{DH - NRE}	MNREX MDATA15 to 0	Vcc ≥ 4.5V Vcc < 4.5V	0 0	- -	ns	
MNALE ↑ ⇒ MNWEX delay time	t _{ALEH - NWEL}	MNALE MNWEX	Vcc ≥ 4.5V Vcc < 4.5V	T _{HCLK} ×1 - 5 T _{HCLK} ×1 - 15	- -	ns	
MNWEX ↑ ⇒ MNALE delay time	t _{NWEH - ALEL}	MNALE MNWEX	Vcc ≥ 4.5V Vcc < 4.5V	T _{HCLK} ×1 - 5 T _{HCLK} ×1 - 15	- -	ns	
MNCLE ↑ ⇒ MNWEX delay time	t _{CLEH - NWEL}	MNCLE MNWEX	Vcc ≥ 4.5V Vcc < 4.5V	T _{HCLK} ×1 - 5 T _{HCLK} ×1 - 15	- -	ns	
MNWEX ↑ ⇒ MNCLE delay time	t _{NWEH - CLEL}	MNCLE MNWEX	Vcc ≥ 4.5V Vcc < 4.5V	T _{HCLK} ×1 - 5 T _{HCLK} ×1 - 15	- -	ns	
MNWEX Min pulse width	t _{NWEW}	MNWEX	Vcc ≥ 4.5V Vcc < 4.5V	T _{HCLK} ×1 - 3	-	ns	
MNWEX ↓ ⇒ Data delay time	t _{NWEL - DV}	MNWEX MDATA15 to 0	Vcc ≥ 4.5V Vcc < 4.5V	- 5 -15	+ 5 +15	ns	
MNWEX ↑ ⇒ Data delay time	t _{NWEH - DX}	MNWEX MDATA15 to 0	Vcc ≥ 4.5V Vcc < 4.5V	T _{HCLK} ×1 - 5 T _{HCLK} ×1 - 15	- -	ns	

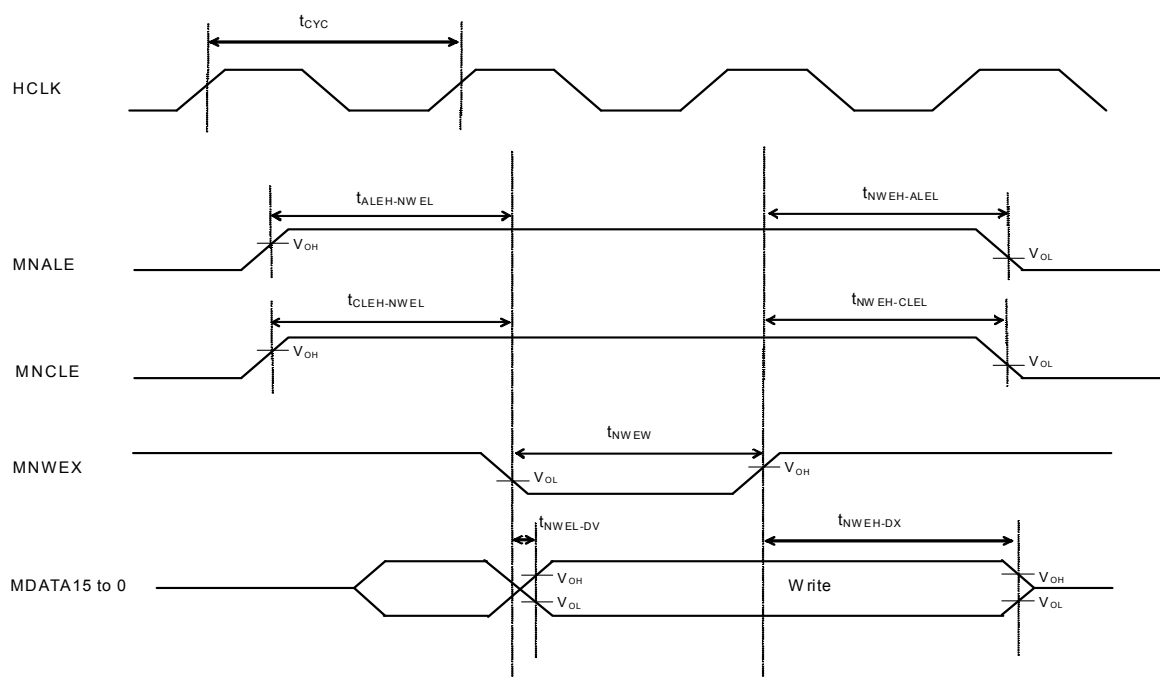
Note: when the external load capacitance = 50pF.

(Continued)

NAND FLASH read



NAND FLASH write



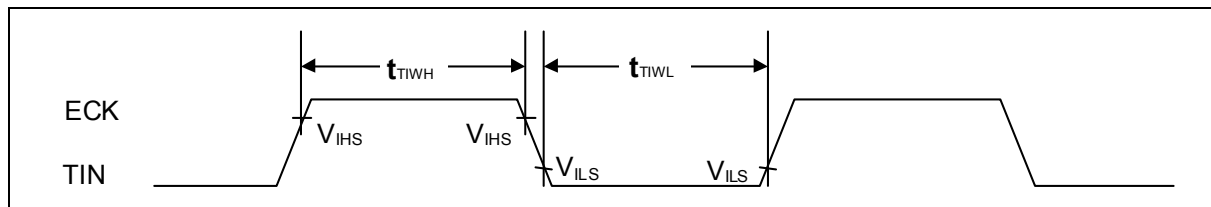
MB9A100A Series

(8) Base Timer Input Timing

• Timer input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V Ta = - 40°C to + 85°C)

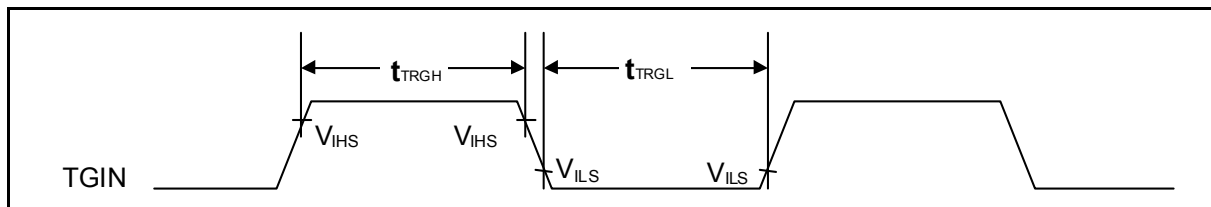
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



• Trigger input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



(9) UART Timing

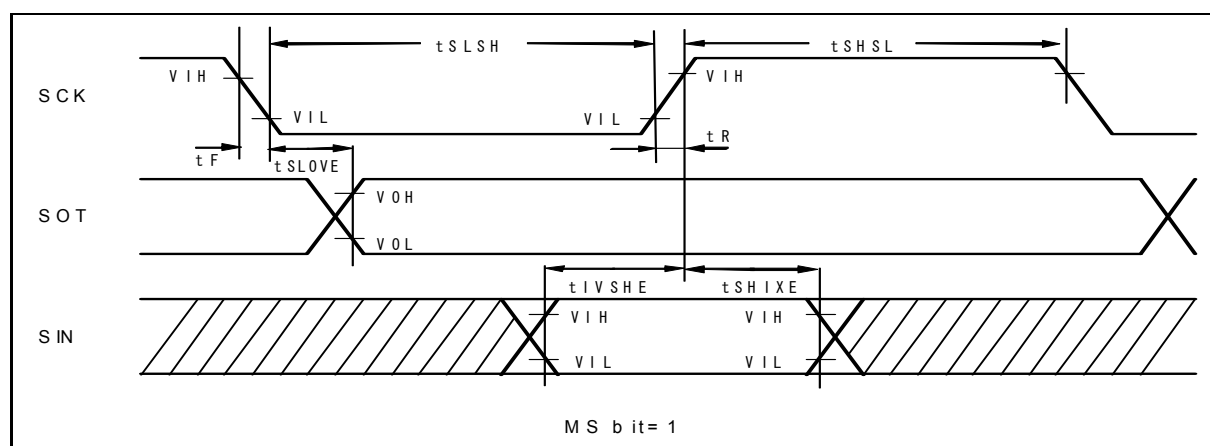
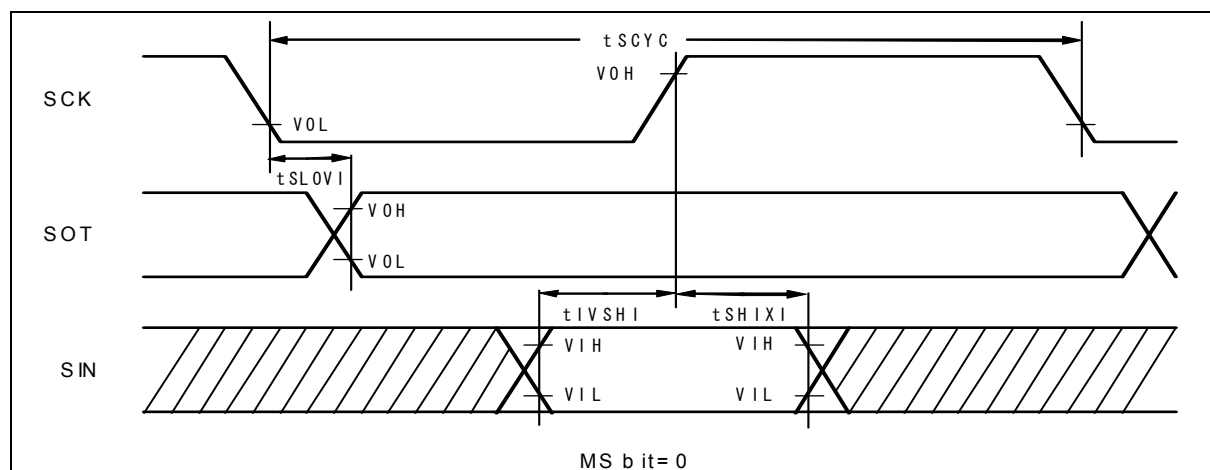
- Synchronous serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	V _{CC} < 4.5V		V _{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	tSCYC	SCK _x	Internal shift clock operation	4tcycp	-	4tcycp	-	ns
SCK ↓ → SOT delay time	tSLOVI	SCK _x SOT _x		-30	+30	- 20	+ 20	ns
SIN → SCK ↑ setup time	tIVSHI	SCK _x SIN _x		50	-	30	-	ns
SCK ↑ → SIN hold time	tSHIXI	SCK _x SIN _x		0	-	0	-	ns
Serial clock "L" pulse width	tSLSH	SCK _x	External shift clock operation	2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	tSHSL	SCK _x		tcycp + 10	-	tcycp + 10	-	ns
SCK ↓ → SOT delay time	tSLOVE	SCK _x SOT _x		-	50	-	30	ns
SIN → SCK ↑ setup time	tIVSHE	SCK _x SIN _x		10	-	10	-	ns
SCK ↑ → SIN hold time	tSHIXE	SCK _x SIN _x		20	-	20	-	ns
SCK fall time	tF	SCK _x		-	5	-	5	ns
SCK rise time	tR	SCK _x		-	5	-	5	ns

- Notes:
- The above characteristics apply to CLK synchronous mode.
 - t_{CYCP} indicates the APB bus clock cycle time. Please see the block diagram to refer the APB bus number which UART is connected.
 - These characteristics only guarantee the same relocate port number.
For example, the combination of SCLK_{x_0} and SOT_{x_1} is not guaranteed.
 - When the external load capacitance = 50pF.

MB9A100A Series



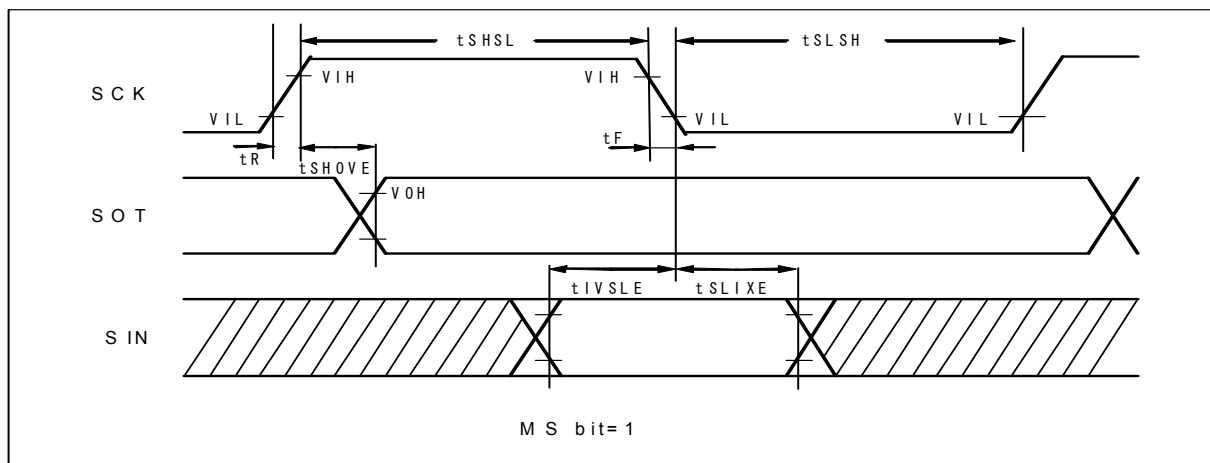
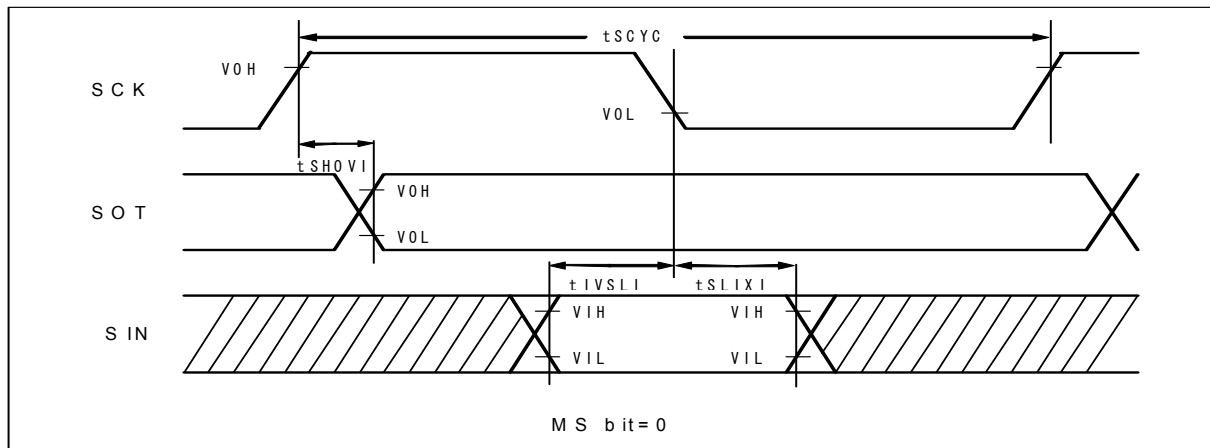
- Synchronous serial(SPI = 0, SCINV = 1)

(Vcc = 2.7V to 5.5V, Vss = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Vcc < 4.5V		Vcc ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	tSCYC	SCKx	Internal shift clock operation	4tcycp	-	4tcycp	-	ns
SCK ↑ → SOT delay time	tSHOVI	SCKx SOTx		-30	+30	- 20	+ 20	ns
SIN → SCK ↓ setup time	tIVSLI	SCKx SINx		50	-	30	-	ns
SCK ↓ → SIN hold time	tSLIXI	SCKx SINx		0	-	0	-	ns
Serial clock "L" pulse width	tSLSH	SCKx	External shift clock operation	2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	tSHSL	SCKx		tcycp + 10	-	tcycp + 10	-	ns
SCK ↑ → SOT delay time	tSHOVE	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↓ setup time	tIVSLE	SCKx SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	tSLIXE	SCKx SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

- Notes:
- The above characteristics apply to CLK synchronous mode.
 - tcycp indicates the APB bus clock cycle time. Please see the block diagram to refer the APB bus number which UART is connected.
 - These characteristics only guarantee the same relocate port number.
For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
 - When the external load capacitance = 50pF.

MB9A100A Series



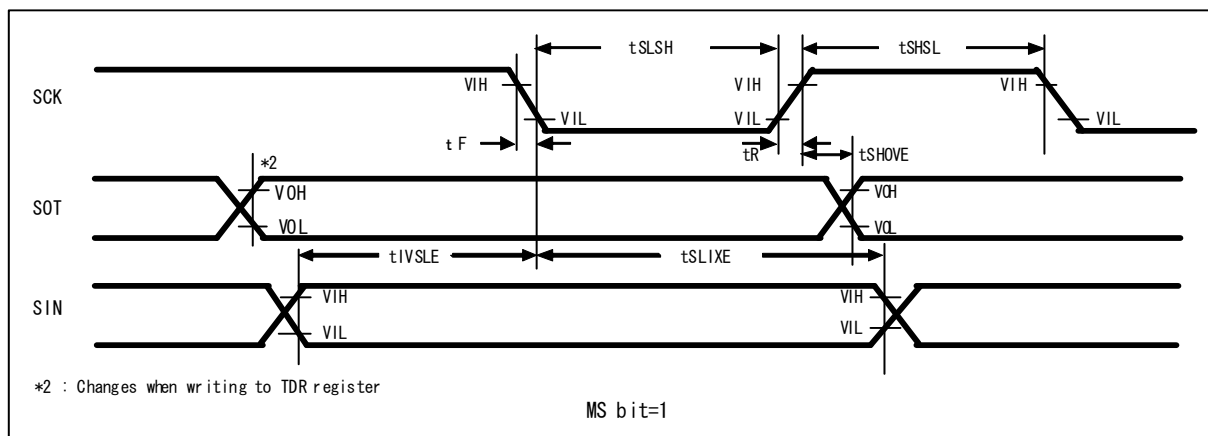
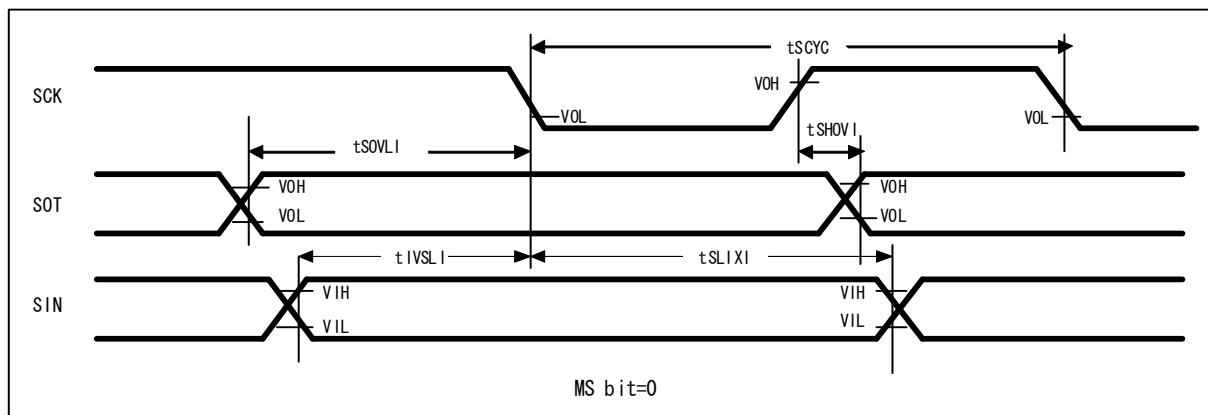
- Synchronous serial(SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	V _{CC} < 4.5V		V _{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	tSCYC	SCK _x	Internal shift clock operation	4tcycp	-	4tcycp	-	ns
SCK ↑ → SOT delay time	tSHOVI	SCK _x SOT _x		-30	+30	- 20	+ 20	ns
SIN → SCK ↓ setup time	tIVSLI	SCK _x SIN _x		50	-	30	-	ns
SCK ↓ → SIN hold time	tSLIXI	SCK _x SIN _x		0	-	0	-	ns
SOT → SCK ↓ delay time	tSOVLI	SCK _x SOT _x		2tcycp - 30	-	2tcycp - 30	-	ns
Serial clock "L" pulse width	tSLSH	SCK _x	External shift clock operation	2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	tSHSL	SCK _x		tcycp + 10	-	tcycp + 10	-	ns
SCK ↑ → SOT delay time	tSHOVE	SCK _x SOT _x		-	50	-	30	ns
SIN → SCK ↓ setup time	tIVSLE	SCK _x SIN _x		10	-	10	-	ns
SCK ↓ → SIN hold time	tSLIXE	SCK _x SIN _x		20	-	20	-	ns
SCK fall time	tF	SCK _x		-	5	-	5	ns
SCK rise time	tR	SCK _x		-	5	-	5	ns

- Notes:
- The above characteristics apply to CLK synchronous mode.
 - t_{CYCP} indicates the APB bus clock cycle time. Please see the block diagram to refer the APB bus number which UART is connected.
 - These characteristics only guarantees the same relocate port number.
For example, the combination of SCLK_x_0 and SOT_x_1 is not guaranteed.
 - When the external load capacitance = 50pF.

MB9A100A Series



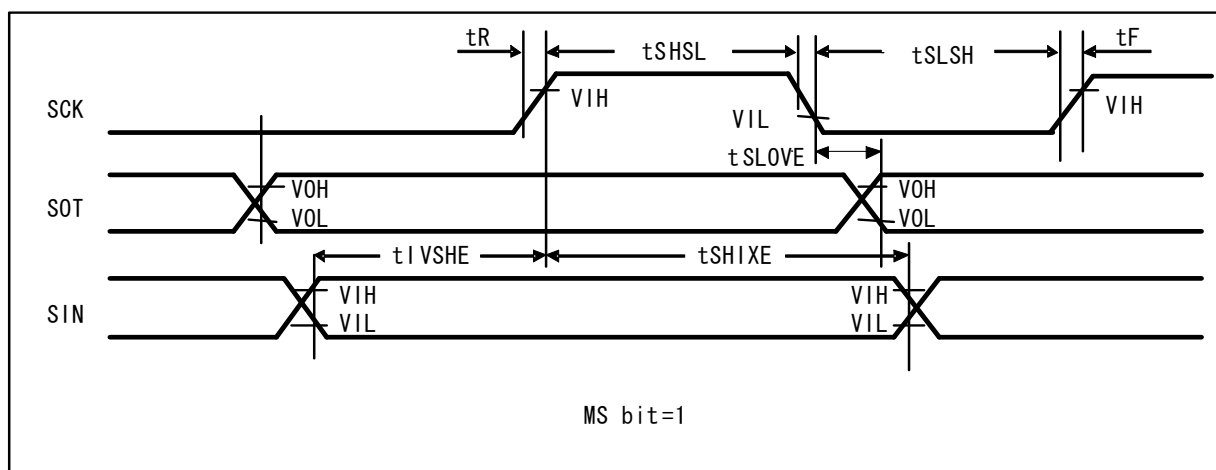
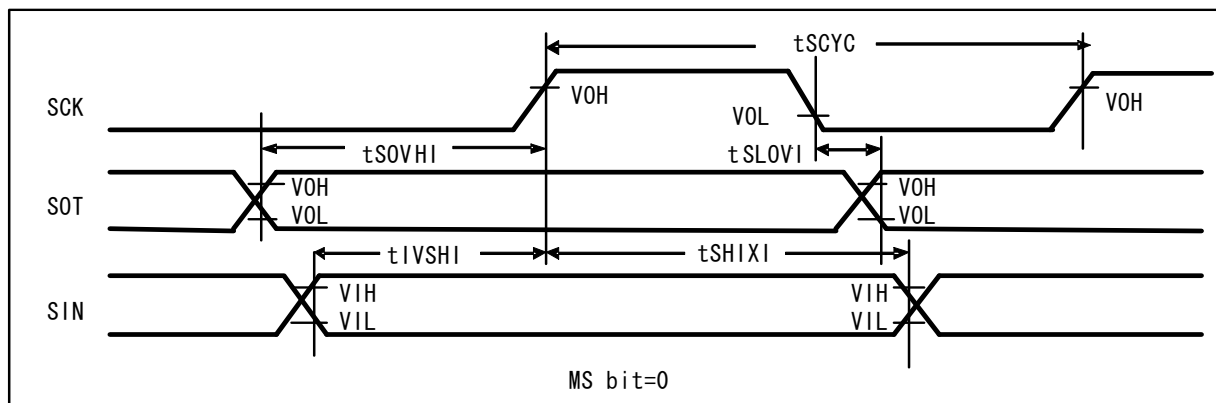
- Synchronous serial(SPI = 1, SCINV = 1)

(Vcc = 2.7V to 5.5V, Vss = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Vcc < 4.5V		Vcc ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	tSCYC	SCKx	Internal shift clock operation	4tcycp	-	4tcycp	-	ns
SCK ↓ → SOT delay time	tSLOVI	SCKx SOTx		-30	+30	- 20	+ 20	ns
SIN → SCK ↑ setup time	tIVSHI	SCKx SINx		50	-	30	-	ns
SCK ↑ → SIN hold time	tSHIXI	SCKx SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	tSOVHI	SCKx SOTx		2tcycp - 30	-	2tcycp - 30	-	ns
Serial clock "L" pulse width	tSLSH	SCKx	External shift clock operation	2tcycp - 10	-	2tcycp - 10	-	ns
Serial clock "H" pulse width	tSHSL	SCKx		tcycp + 10	-	tcycp + 10	-	ns
SCK ↓ → SOT delay time	tSLOVE	SCKx SOTx		-	50	-	30	ns
SIN → SCK ↑ setup time	tIVSHE	SCKx SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	tSHIXE	SCKx SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

- Notes:
- The above characteristics apply to CLK synchronous mode.
 - tcycp indicates the APB bus clock cycle time. Please see the block diagram to refer the APB bus number which UART is connected.
 - These characteristics only guarantee the same relocate port number.
For example, the combination of SCLKx_0 and SOTx_1 is not guaranteed.
 - When the external load capacitance = 50pF.

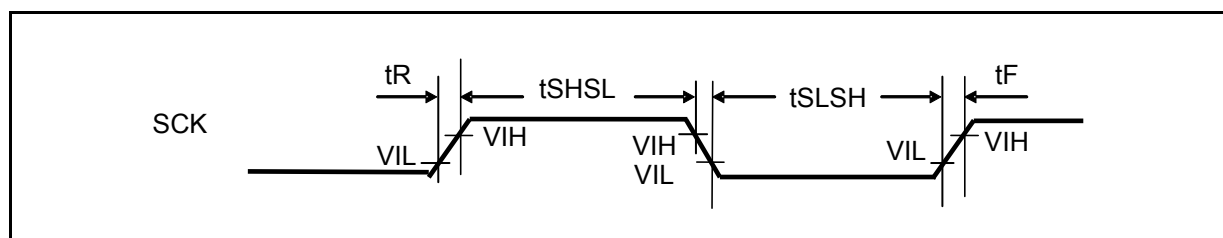
MB9A100A Series



• External clock(EXT = 1) : asynchronous only

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V T_a = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Min	Max	Unit	Remarks
Serial clock "L" pulse width	t _{SLSH}	C _L = 50pF	t _{cycp} + 10	-	ns	
Serial clock "H" pulse width	t _{SHSL}		t _{cycp} + 10	-	ns	
SCK fall time	t _F		-	5	ns	
SCK rise time	t _R		-	5	ns	



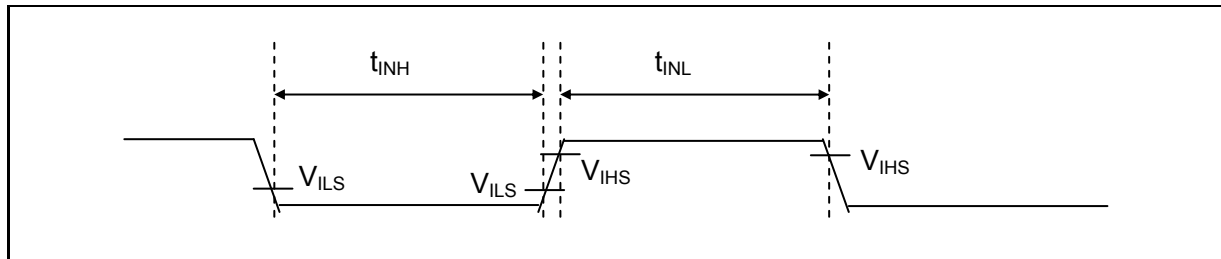
(10) External input timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH} t_{INL}	ADTG	-	$2t_{CYCP} * 1$	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTiXx	-	$2t_{CYCP} * 1$	-	ns	Wave form generator
		INT00 to INT15, NMIX	-	$2t_{CYCP} + 100 * 1$	-	ns	External interrupt
				500 * 2	-	ns	NMI

*1 : t_{CYCP} indicates the APB bus clock cycle time except stop when in stop mode. Please see the block diagram to refer the APB bus number which Multi function timer is connected.

*2 : When in stop mode, in timer mode.



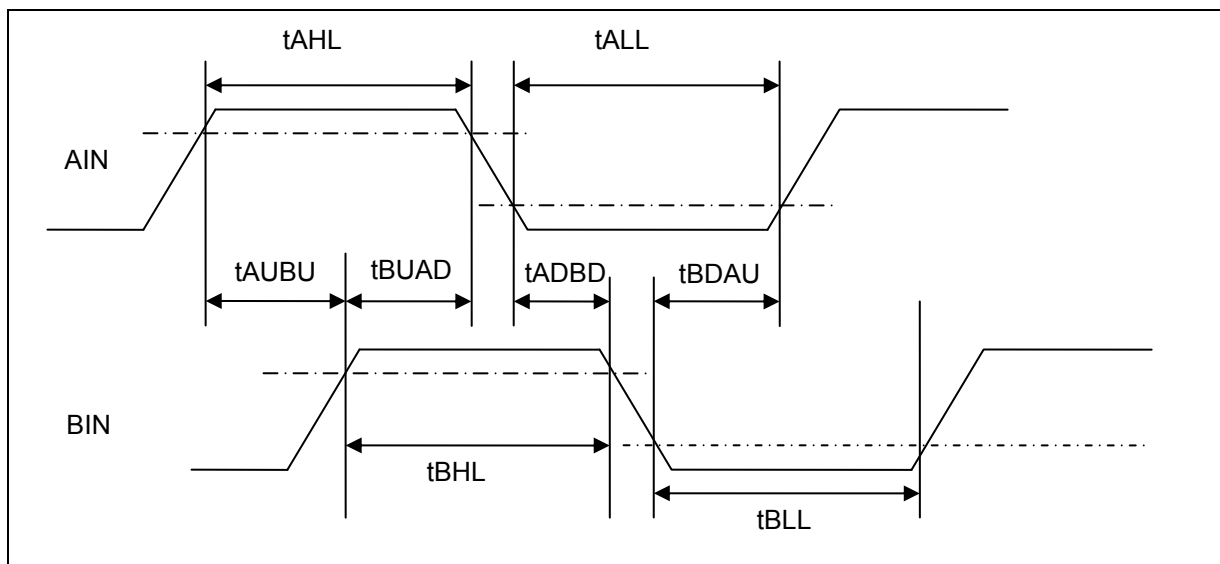
MB9A100A Series

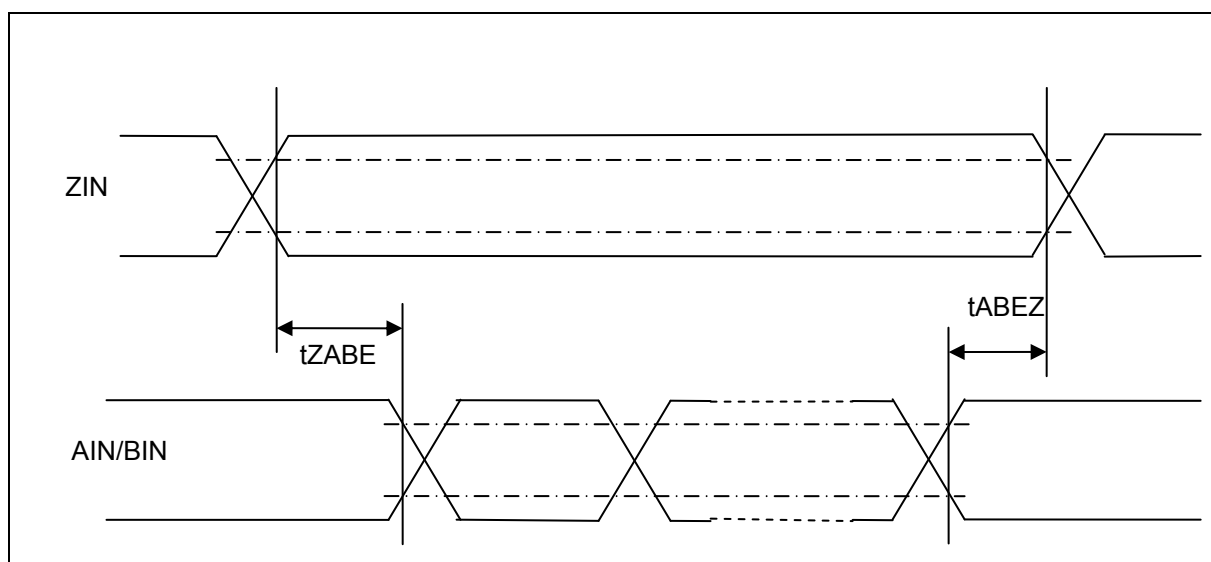
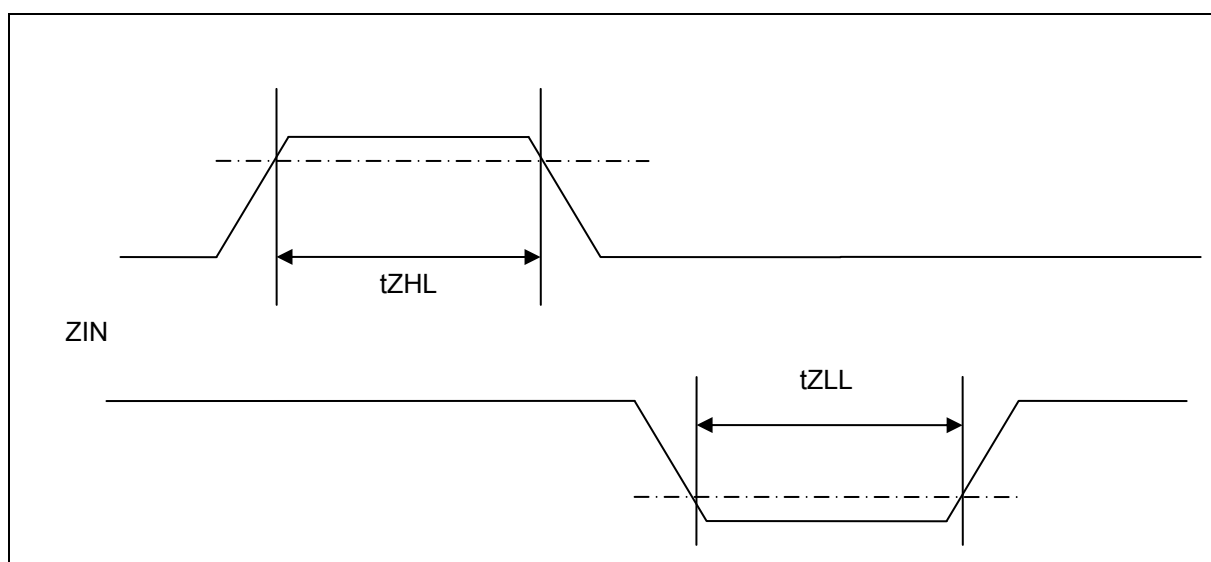
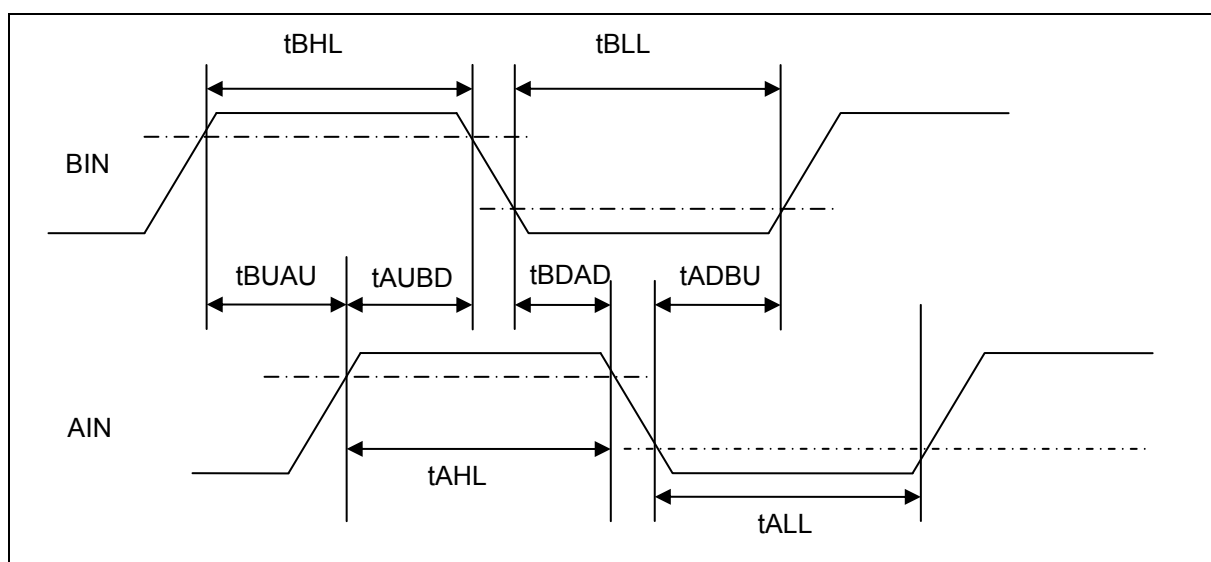
(11) Quadrature Position/Revolution Counter timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin "H" width	tAHL	-	2t _{CYCP} *	-	ns
AIN pin "L" width	tALL	-			
BIN pin "H" width	tBHL	-			
BIN pin "L" width	tBLL	-			
BIN rise time from AIN pin "H" level	tAUBU	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "H" level	tBUAD	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "L" level	tADBD	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "L" level	tBDAU	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin "H" level	tBUAU	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin "H" level	tAUBD	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin "L" level	tBDAD	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin "L" level	tADBU	PC_Mode2 or PC_Mode3			
ZIN pin "H" width	tZHL	QCR:CGSC="0"			
ZIN pin "L" width	tZLL	QCR:CGSC="0"			
AIN/BIN rise and fall time from determined ZIN level	tZABE	QCR:CGSC="1"			
Determined ZIN level from AIN/BIN rise and fall time	tABEZ	QCR:CGSC="1"			

* : t_{CYCP} indicates the APB bus clock cycle time except stop when in stop mode. Please see the block diagram to refer the APB bus number which QPRC is connected.





MB9A100A Series

(12) I²C timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V Ta = - 40°C to + 85°C)

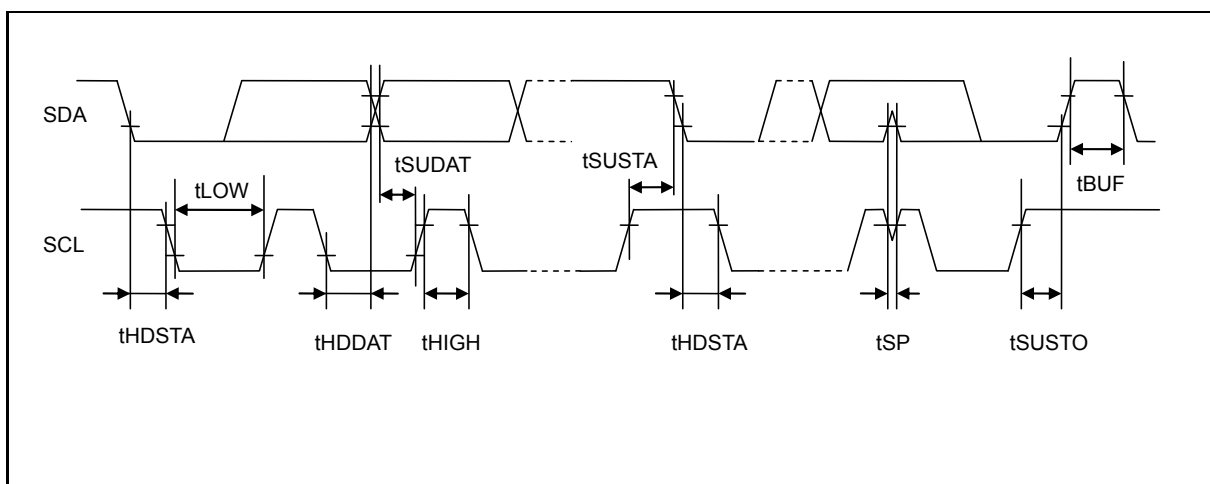
Parameter	Symbol	Conditions	Typical mode		High-speed mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	fSCL		0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	tHDSTA		4.0	-	0.6	-	μs	
SCL clock "L" width	tLOW		4.7	-	1.3	-	μs	
SCL clock "H" width	tHIGH		4.0	-	0.6	-	μs	
(Repeated) START setup time SCL ↑ → SDA ↓	tSUSTA		4.7	-	0.6	-	μs	
Data hold time SCL ↓ → SDA ↓ ↑	tHDDAT		0	3.45 (*2)	0	0.9 (*3)	μs	
Data setup time SDA ↓ ↑ → SCL ↑	tSUDAT		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	tSUSTO		4.0	-	0.6	-	μs	
Bus free time between "STOP condition" and "START condition"	tBUF		4.7	-	1.3	-	μs	
Noise filter	tSP	-	2 t _{CYCP} (*4)	-	2 t _{CYCP} (*4)	-	ns	

*1 : R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2 : The maximum tHDDAT must satisfy that it doesn't extend at least "L" period (tLOW) of device's SCL signal.

*3 : A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "tSUDAT ≥ 250 ns".

*4 : t_{CYCP} is the APB bus clock cycle time. Please see the block diagram to refer the APB bus number which I²C is connected. To use I²C, set the APB bus clock at 8 MHz or more.

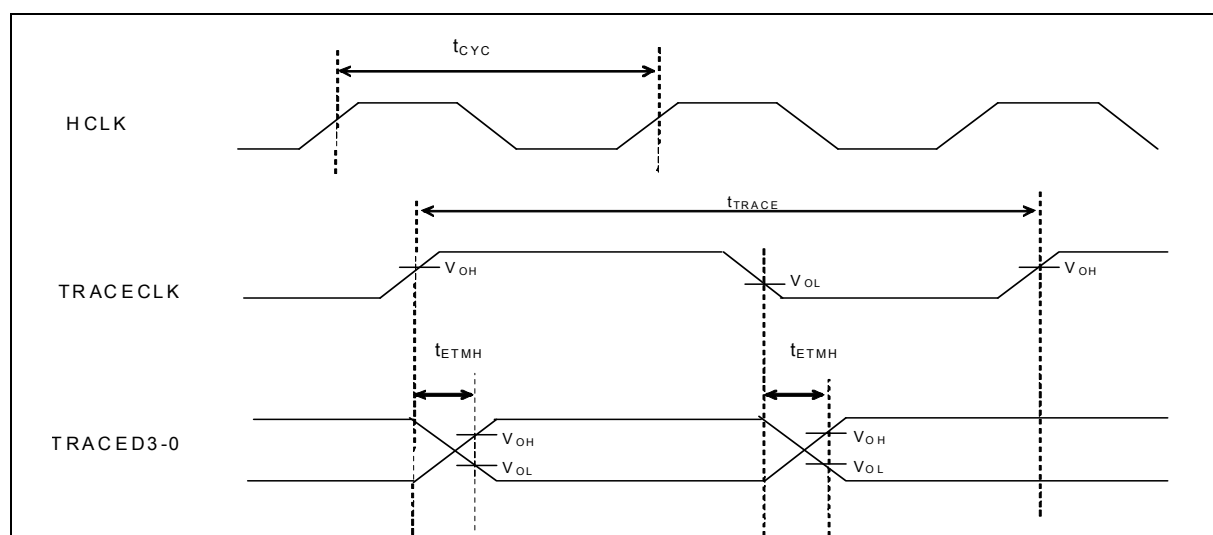


(13) ETM timing

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$ $T_a = -40^{\circ}C$ to $+85^{\circ}C$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK TRACED3 - 0	$V_{CC} \geq 4.5V$	2	9	ns	
			$V_{CC} < 4.5V$	2	15		
TRACECLK Frequency	$1/t_{TRACE}$	TRACECLK	$V_{CC} \geq 4.5V$	-	40	MHz	
			$V_{CC} < 4.5V$	-	32	MHz	
TRACECLK clock cycle time	t_{TRACE}	TRACECLK	$V_{CC} \geq 4.5V$	25	-	ns	
			$V_{CC} < 4.5V$	31.25	-	ns	

Note: When the external load capacitance = 50pF.



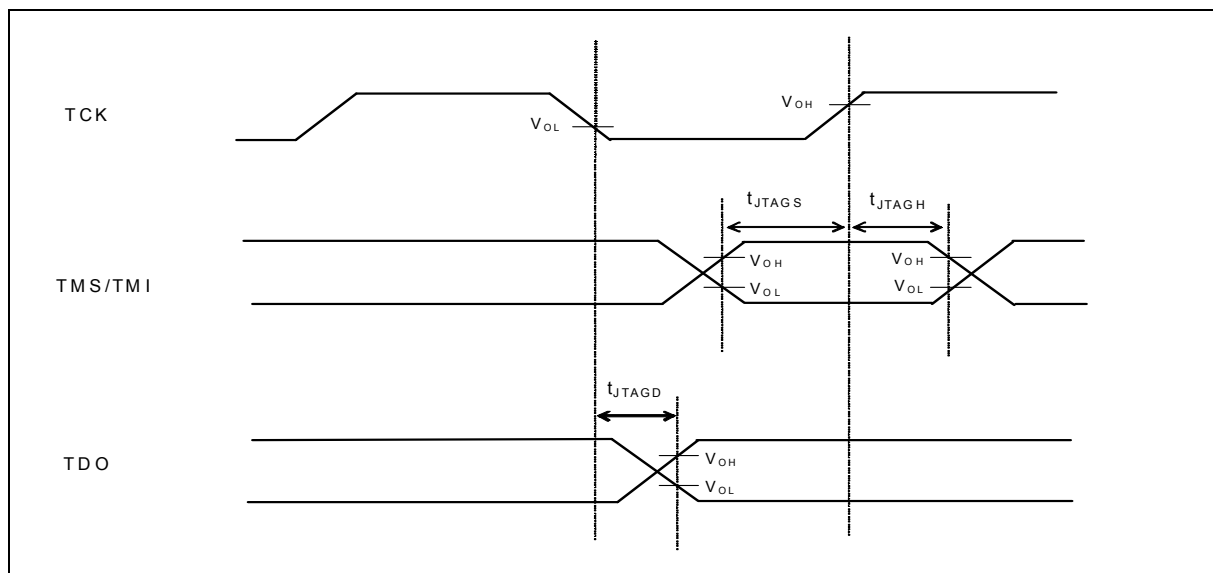
MB9A100A Series

(14) JTAG timing

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$ $T_a = -40^{\circ}C$ to $+85^{\circ}C$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS,TDI setup time	t_{JTAS}	TCK TMS,TDI	$V_{CC} \geq 4.5V$	15	-	ns	
			$V_{CC} < 4.5V$				
TMS,TDI hold time	t_{JTGH}	TCK TMS,TDI	$V_{CC} \geq 4.5V$	15	-	ns	
			$V_{CC} < 4.5V$				
TDO delay time	t_{JTGD}	TCK TDO	$V_{CC} \geq 4.5V$	-	25	ns	
			$V_{CC} < 4.5V$	-	45		

Note: When the external load capacitance = 50pF.



● 12bit A/D Converter

This chapter shows the electrical characteristics for the A/D converter.

1. Electrical characteristics for the A/D converter.

(Vcc = AVcc = 2.7V to 5.5V, Vss = AVss = 0V Ta = - 40°C to + 85°C)

Parameter	Pin name	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	-	-	-	12	bit	
Linearity error	-	- 4.5	-	+ 4.5	LSB	AVRH = 2.7V to 5.5V
Differential linearity error	-	-2.5	-	+ 2.5	LSB	
Zero transition voltage	AN0 to AN15	- 20	-	+ 20	mV	
Full transition voltage	AN0 to AN15	- 20	-	+ 20	mV	
Conversion time	-	1.0 (*1)	-	-	μs	AVcc ≥ 4.5V
Sampling time	Ts	*2	-	-	ns	AVcc ≥ 4.5V
		*2	-	-		AVcc < 4.5V
Compare clock cycle *3	Tck	55.5	-	10000	ns	AVcc ≥ 4.5V
		166.6(*4)				AVcc < 4.5V
State transition time to operation permission	Tstt	2.5	-	-	μs	
Power supply current (analog + digital)	AVCC	-	2.3	3.6	mA	A/D 1unit operation
		-	0.1	2	μA	When ADC stop
Reference power supply current (between AVRH to AVSS)	AVRH	-	2.2	3.0	mA	A/D 1unit operation AVRH=5.5V
		-	0.03	0.6	μA	When ADC stop
Analog input capacity	Cin	-	-	14.5	pF	
Analog input resistance	Rin	-	-	0.93	kΩ	AVcc ≥ 4.5V
				2.04		AVcc < 4.5V
Interchannel disparity	-	-	-	4	LSB	
Analog port input current	AN0 to AN15	-	-	5	μA	
Analog input voltage	AN0 to AN15	AVSS	-	AVRH	V	
Reference voltage	AVRH	AVSS	-	AVCC	V	

*1: Conversion time is the value of sampling time(Ts) + compare time(Tc).

The condition of the minimum conversion time is when HCLK=72MHz, the value of sampling time: 0.222μs, the value of sampling time: 778ns (AVcc ≥ 4.5V)

Ensure that it satisfies the value of sampling time(Ts) and compare clock cycle (Tck).

For setting of sampling time and compare clock cycle, see chapter "12-bit A/D Converter" in "Peripheral Manual".

ADC register is set at APB bus clock timing. Sampling and compare clock is set at Base clock(HCLK).

*2: A necessary sampling time changes by external impedance.

Ensure that it set the sampling time to satisfy (Equation 1)

*3: Compare time (Tc) is the value of (Equation 2)

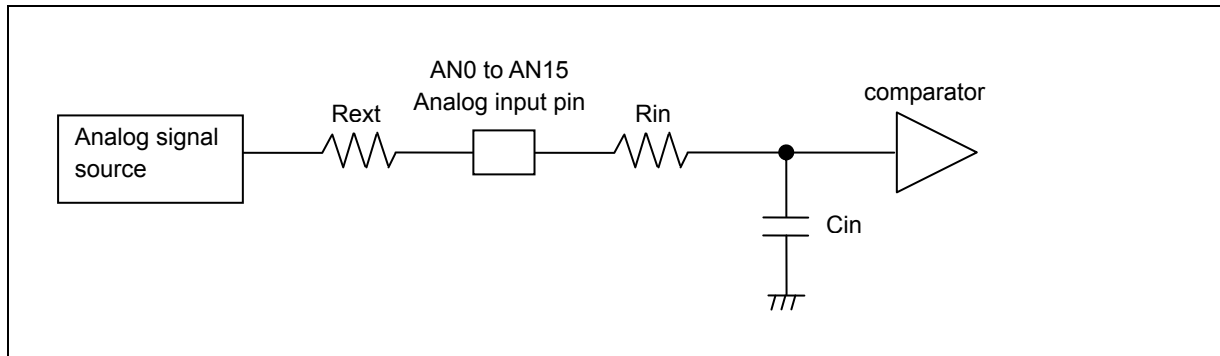
MB9A100A Series

(Continued)

*4: When 12bit A/D converter is used at $AV_{CC} < 4.5V$, there is a limitation as follows.

It cannot be used at minimum compare clock cycle when HCLK is set over 54MHz, because maximum compare clock division ratio is "9"(please refer **FM3 PERIPHERAL MANUAL** chapter "12bit A/D converter"),

Please set the HCLK frequency under 54MHz.



$$\text{(Equation 1) } T_s \geq (R_{in} + R_{ext}) \times C_{in} \times 9$$

T_s : Sampling time

R_{in} : input resistance of A/D = $0.93k\Omega$ $4.5 \leq AV_{CC} \leq 5.5$
input resistance of A/D = $2.04k\Omega$ $2.7 \leq AV_{CC} < 4.5$

C_{in} : input capacity of A/D = $14.5pF$ $2.7 \leq AV_{CC} \leq 5.5$

R_{ext} : Output impedance of external circuit

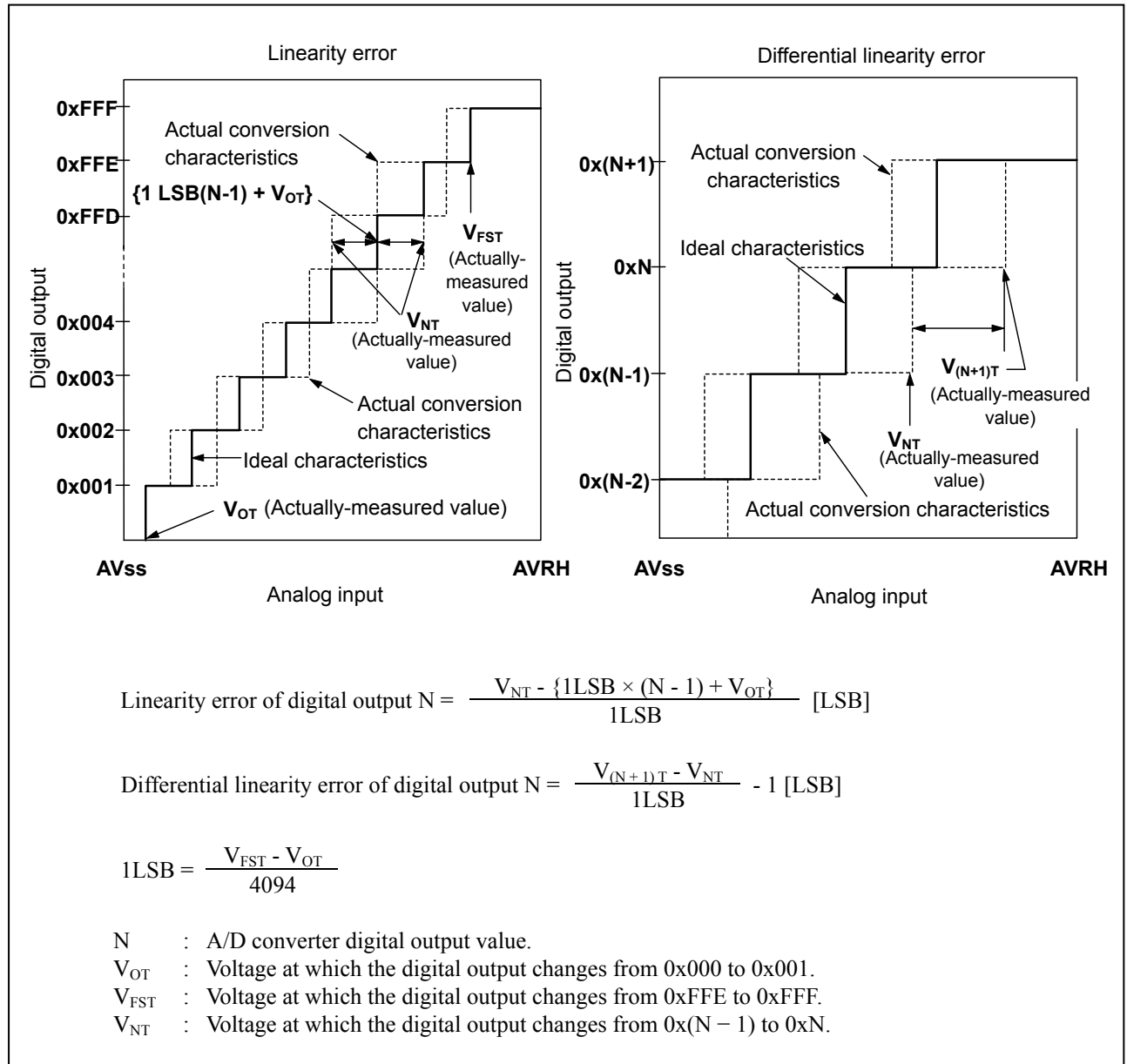
$$\text{(Equation 2) } T_c = T_{ck} \times 14$$

T_c : Compare time

T_{ck} : Compare clock cycle

• Definition of 12-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Deviation of the line between the zero-transition point (0b000000000000 $\longleftrightarrow$ 0b000000000001) and the full-scale transition point (0b111111111110 $\longleftrightarrow$ 0b111111111111) from the actual conversion characteristics.
- Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



MB9A100A Series

● Low voltage detection characteristics

1. Low voltage detection reset

(Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.20	2.40	2.60	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

2. Interrupt of low voltage detection

(Ta = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 0000	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 0001	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 0010	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 0011	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 0100	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 0111	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 1000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 1001	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	T _{LVDW}	-	-	-	2040 × t _{CYCP} *	μs	

* : t_{CYCP} indicates the APB2 bus clock cycle time.

● Flash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 5.5V, T_a = - 40°C to + 85°C)

Parameter		Value			Value	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.6	3.1	s	Excludes write time prior to internal erase
	Small Sector		0.3	1.6		
Half word (16 bit) write time		-	25	400	μs	Not including system-level overhead time.
Chip erase time		-	7.2	37.6	s	Excludes write time prior to internal erase

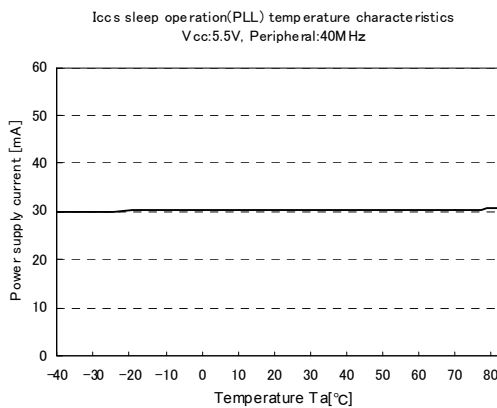
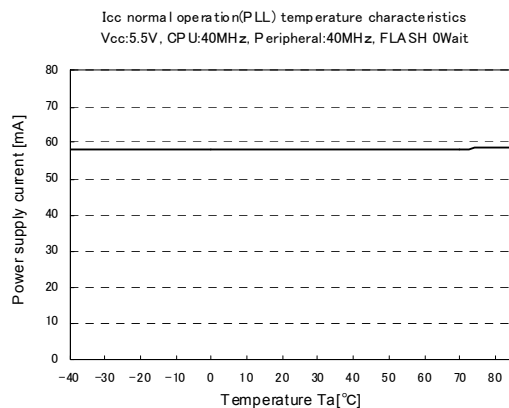
Erase/write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20 *	
10,000	10 *	
100,000	5 *	

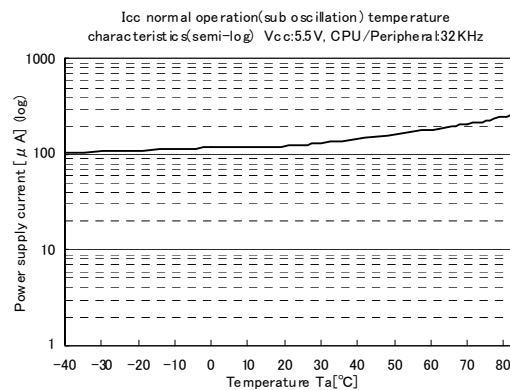
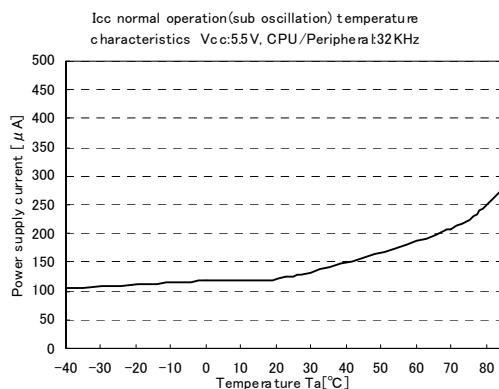
*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C) .

■ EXAMPLE OF CHARACTERISTIC

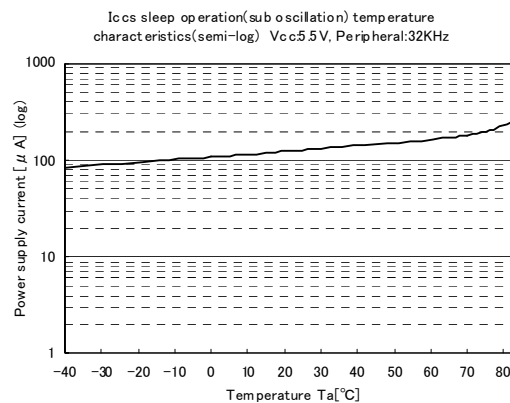
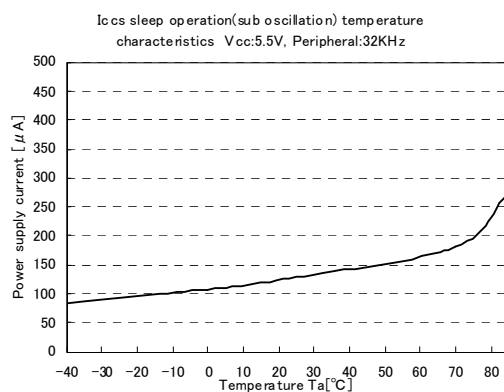
Power supply current (PLL run mode, PLL sleep mode)



Power supply current (Sub run mode)

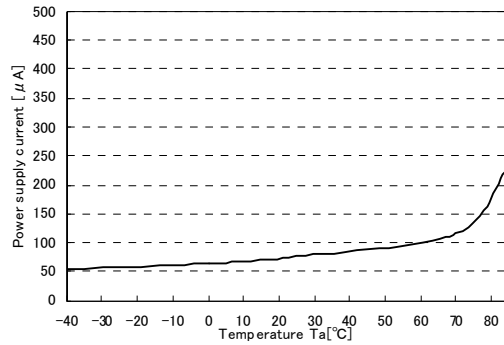


Power supply current (Sub sleep mode)

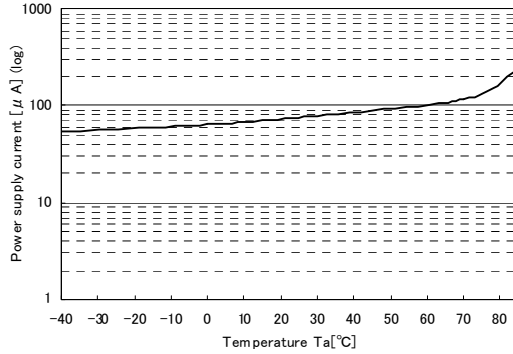


Power supply current (Sub timer mode)

I_{CC1} timer mode(sub oscillation) temperature characteristics
Vcc:5.5V, LVD is Off

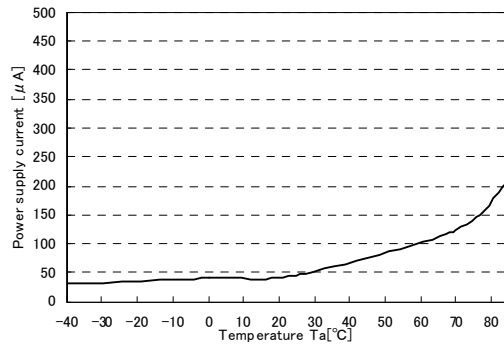


I_{CC1} timer mode(sub oscillation) temperature characteristics(semi-log) Vcc:5.5V, LVD is Off

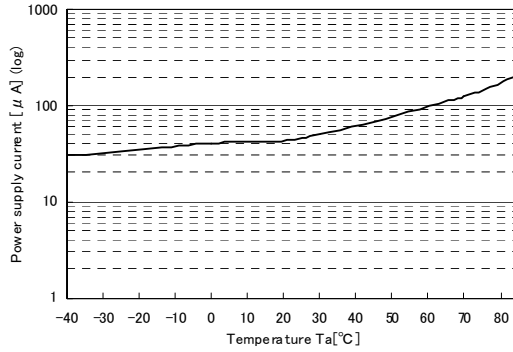


Power supply current (Stop mode)

I_{CC1} stop mode (sub oscillation) temperature characteristics
Vcc:5.5V, LVD is Off



I_{CC1} stop mode (sub oscillation) temperature characteristics(semi-log) Vcc:5.5V, LVD is Off



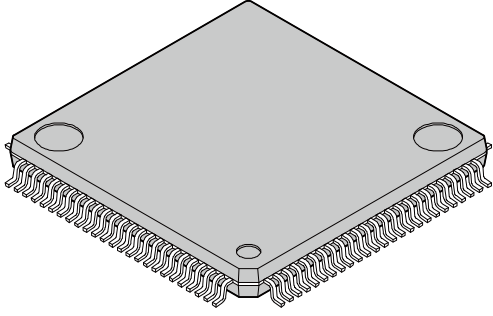
MB9A100A Series

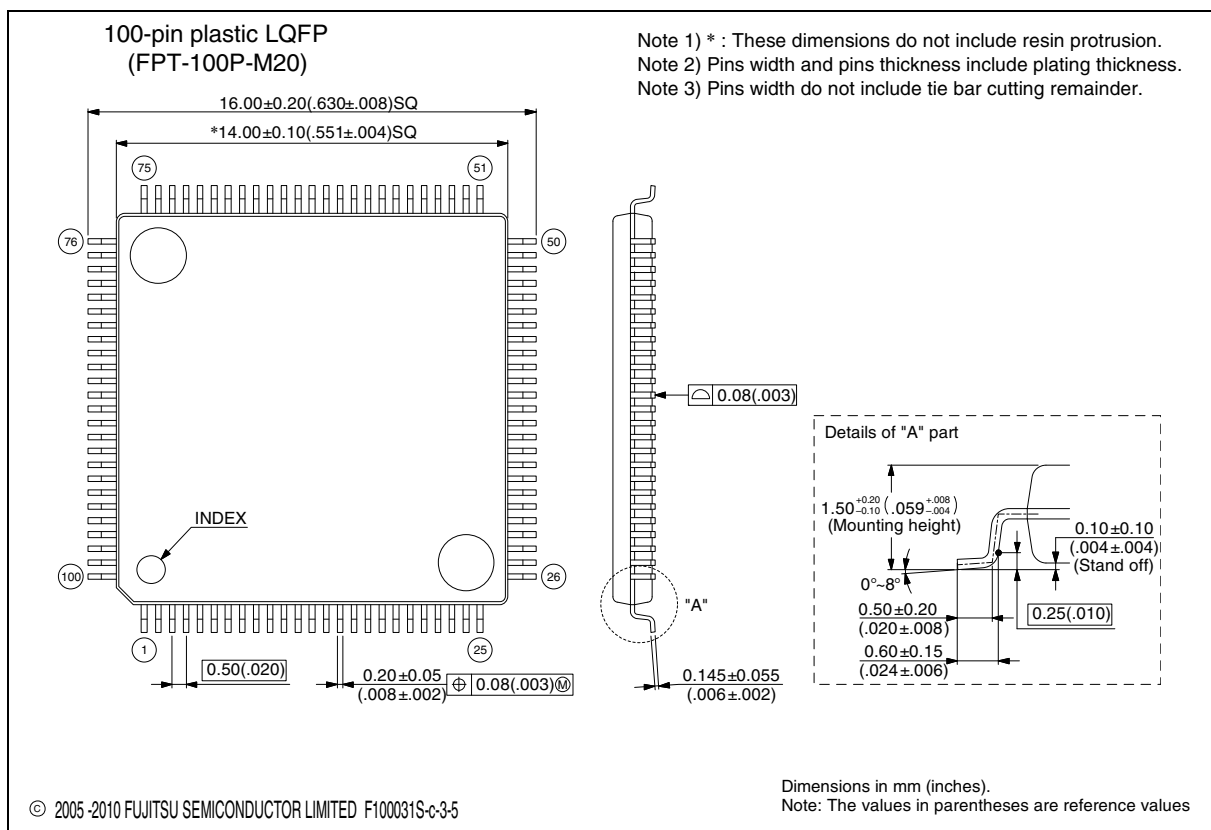
■ ORDERING INFORMATION

Part number	Package
MB9AF102NAPMC	Plastic • LQFP(0.5mm pitch),100-pin (FPT-100P-M20*/M23)
MB9AF104NAPMC	
MB9AF105NAPMC	
MB9AF102RAPMC	Plastic • LQFP(0.5mm pitch),120-pin (FPT-120P-M21/M37)
MB9AF104RAPMC	
MB9AF105RAPMC	
MB9AF102NABGL	Plastic • PFBGA(0.8mm pitch),112-pin (BGA-112P-M04)
MB9AF104NABGL	
MB9AF105NABGL	
MB9AF102NAPF	Plastic • QFP(0.65mm pitch),100-pin (FPT-100P-M06)
MB9AF104NAPF	
MB9AF105NAPF	

* : ES product only

■ PACKAGE DIMENSIONS

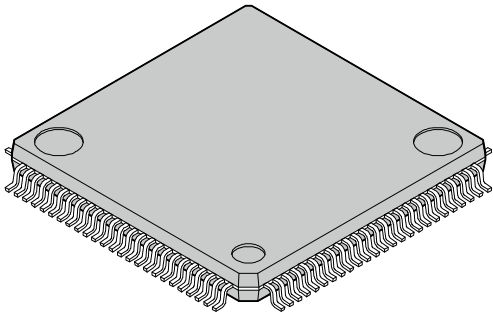
 100-pin plastic LQFP (FPT-100P-M20)	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
	Code (Reference)	P-LFQFP100-14×14-0.50

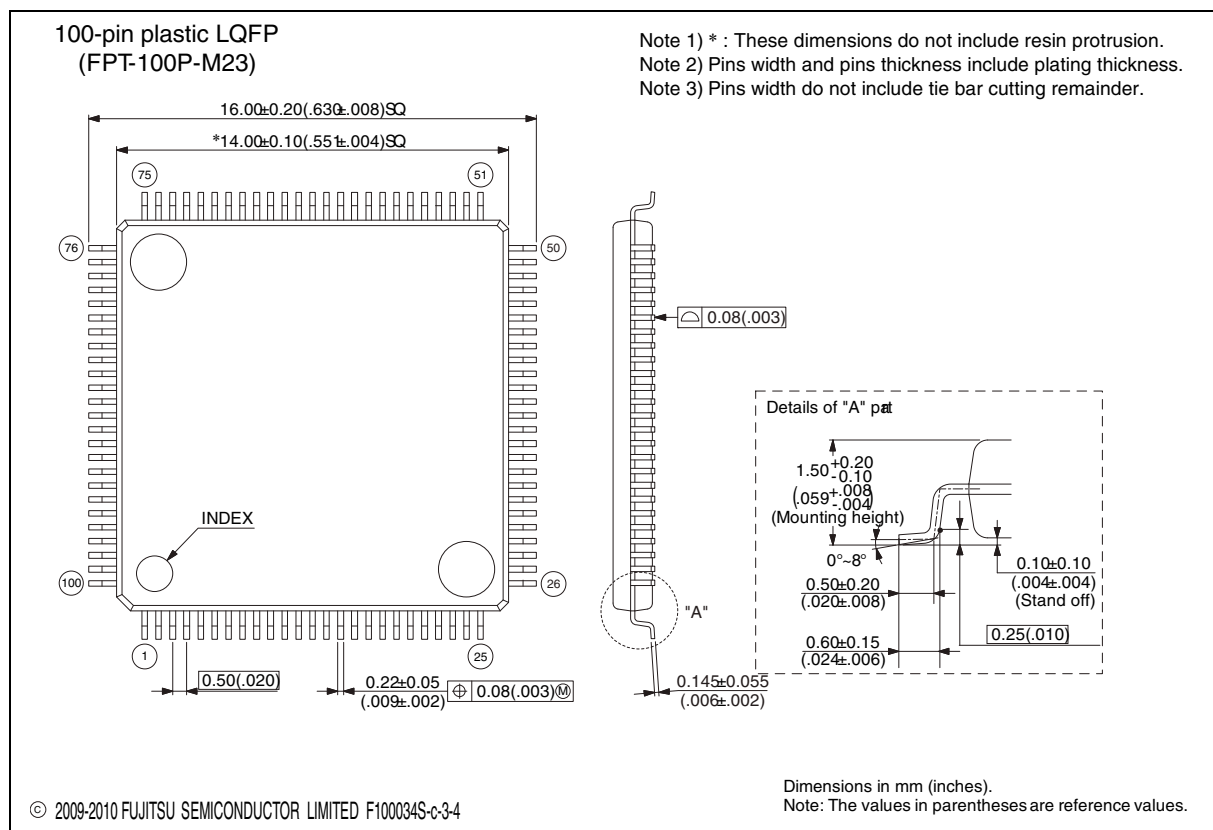


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MB9A100A Series

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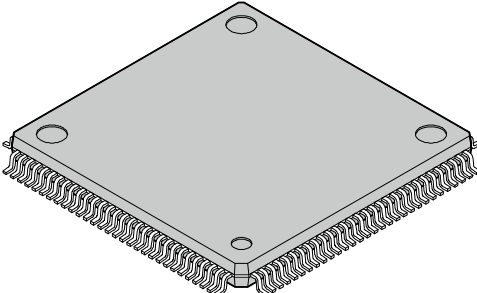
 100-pin plastic LQFP (FPT-100P-M23)	Lead pitch	0.50 mm
	Package width × package length	14.00 mm × 14.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.65 g

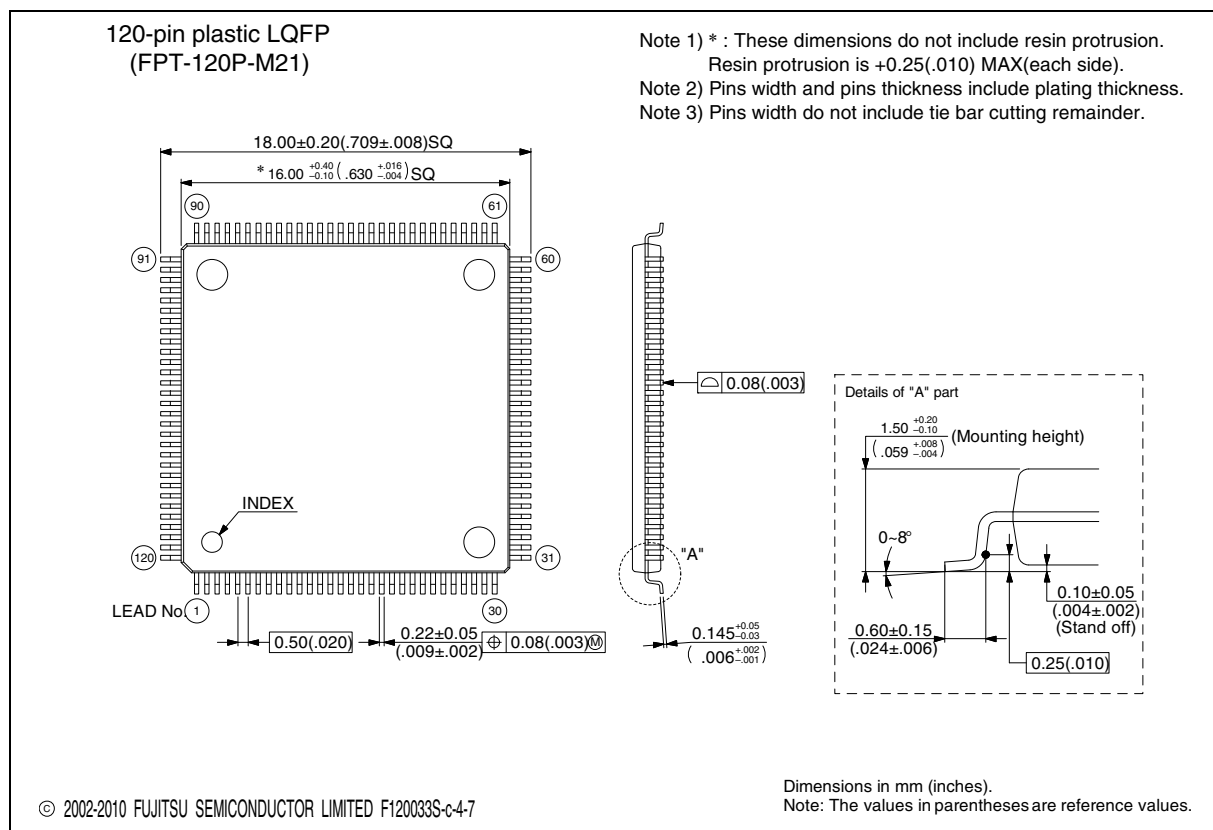


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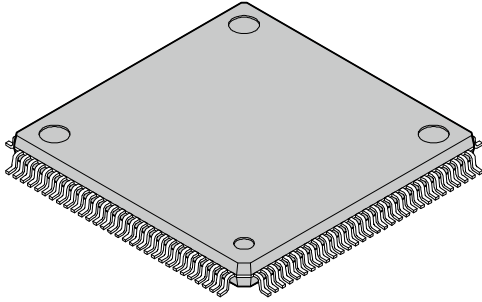
120-pin plastic LQFP  (FPT-120P-M21)	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
	Code (Reference)	P-LFQFP120-16×16-0.50

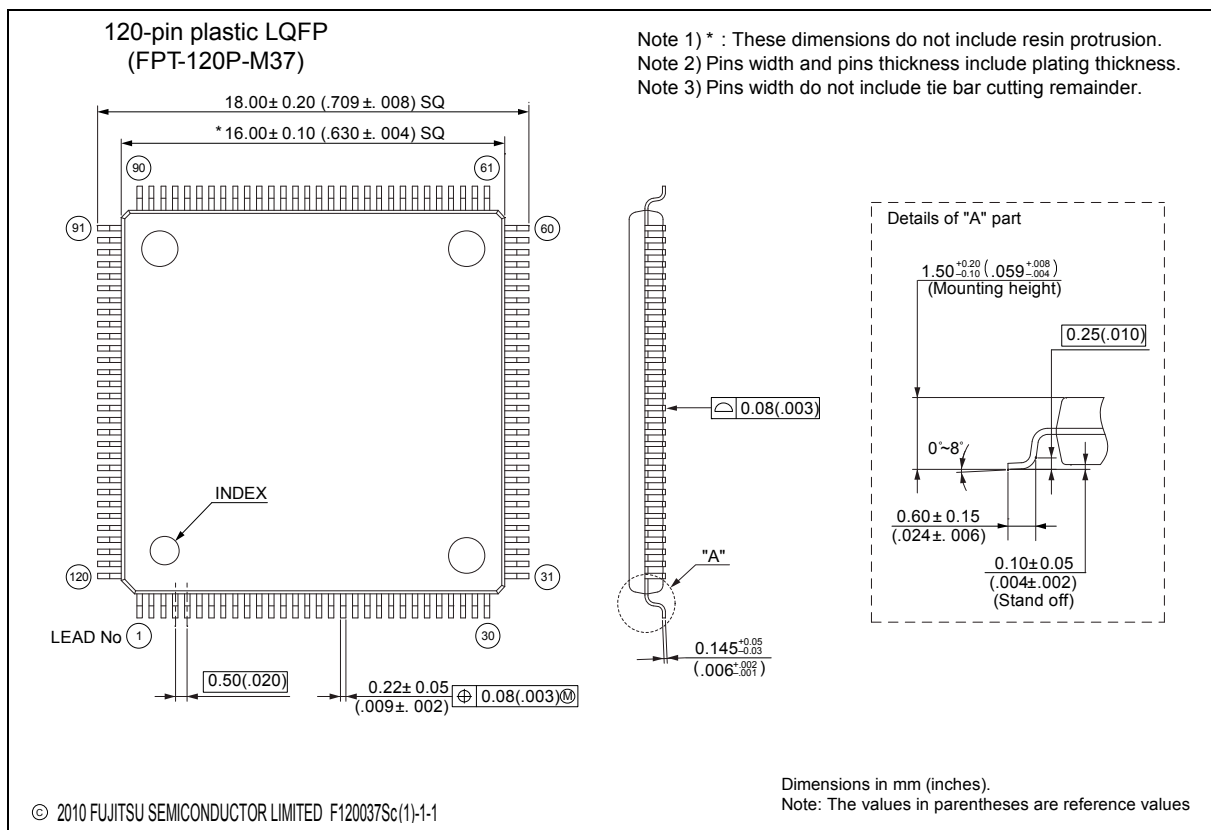


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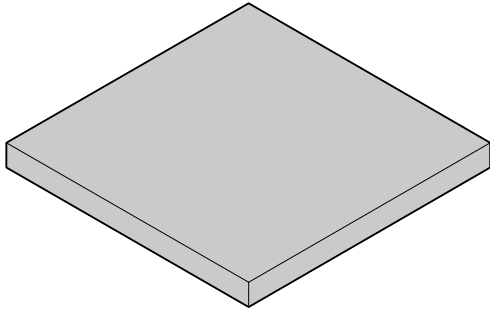
120-pin plastic LQFP  (FPT-120P-M37)	Lead pitch	0.50 mm
	Package width × package length	16.0 mm × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.88 g
	Code (Reference)	P-LFQFP120-16 × 16-0.50

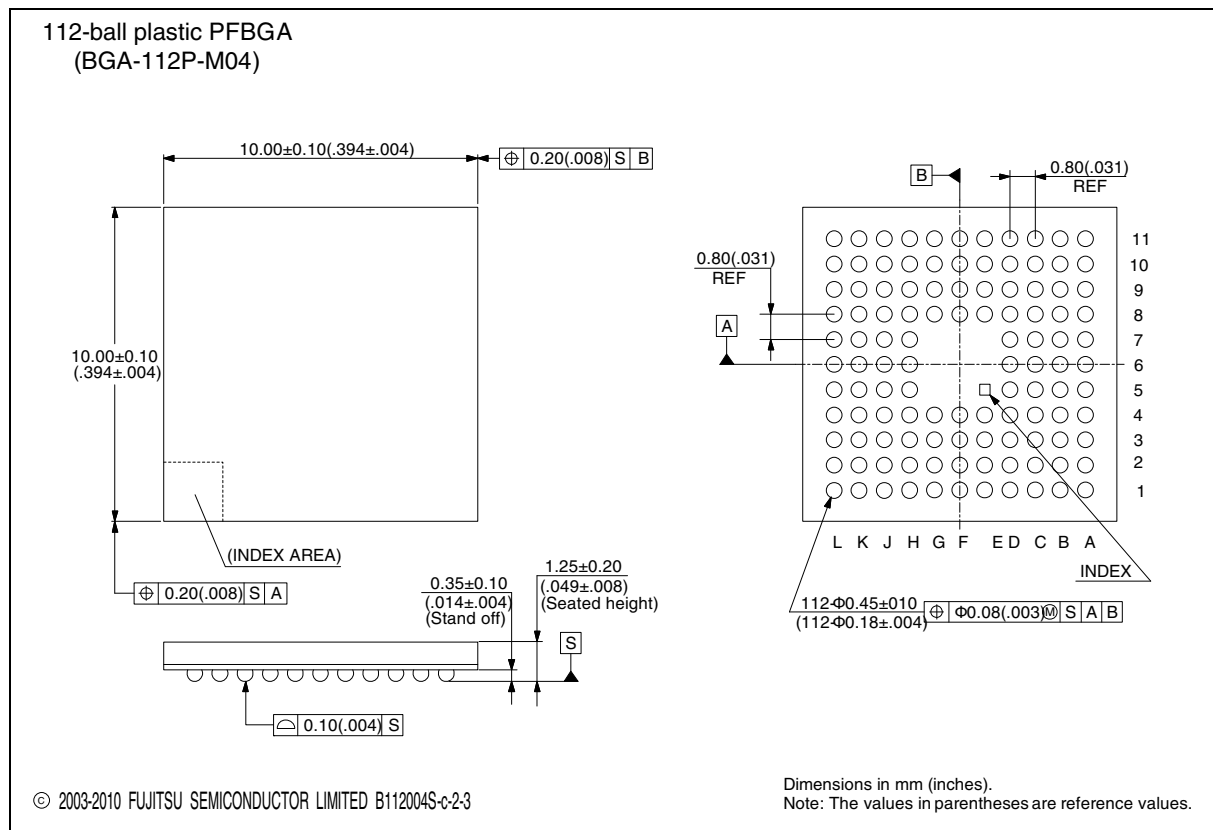


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<http://edevice.fujitsu.com/package/en-search/>

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112-ball plastic PFBGA  (BGA-112P-M04)	Ball pitch	0.80 mm
	Package width × package length	10.00 × 10.00 mm
	Lead shape	Soldering ball
	Sealing method	Plastic mold
	Ball size	Φ 0.45 mm
	Mounting height	1.45 mm Max.
	Weight	0.22 g



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MEMO

MEMO

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FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan

Tel: +81-45-415-5858

<http://jp.fujitsu.com/fsl/en/>

For further information please contact:

North and South America

FUJITSU SEMICONDUCTOR AMERICA, INC.

1250 E. Arques Avenue, M/S 333

Sunnyvale, CA 94085-5401, U.S.A.

Tel: +1-408-737-5600 Fax: +1-408-737-5999

<http://us.fujitsu.com/micro/>

Asia Pacific

FUJITSU SEMICONDUCTOR ASIA PTE. LTD.

151 Lorong Chuan,

#05-08 New Tech Park 556741 Singapore

Tel: +65-6281-0770 Fax: +65-6281-0220

<http://sg.fujitsu.com/semiconductor/>

Europe

FUJITSU SEMICONDUCTOR EUROPE GmbH

Pittlerstrasse 47, 63225 Langen, Germany

Tel: +49-6103-690-0 Fax: +49-6103-690-122

<http://emea.fujitsu.com/semiconductor/>

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.

Rm. 3102, Bund Center, No.222 Yan An Road (E),

Shanghai 200002, China

Tel: +86-21-6146-3688 Fax: +86-21-6335-1605

<http://cn.fujitsu.com/fss/>

Korea

FUJITSU SEMICONDUCTOR KOREA LTD.

902 Kosmo Tower Building, 1002 Daechi-Dong,

Gangnam-Gu, Seoul 135-280, Republic of Korea

Tel: +82-2-3484-7100 Fax: +82-2-3484-7111

<http://kr.fujitsu.com/fsk/>

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.

10/F., World Commerce Centre, 11 Canton Road,

Tsimshatsui, Kowloon, Hong Kong

Tel: +852-2377-0226 Fax: +852-2376-3269

<http://cn.fujitsu.com/fsp/>

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