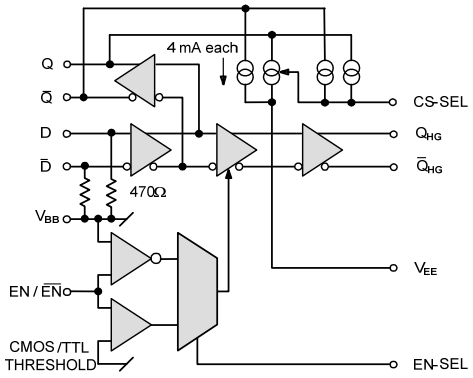
CTSLV399
LVPECL/LVDS Oscillator Gain Stage & Buffer with Selectable Enable
MLP8, MSOP8

Features

- Minimizes External Components
- Selectable Enable Polarity and Threshold (CMOS or PECL)
- 3V to 5.5V Power Supply
- Similar Operation as CTS100LVEL16VT Except with LVDS Outputs

Block Diagram



Description

The CTSLV399 is a specialized oscillator gain stage with an LVDS output buffer including an enable. The selectable enable input allows continuous oscillator operation by only controlling the Q_{HG} /$\overline{Q}_{HG}$ outputs.

The CTSLV399 provides adjustable internal pull-down current sources for the Q/$\overline{Q}$ outputs. Internal input biasing further reduces the number of needed external components

Engineering Notes

The CTSLV399 is a specialized oscillator gain stage with LVDS output buffer including an enable. The enable input (EN) allows continuous oscillator operation by only controlling the Q_{HG} /$\overline{Q}_{HG}$ outputs.
The CTSLV399 also provides a V_{BB} and 470Ω internal bias resistors from D to V_{BB} and $\overline{D}$ to V_{BB}. The V_{BB} pin can support 1.5 mA sink/source current. Bypassing V_{BB} to ground with a 0.01 µF capacitor is recommended.

Functionality MLP8 Package (CTSLV399NG)
The MLP8, NG options of the CTSLV399, provide a PECL/ECL level enable input ($\overline{EN}$). When the $\overline{EN}$ input is LOW, the $\overline{Q}$ and Q_{HG}/$\overline{Q}_{HG}$ outputs pass data from the inputs. When $\overline{EN}$ is HIGH, the $\overline{Q}$ output continues to pass data while the Q_{HG} output is forced high and the $\overline{Q}_{HG}$ output is forced low.

Only the $\overline{Q}$ output operates with a current source (4 mA) to V_{EE}. This is accomplished by internal bonding of CS-SEL. An external resistor may also be used to increase pull-down current to a maximum of 25mA (includes 4mA on-chip current source).

The CTSLV399NB and CTSLV399ND versions operate with a single ended data input (D). The $\overline{D}$ input is internally bonded directly to the V_{BB} pin bypassing the 470Ω bias resistor.

Functionality MLP8 Package (CTSLV399N) & MSOP8 Package (CTSLV399T)
The MSOP8 (T) and MLP8 (N) versions of the CTSLV399 provide a CMOS/TTL level enable input (EN). When the EN input is HIGH, the $\overline{Q}$ and Q_{HG}/$\overline{Q}_{HG}$ outputs pass data from the inputs. When EN is LOW, the $\overline{Q}$ output continues to pass data while the Q_{HG} output is forced high and the $\overline{Q}_{HG}$ output is forced low.

Only the $\overline{Q}$ output operates with a current source (4 mA) to V_{EE}. This is accomplished by internal bonding of CS-SEL. An external resistor may also be used to increase pull-down current to a maximum of 25mA (includes 4mA on-chip current source).

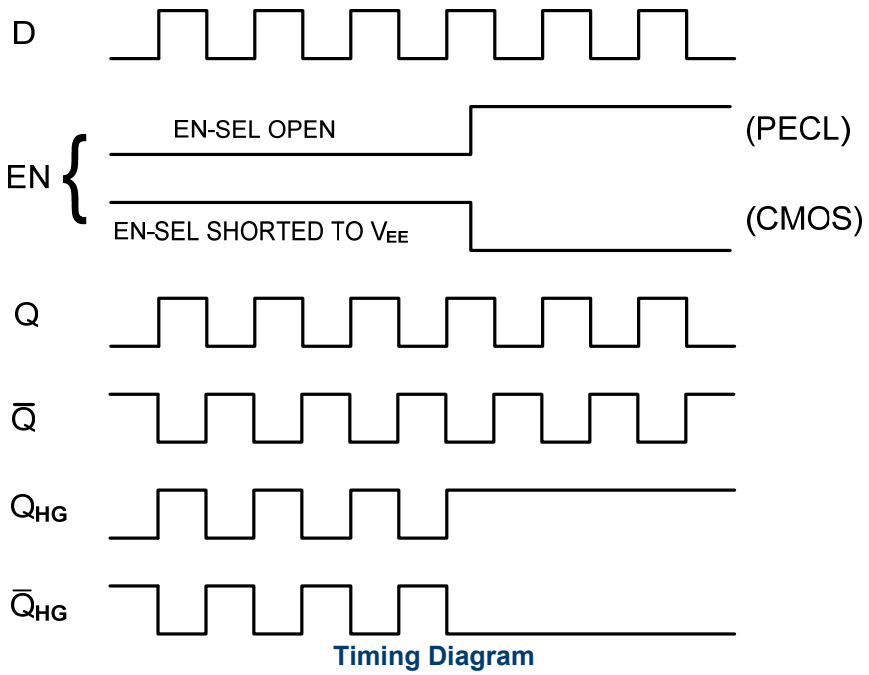
The MSOP8 (T) and MLP8 (N) CTSLV399 operates with a single ended data input (D). The $\overline{D}$ input is internally bonded directly to the V_{BB} pin bypassing the 470Ω bias resistor.

Enable Truth Table

EN-SEL	EN/ $\overline{EN}$	Q/$\overline{Q}$	Q_{HG}	$\overline{Q}_{HG}$
NC	PECL Low, V_{EE} or NC	Data	Data	Data
	PECL High or V_{CC}	Data	High	Low
V_{EE}[1]	CMOS/TTL Low, V_{EE} or NC	Data	High	Low
	CMOS/TTL High or V_{CC}[2]	Data	Data	Data

1 EN-SEL connections must be less than 1Ω.

2 An external ≤ 20kΩ pull-up resistor between EN and V_{CC} ensures a High when the EN pin is not driven.

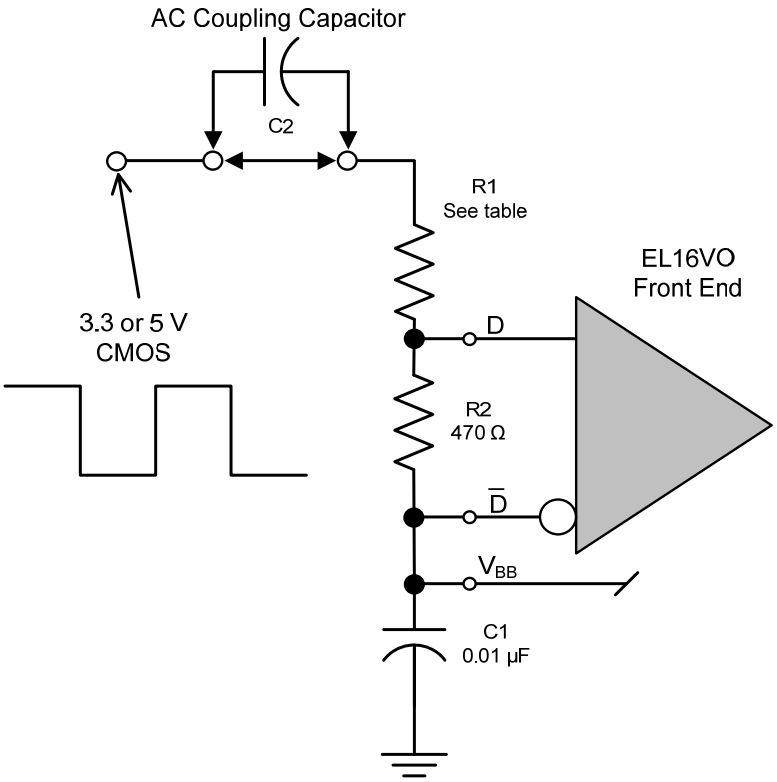


Timing Diagram

Current Source Truth Table

CS-SEL	Q	$\overline{Q}$
NC	4mA typ	4mA typ
V_{EE}[1]	8mA typ	8mA typ
V_{CC}[1]	0	4mA typ

[1] Connection must be less than 1Ω.

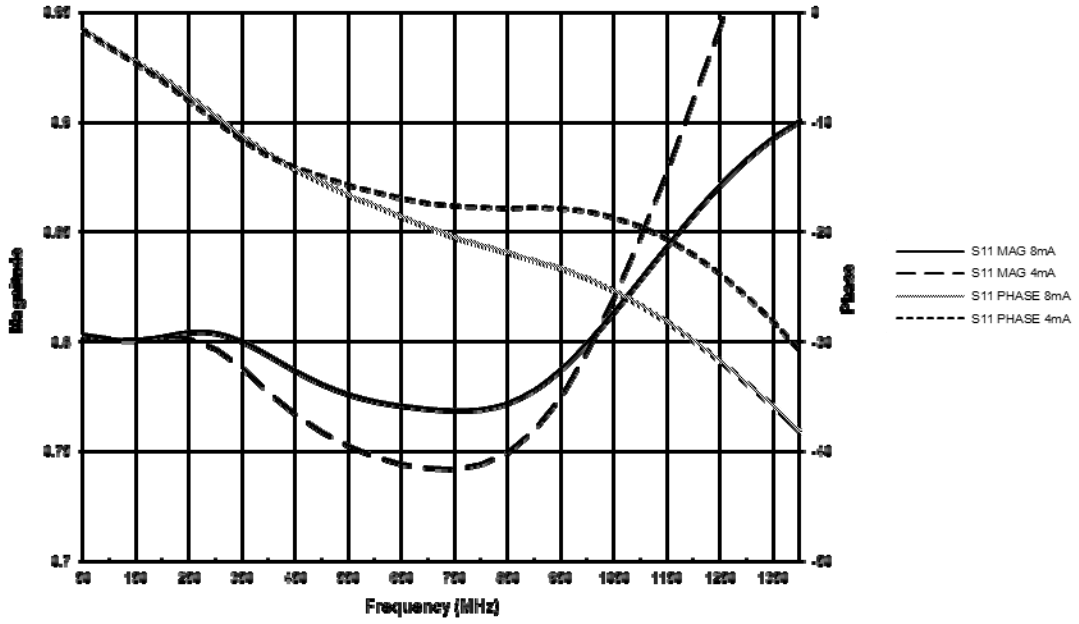


Application Circuit for CMOS inputs

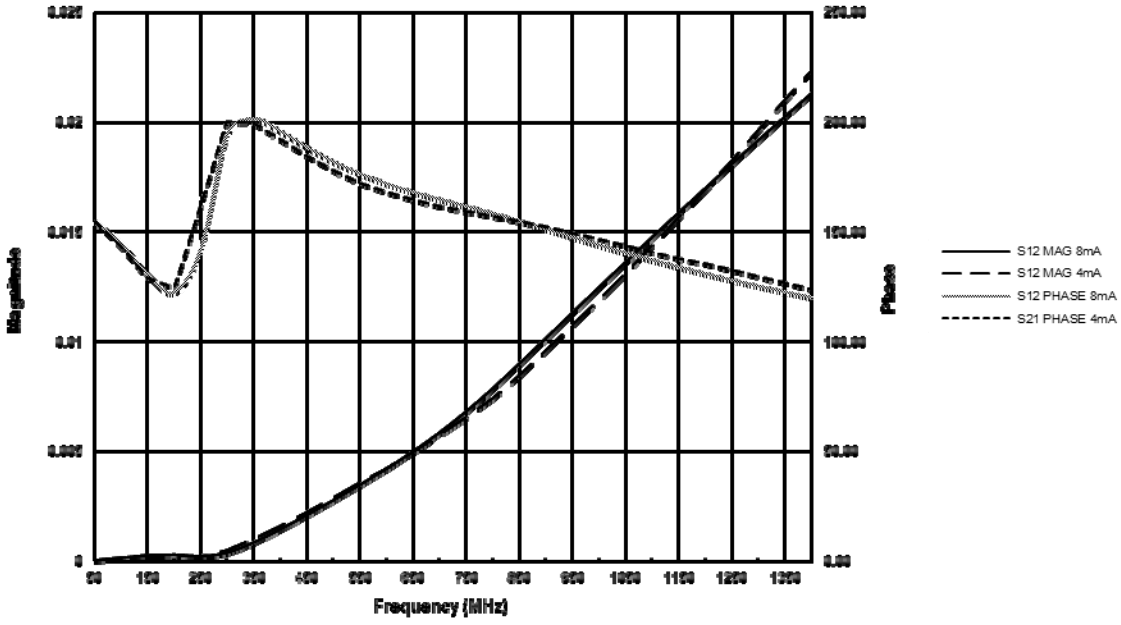
Recommended Component Values for CMOS Single Ended Inputs

Input Type	R1[1] Value	
	AC Coupled (C2 in circuit)	DC Coupled (C2 shorted)
3.3 V CMOS	1.1 kΩ	2.0 kΩ
5.0 V CMOS	1.6 kΩ	3.3 kΩ

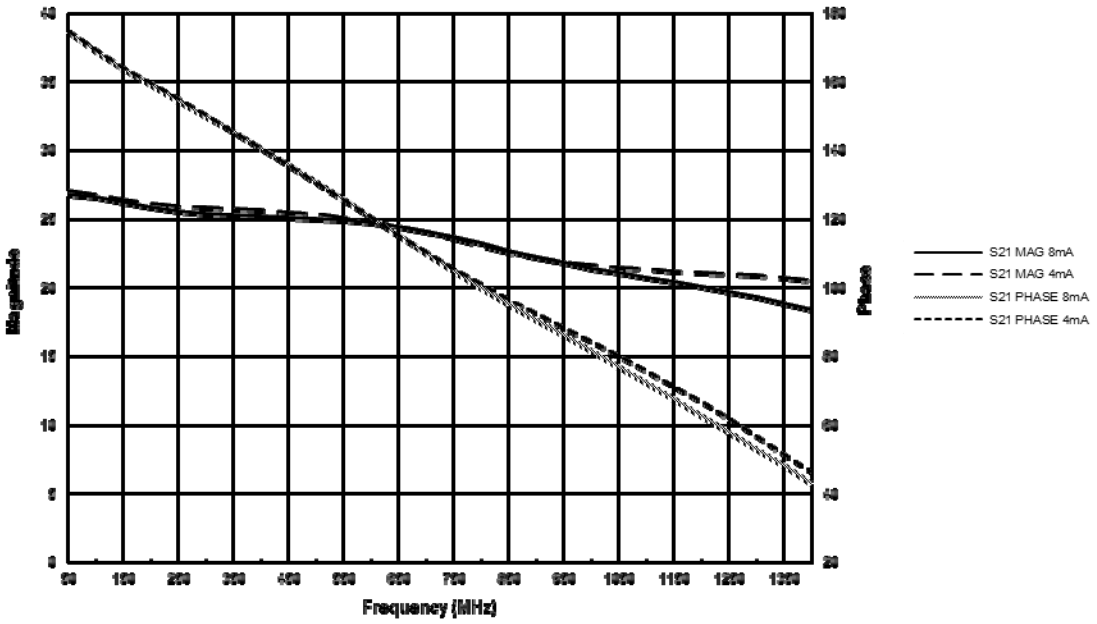
R1 should be chosen so that the input swing on the D input with respect to $\overline{D}$ is in the range of ±80 to ±1000 mV, per the AC Characteristics table and the D input is < ±750 mV with respect to V_{BB}.



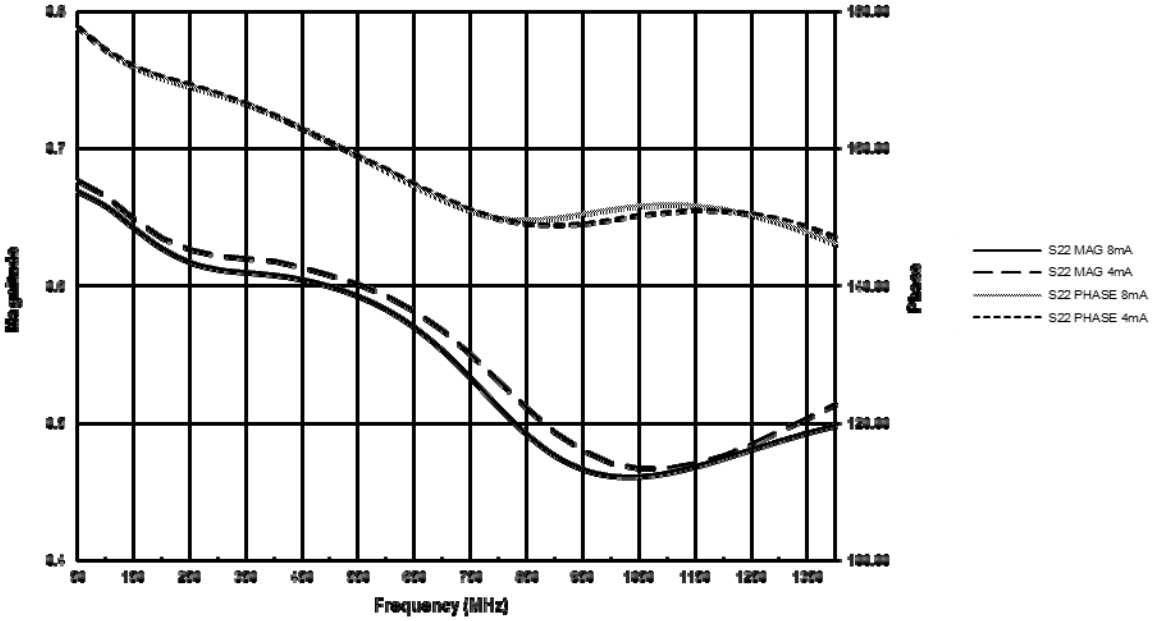
S11, 50Ω AC load



S12, 50Ω AC load



S21, 50Ω AC load



S22, 50Ω AC load

Electrical Specifications

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V_{CC}	PECL Power Supply	V_{EE} = 0V	0 to + 6.0	V
V_I	PECL Input Voltage	V_{EE} = 0V	0 to + 6.0	V
$V_{D/}$	D/$\overline{D}$ Input Voltage	Referenced to V_{BB}	±0.75	V
I_{OUT}	Output Current	Continuous Q/$\overline{Q}$	25	mA
		Surge Q/$\overline{Q}$	50	
		Continuous Q_{HG}/$\overline{Q}_{HG}$	5	
		Surge Q_{HG}/$\overline{Q}_{HG}$	10	
T_A	Operating Temperature Range	-	-40 to +85	°C
T_{STG}	Storage Temperature Range	-	-65 to +150	°C
ESD_{HBM}	Human Body Model Electro Static Discharge	-	2500	V
ESD_{MM}	Machine Model Electro Static Discharge	-	200	V
ESD_{CDM}	Charged Device Model Electro Static Discharge	-	2000	V

100K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	2255	2465	2275	2465	2275	2465	2275	2465	mV
V_{OL}	Output LOW Voltage[1,2]	1375	1745	1400	1680	1400	1680	1400	1680	mV
V_{IH}	Input HIGH Voltage D,EN (EN-SEL open)[1]	2135	2560	2135	2560	2135	2560	2135	2560	mV
	Input HIGH Voltage EN (EN-SEL tied to V_{EE})[1]	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	mV
V_{IL}	Input LOW Voltage D,EN (EN-SEL open)[1]	1400	1825	1400	1825	1400	1825	1400	1825	mV
	Input LOW Voltage EN (EN-SEL tied to V_{EE})[1]	GND	800	GND	800	GND	800	GND	800	mV
V_{BB}	Reference Voltage[1]	1910	2050	1910	2050	1910	2050	1910	2050	mV
I_{IH}	Input HIGH Current EN[3]		150		150		150		150	µA
I_{IL}	Input LOW Current EN[3]	0.5		0.5		0.5		0.5		µA
I_{EE}	Power Supply Current[2]		48		48		48		48	mA

1 Voltage levels vary 1:1 with V_{CC}.

2 Specified with CS-SEL open.

3 Specified with EN-SEL open.

100K PECL DC Characteristics (VEE = GND, VCC = +5.0V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	3955	4165	3975	4165	3975	4165	3975	4165	mV
V_{OL}	Output LOW Voltage[1,2]	3075	3445	3100	3380	3100	3380	3100	3380	mV
V_{IH}	Input HIGH Voltage D,EN (EN-SEL open)[1]	3835	4260	3835	4260	3835	4260	3835	4260	mV
	Input HIGH Voltage EN (EN-SEL tied to V_{EE})[1]	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	mV
V_{IL}	Input LOW Voltage D,EN (EN-SEL open)[1]	3100	3525	3100	3525	3100	3525	3100	3525	mV
	Input LOW Voltage EN (EN-SEL tied to V_{EE})[1]	GND	800	GND	800	GND	800	GND	800	mV
V_{BB}	Reference Voltage[1]	3610	3750	3610	3750	3610	3750	3610	3750	mV
I_{IH}	Input HIGH Current EN[3]		150		150		150		150	µA
I_{IL}	Input LOW Current EN[3]	0.5		0.5		0.5		0.5		µA
I_{EE}	Power Supply Current[2]		48		48		48		52	mA

1 Voltage levels vary 1:1 with V_{CC}.

2 Specified with CS-SEL open.

3 Specified with EN-SEL open.

LVDS DC Characteristics for $Q_{HG}/\overline{Q}_{HG}$ Outputs[1] (V_{EE} = GND, V_{CC} = +3.0V to +5.5V)

Symbol	Characteristic	-40□C		0□C		25□C		85□C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage		1600		1600		1600		1600	mV
V_{OL}	Output LOW Voltage	900		900		900		900		mV
V_{OC}	Output Common Mode Voltage[2]	1125	1375	1125	1375	1125	1375	1125	1375	mV
□V_{OC}	Change in Common Mode Voltage[3]	-50	50	-50	50	-50	50	-50	50	mV
V_{OUT}	Single-Ended Output Swing	250	450	250	450	250	450	250	450	mV
V_{DIFF_OUT}	Differential Output Swing	500	900	500	900	500	900	500	900	mV

1 Specified with 100Ω resistor connecting Q_{HG} and $\overline{Q}_{HG}$ together.

2 Common mode voltage is the center voltage between Q_{HG} and $\overline{Q}_{HG}$ during a steady state.

3 Change in common mode voltage is the difference between common mode voltages at opposite binary states.

AC Characteristics (V_{EE} = -3.0V to -5.5V; V_{CC}=GND or V_{EE}=GND; V_{CC} = +3.0V to +5.5V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}/t_{PHL}	Propagation Delay													
	D to Q/$\overline{Q}$[1]			400			400			400			430	ps
	D to $Q_{HG}/\overline{Q}_{HG}$[2]			550			550			550			630	ps
t_{SKEW}	Duty Cycle Skew[3]		5	20		5	20		5	20		5	20	ps
V_{PP} (AC)	Input Swing[4]	80		1000	80		1000	80		1000	80		1000	mV
t_r/t_f	Output Rise/Fall[1] (20% - 80%) - Q	100		260	100		260	100		260	100		260	
	Output Rise/Fall[1] (20% - 80%) - Q_{HG}	180		280	180		280	180		280	180		280	ps

1 Specified with CS-SEL connected to V_{EE} and Q/$\overline{Q}$ with AC coupled 50Ω loads.

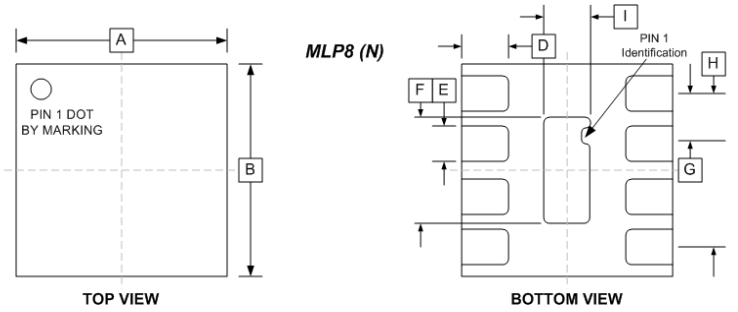
2 Specified with 100Ω resistor connecting Q_{HG} and $\overline{Q}_{HG}$ together.

3 Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

4 The peak-to-peak differential input swing is the range for which AC parameters guaranteed. V_D and V must remain within the range of ±750 mV with respect to V_{BB}.

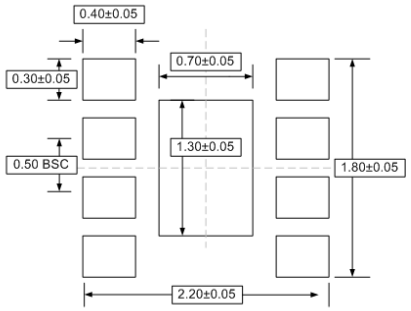
Package Dimensions

MLP8 (N)

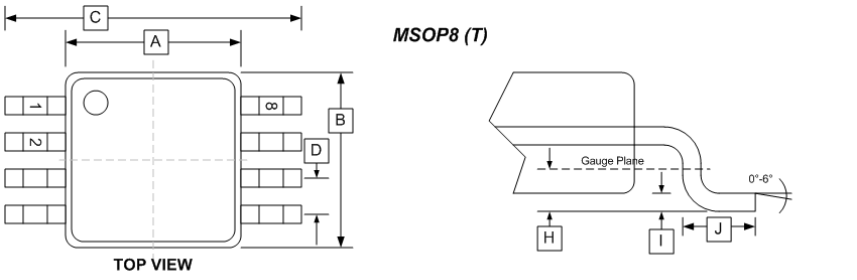


	MILLIMETERS	
DIM	MIN	MAX
A	2.00±0.050	
B	2.00±0.050	
C	0.75±0.050	
C_1	0.00	0.05
C_2	0.203 Ref.	
D	0.35±0.050	
E	0.25±0.050	
F	1.20±0.050	
G	0.500 BSC	
H	1.500 REF	
I	0.60±0.050	

PCB LAND PATTERN/FOOTPRINT

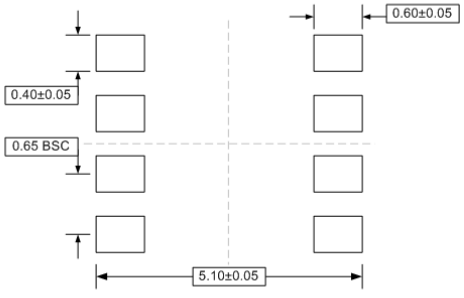


MSOP8 (T)



	INCHES	
DIM	MIN	MAX
A	0.118±0.004	
B	0.118±0.004	
C	0.192±0.008	
D	0.0256 TYP	
E	0.004±0.002	
F	0.034±0.002	
G	0.009±0.014	
H	0.010	
I	0.006±0.002	
J	0.021±0.004	

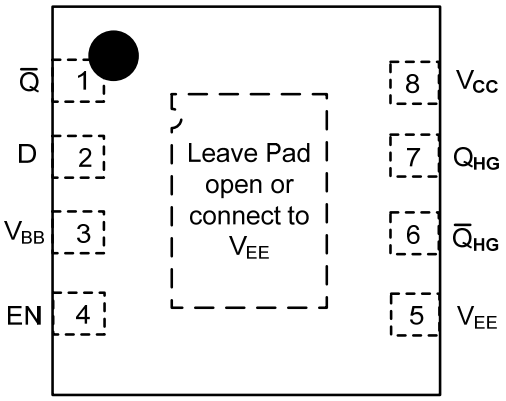
PCB LAND PATTERN/FOOTPRINT
Dimensions in mm



Pin Description and Configuration

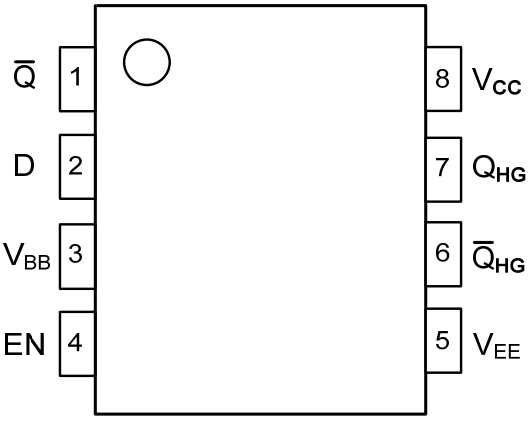
Pin Assignments for CTSLV399NG

Pin	Name	Type	Function
1	$\overline{Q}$	Output	Inverting PECL Output
2	D	Input	Data Input
3	V_{BB}	Output	Reference Voltage
4	EN	Input	Output Enable
5	V_{EE}	Power	Negative Supply
6	$\overline{Q}_{HG}$	Output	Inverting LVDS Output
7	Q_{HG}	Output	LVDS Output
8	V_{CC}	Power	Positive Supply



Pin Assignments for CTSLV399TG

Pin	Name	Type	Function
1	$\overline{Q}$	Output	Inverting PECL Output
2	D	Input	Data Input
3	V_{BB}	Output	Reference Voltage
4	EN	Input	Output Enable
5	V_{EE}	Power	Negative Supply
6	$\overline{Q}_{HG}$	Output	Inverting LVDS Output
7	Q_{HG}	Output	LVDS Output
8	V_{CC}	Power	Positive Supply



Part Ordering Information:

Part Number	Package	Marking
CTSLV399NG	MLP8	V1G / YWW
CTSLV399TG	MSOP8	HV99G / YYWW