Model 656P/L

Advanced PLL LVPECL or LVDS Clock

Features

- Ceramic Surface Mount Package
- Low Phase Jitter Performance, 600fs Typical
- Advanced PLL Design w/ Low Fundamental Crystal
- Frequency Range 10MHz – 1.0GHz *
- +2.5V or +3.3V Operation
- Output Enable Standard
- Tape and Reel Packaging, EIA-418

Part Dimensions:
7.0 × 5.0 × 2.0mm • 178.462mg

Standard Frequencies

- 20.00MHz	- 161.1328MHz
- 25.00MHz	- 200.00MHz
- 27.00MHz	- 204.80MHz
- 122.88MHz	- 250.00MHz
- 125.00MHz	- 312.50MHz
- 148.351648MHz	- 622.08MHz
- 155.52MHz	- 693.4830MHz
- 156.253906MHz	- 983.04MHz

* Check with factory for availability.

Applications

- Broadcast Video
- Storage Area Networking
- Broadband Access
- PCI Express
- Networking Equipment
- Ethernet/GbE/SyncE
- Fiber Channel
- Test and Measurement

Description

CTS Model 656P/L is a low cost, high performance PLL clock oscillator supporting differential LVPECL or LVDS outputs. Employing the latest IC technology, M656P/L has excellent stability and low phase jitter performance.

Ordering Information

Model	Output Type	Frequency Code [MHz]	Frequency Stability	Temperature Range	Supply Voltage	Packaging
656	P	XXX or XXXX	3	I	3	T

Code	Frequency
Product Frequency Code [1]	

Code	Temp. Range
C	-20°C to +70°C
I	-40°C to +85°C

Code	Packing
T	1k pcs./reel

Code	Output
P	LVPECL
L	LVDS

Code	Stability
6	±20ppm [2]
5	±25ppm
3	±50ppm

Code	Voltage
2	+2.5Vdc
3	+3.3Vdc

Notes:

1] Refer to document 016-1454-0, Frequency Code Tables.
3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.

2] Consult factory for availability of 6I Stability/Temperature combination.

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.

Electrical Specifications

Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.5	-	5.0	V
Supply Voltage	V_{CC}	±5%	2.375 3.135	2.5 3.3	2.625 3.465	V
Supply Current						
LVPECL	I_{CC}	Maximum Load	-	54	-	mA
LVDS			-	23	-	
Operating Temperature	T_A	-	-20 -40	+25	+70 +85	°C
Storage Temperature	T_{STG}	-	-55	-	+125	°C

Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range	f_O	-		10 - 1000		MHz
Frequency Stability [Note 1]	$\Delta f/f_O$	-		20, 25 or 50		±ppm
Aging	$\Delta f/f_{25}$	First Year @ +25°C, nominal V_{CC}	-3	-	3	ppm

1] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		LVPECL		-
Output Load	R_L	Terminated to V_{CC} - 2.0V	-	50	-	Ohms
Output Voltage Levels	V_{OH} V_{OL}	PECL Load	V_{CC} - 1.03 V_{CC} - 1.85	- -	V_{CC} - 0.60 V_{CC} - 1.60	V
Output Duty Cycle	SYM	@ V_{CC} - 1.3V	45	-	55	%
Rise and Fall Time	T_R, T_F	@ 20%/80% Levels, R_L = 50 Ohms	-	0.25	0.60	ns

Output Type	-	-		LVDS		-
Output Load	R_L	Between Outputs	-	100	-	Ohms
Output Voltage Levels	V_{OH} V_{OL}	LVDS Load	- 0.90	1.43 1.10	1.60 -	V
Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
Differential Output Voltage	V_{OD}	R_L = 100 Ohms	175	350	454	mV
Offset Voltage	V_{OS}	LVDS Load	1.20	1.25	1.30	V
Rise and Fall Time	T_R, T_F	@ 20%/80% Levels, R_L = 100 Ohms	-	-	0.4	ns

Electrical Specifications

Output Parameters

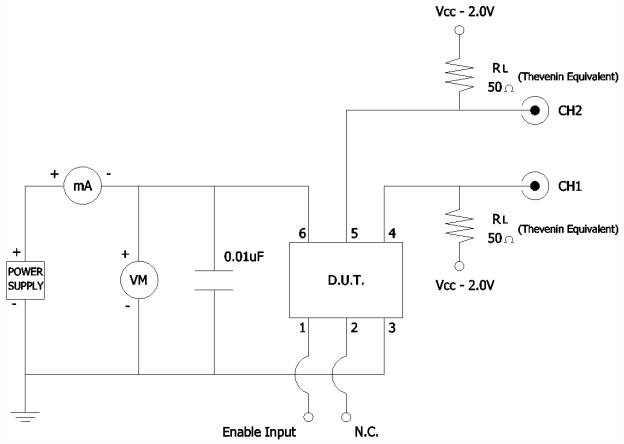
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Start Up Time	T_S	Application of V_{CC}	-	3	5	ms
Enable Function [Standby]						
Enable Input Voltage	V_{IH}	Pin 1 Logic '1', Output Enabled	$0.7V_{CC}$	-	-	V
Disable Input Voltage	V_{IL}	Pin 1 Logic '0', Output Disabled	-	-	$0.3V_{CC}$	V
Disable Current	I_{IL}	Pin 1 Logic '0', Output Disabled	-	-	20	uA
Enable Time	T_{PLZ}	Pin 1 Logic '1', Output Enabled	-	-	5	ns
Phase Jitter, RMS	tjrms	Bandwidth 12 kHz - 20 MHz	-	600	<1000	fs
Period Jitter, pk-pk	pjpk-pk	-	-	2.5	-	ps
Period Jitter, RMS	pjrms	-	-	25	-	ps

Enable Truth Table

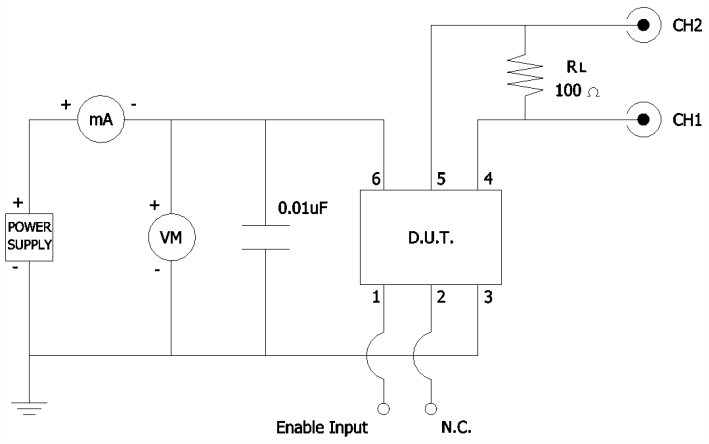
Pin 1	Pin 4 & Pin 5
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

Test Circuit

LVPECL

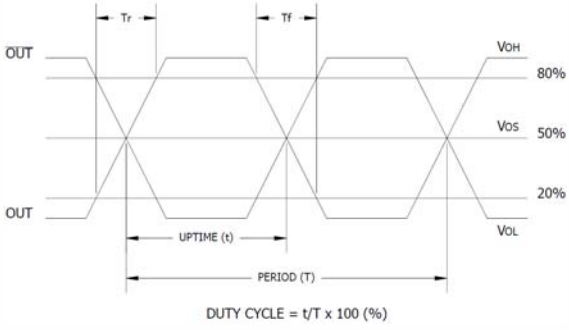


LVDS



Output Waveform

LVPECL or LVDS

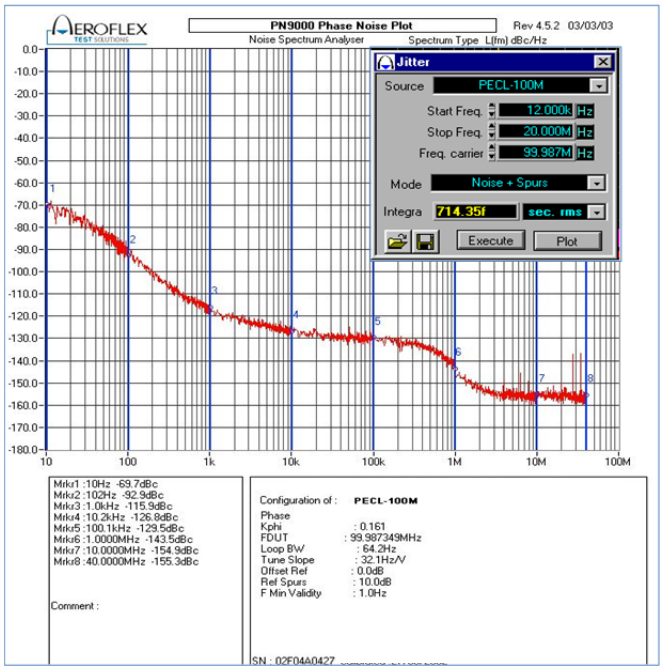


Electrical Specifications

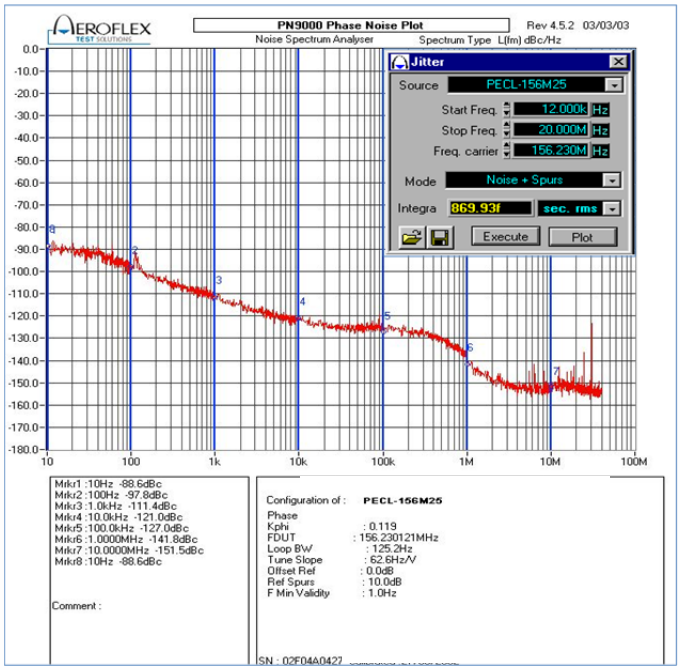
Performance Data

Phase Noise [typical]

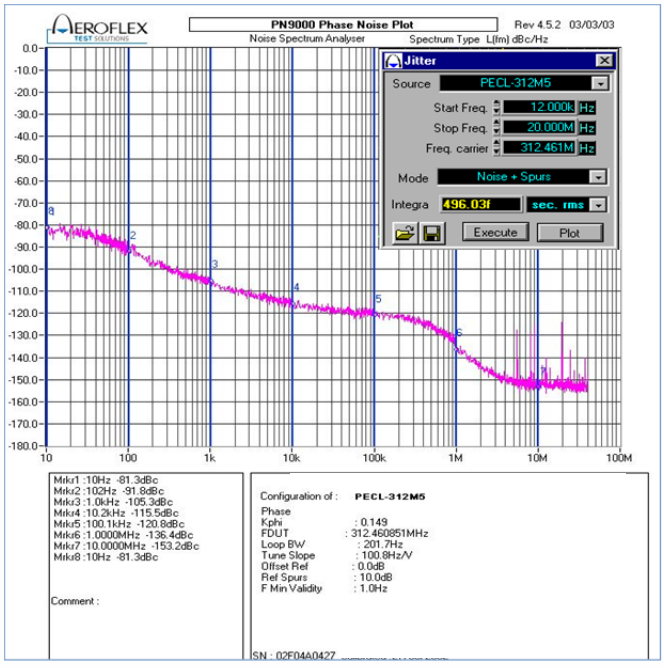
100.00MHz, LVPECL, V_{CC} = 3.3V, T_A = +25°C



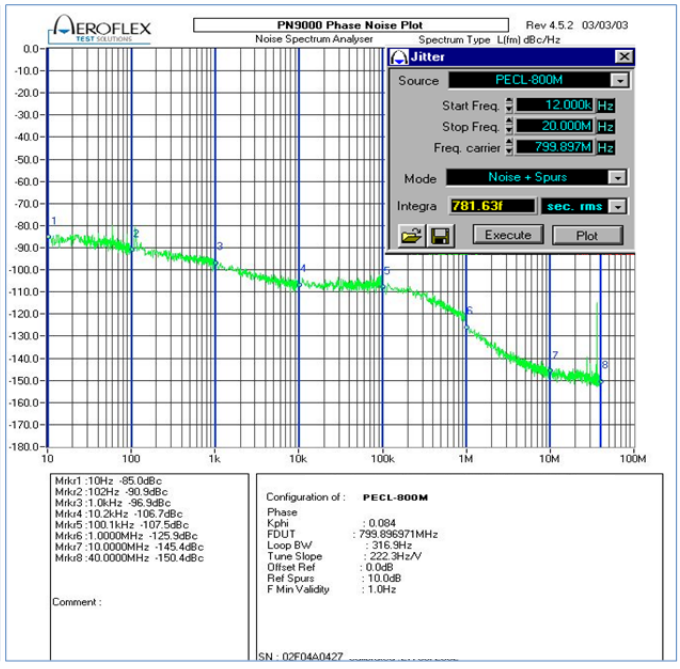
156.25MHz, LVPECL, V_{CC} = 3.3V, T_A = +25°C



312.50MHz, LVPECL, V_{CC} = 3.3V, T_A = +25°C



800.00MHz, LVPECL, V_{CC} = 3.3V, T_A = +25°C



Electrical Specifications

Performance Data

Phase Noise Tabulated

Typical, HCMOS, V_{CC} = 3.3V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 100.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-69.70	
		@ 100Hz	-92.90	
		@ 1kHz	-115.90	
	-	@ 10kHz	-126.80	dBc/Hz
		@ 100kHz	-129.50	
		@ 1MHz	-143.50	
		@ 10MHz	-154.90	
		@ 40MHz	-155.30	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	714.35	fs

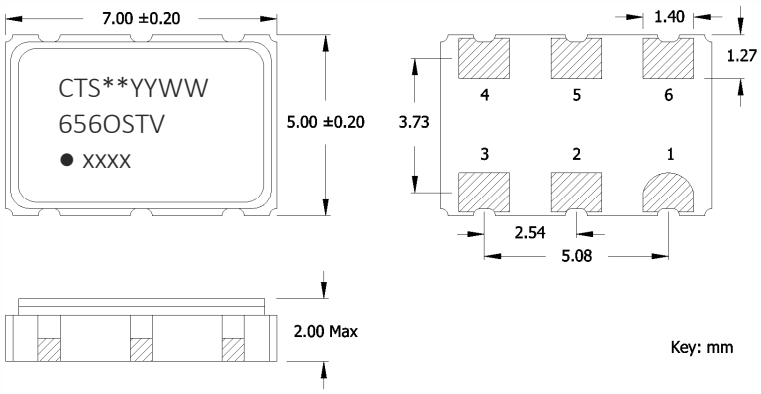
PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 156.25MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-88.60	
		@ 100Hz	-97.80	
		@ 1kHz	-111.40	
	-	@ 10kHz	-121.00	dBc/Hz
		@ 100kHz	-127.00	
		@ 1MHz	-141.80	
		@ 10MHz	-151.50	
		@ 40MHz	-153.30	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	869.93	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 312.50MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-81.30	
		@ 100Hz	-91.80	
		@ 1kHz	-105.30	
	-	@ 10kHz	-115.50	dBc/Hz
		@ 100kHz	-120.80	
		@ 1MHz	-136.40	
		@ 10MHz	-153.20	
		@ 40MHz	-153.20	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	496.03	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 800.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-85.00	
		@ 100Hz	-90.90	
		@ 1kHz	-96.90	
	-	@ 10kHz	-106.70	dBc/Hz
		@ 100kHz	-107.50	
		@ 1MHz	-125.90	
		@ 10MHz	-145.40	
		@ 40MHz	-150.40	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	781.63	fs

Mechanical Specifications

Package Drawing

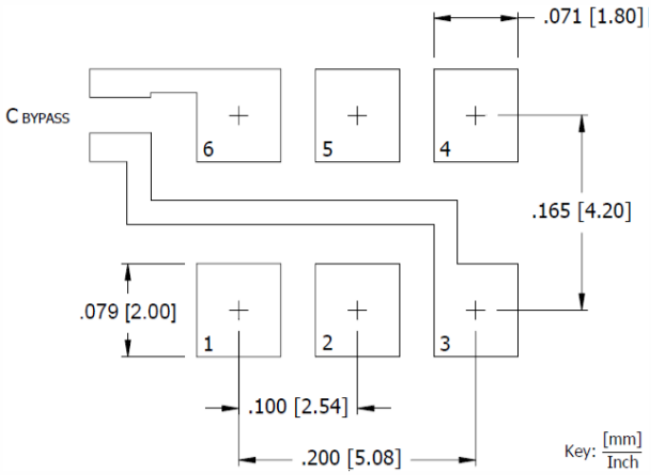


Marking Information

1. ** - Manufacturing Site Code.
2. YYWW – Date Code; YY – year, WW – week.
3. O – Output Type; P = LVPECL, L = LVDS.
4. ST – Frequency Stability/Temperature Code. [Refer to Ordering Information]
5. V – Voltage Code; 3 = 3.3V, 2 = 2.5V.
6. xxxx – Frequency Code.
   3-digits, frequencies below 100MHz
   4-digits, frequencies 100MHz or greater

[See document 016-1454-0, Frequency Code Tables.]

Recommended Pad Layout



Notes

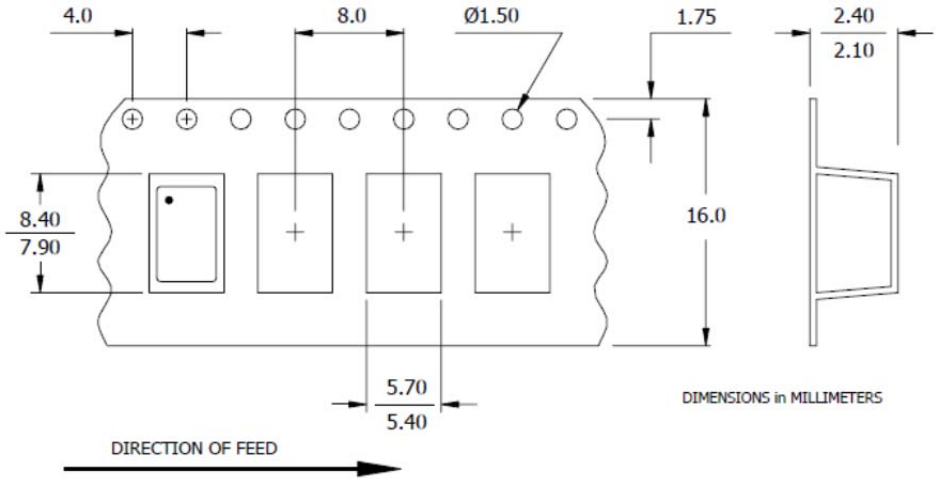
1. JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
3. MSL = 1.

Pin Assignments

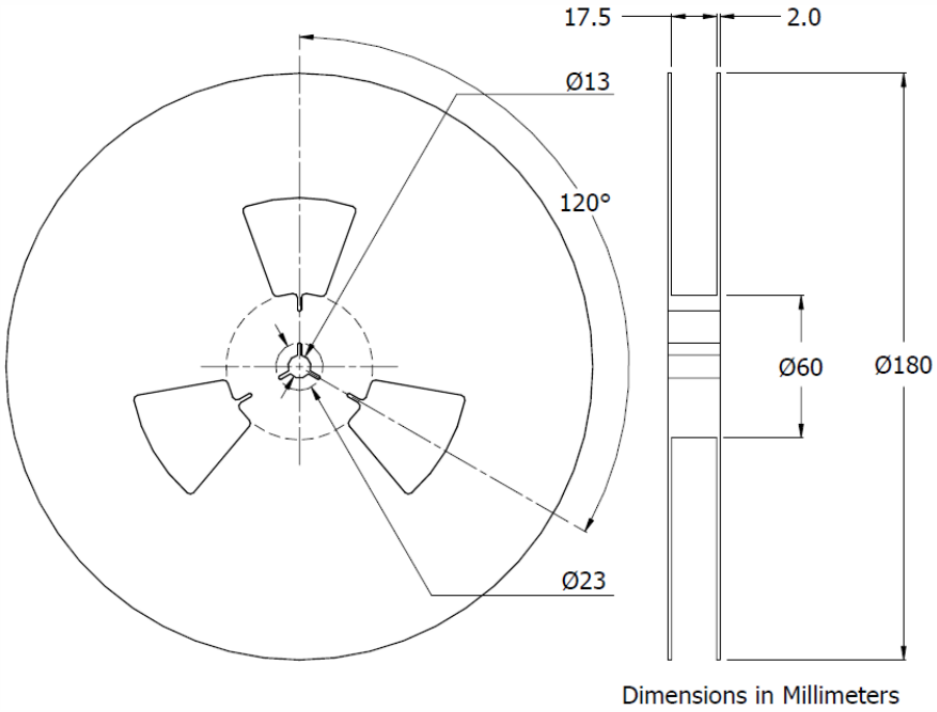
Pin	Symbol	Function
1	EOH	Enable
2	N.C.	No Connect
3	GND	Circuit & Package Ground
4	Output	RF Output
5	$\overline{\text{Output}}$	Complimentary RF Output
6	V_{CC}	Supply Voltage

Packaging - Tape and Reel

Tape Drawing



Reel Drawing



Notes

1. Device quantity is 1k pieces maximum per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.