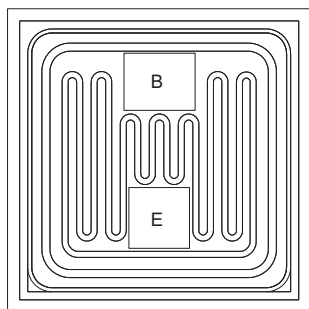


CP710V-MPSA92

PNP - High Voltage Transistor Die

The CP710V-MPSA92 is a silicon PNP transistor designed for high voltage applications.



BACKSIDE COLLECTOR R2

MECHANICAL SPECIFICATIONS:

Die Size	26 x 26 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Size	6.1 x 4.9 MILS
Emitter Bonding Pad Size	5.2 x 5.2 MILS
Top Side Metalization	Al – 30,000Å
Back Side Metalization	Au – 9,000Å
Scribe Alley Width	2.2 MILS
Wafer Diameter	5 INCHES
Gross Die Per Wafer	25,214

MAXIMUM RATINGS: ($T_A=25^{\circ}\text{C}$)

	SYMBOL		UNITS
Collector-Base Voltage	V_{CBO}	300	V
Collector-Emitter Voltage	V_{CEO}	300	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Continuous Collector Current	I_C	500	mA
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS: ($T_A=25^{\circ}\text{C}$)

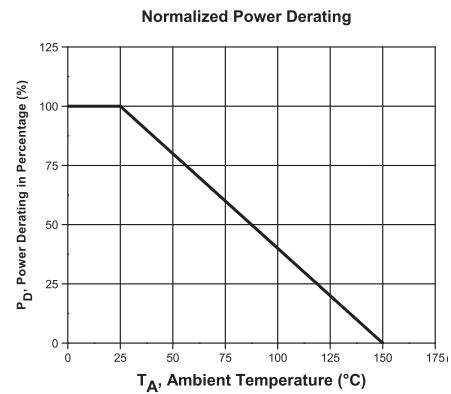
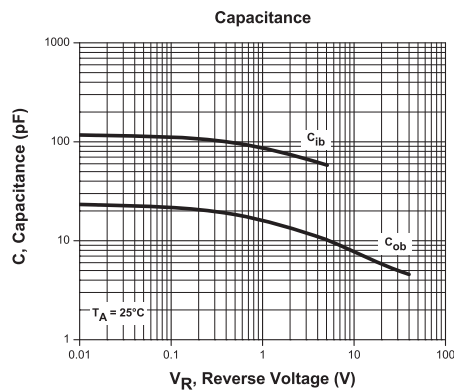
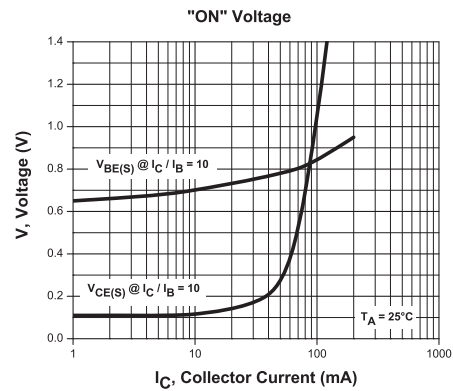
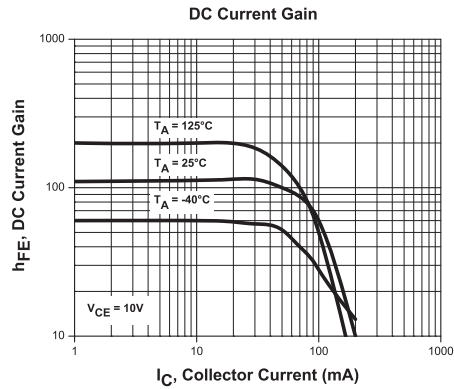
SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{CBO}	$V_{CB}=200\text{V}$		250	nA
I_{EBO}	$V_{EB}=3.0\text{V}$		100	nA
BV_{CBO}	$I_C=100\mu\text{A}$	300		V
BV_{CEO}	$I_C=1.0\text{mA}$	300		V
BV_{EBO}	$I_E=100\mu\text{A}$	5.0		V
$V_{CE(SAT)}$	$I_C=20\text{mA}, I_B=2.0\text{mA}$		0.5	V
$V_{BE(SAT)}$	$I_C=20\text{mA}, I_B=2.0\text{mA}$		0.9	V
h_{FE}	$V_{CE}=10\text{V}, I_C=1.0\text{mA}$	25		
h_{FE}	$V_{CE}=10\text{V}, I_C=10\text{mA}$	40		
h_{FE}	$V_{CE}=10\text{V}, I_C=30\text{mA}$	25		
f_T	$V_{CE}=20\text{V}, I_C=10\text{mA}, f=100\text{MHz}$	50		MHz
C_{ob}	$V_{CB}=20\text{V}, I_E=0, f=1.0\text{MHz}$		6.0	pF

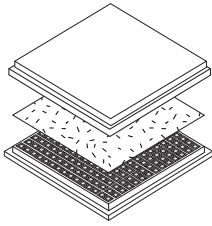
PACKING OPTIONS:

- CP710V-MPSA92-CT: Singulated die in waffle pack; 400 die per tray.
- CP710V-MPSA92-WN: Full wafer, unsawn, 100% tested with reject die inked.
- CP710V-MPSA92-WR: Full wafer, sawn and mounted on plastic ring, 100% tested with reject die inked.

CP710V-MPSA92

Typical Electrical Characteristics

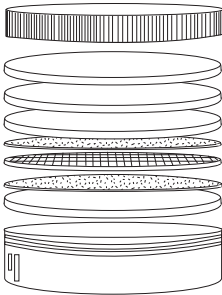




BARE DIE IN TRAY (WAFFLE) PACK

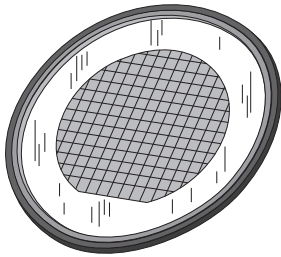
CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



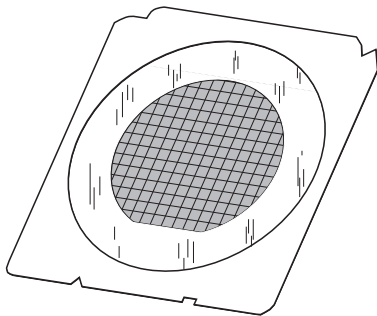
UNSAWN WAFER

WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)



SAWN WAFER ON METAL FRAME

WS: Full wafer, sawn and mounted on metal frame, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WS)

PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

CONTACT US

Corporate Headquarters & Customer Support Team

Central Semiconductor Corp.
145 Adams Avenue
Hauppauge, NY 11788 USA
Main Tel: (631) 435-1110
Main Fax: (631) 435-1824
Support Team Fax: (631) 435-3388
www.centrasemi.com

Worldwide Field Representatives:
www.centrasemi.com/wwreps

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