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CS5321

High Dynamic Range Delta-Sigma Modulator

Features

- Delta-Sigma Architecture
  - Fourth-Order Modulator
  - Variable Sample Rate
  - Internal Track-and-Hold Amplifier
- Clock Jitter Tolerant Architecture
- Dynamic Range
  - 121 dB @ 411 Hz Bandwidth
  - 118 dB @ 822 Hz Bandwidth
- Signal-to-Distortion: 115 dB
- Input Range: ±4.5 V
- Improved offset drift, gain drift, and clock jitter immunity over CS5323

Description

The CS5321 is a high dynamic range, fourth-order delta-sigma modulator intended for geophysical and sonar applications. Used in combination with the CS5322 digital FIR filter, a unique high resolution A/D system results.

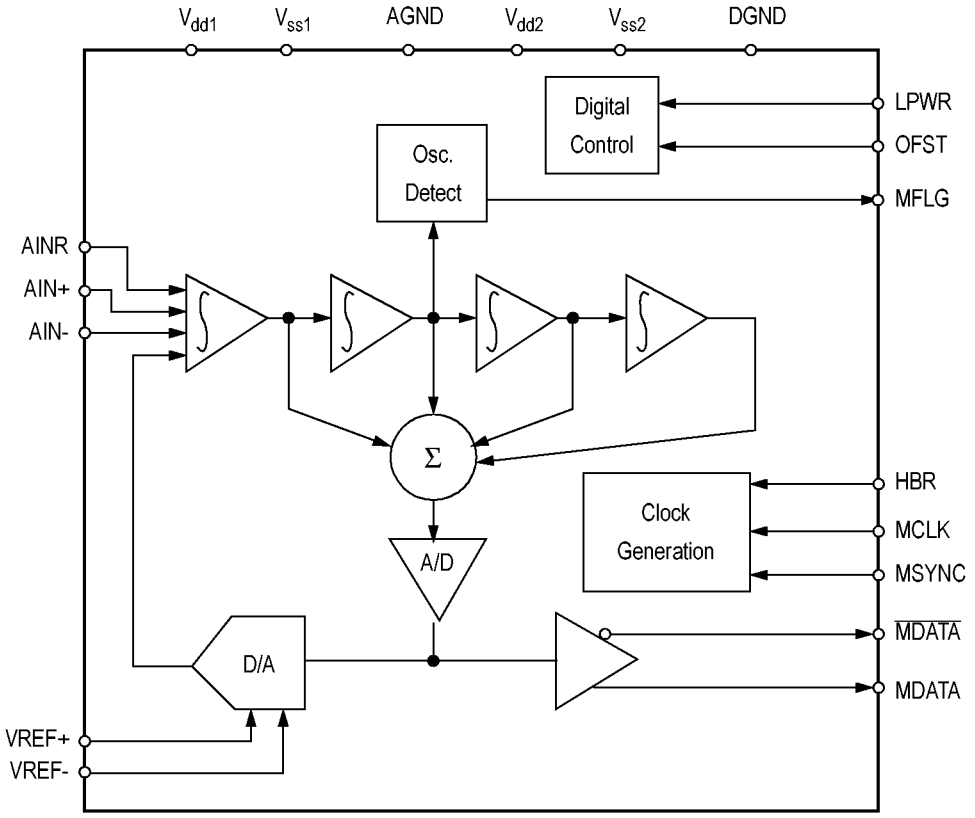
The CS5321 provides an oversampled serial bit stream at 256 kbits per second (HBR=1) and 128 kbits per second (HBR=0) operating with a clock rate of 1.024 MHz.

The monolithic CMOS design of the CS5321 insures high reliability while minimizing power dissipation.

The CS5321 can be operated in two power modes. In Normal mode (LPWR=0) power dissipation is 55 mW. In Low Power mode (LPWR=1) power dissipation is 30 mW.

ORDERING INFORMATION

CS5321-BL -55° to +85° C 28-pin PLCC



Cirrus Logic, Inc.
Crystal Semiconductor Products Division
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.crystal.com

ANALOG CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; V_{ss1}, V_{ss2} = -5V; V_{dd1}, V_{dd2} = 5V; GND=0V; MCLK=1.024 MHz; HBR=V_{dd}; LPWR=0; Device is connected as shown in Figure 3, the System Connection Diagram; unless otherwise specified. (Note 1))

Parameter*		Symbol	Min	Typ	Max	Units
Specified Temperature Range			-55	-	+85	°C
Dynamic Performance						
Dynamic Range	(Note 1)	DR				
HBR = 1:	fo = 4000 Hz		-	103	-	dB
OFST =1	fo = 2000 Hz		-	118	-	dB
	fo = 1000 Hz		116	121	-	dB
	fo = 500 Hz		-	124	-	dB
	fo = 250 Hz		-	127	-	dB
	fo = 125 Hz		-	129	-	dB
	fo = 62.5 Hz		-	130	-	dB
HBR = 0:	fo = 2000 Hz		-	99	-	dB
OFST = 1	fo = 1000 Hz		-	118	-	dB
	fo = 500 Hz		-	121	-	dB
	fo = 250 Hz		-	124	-	dB
	fo = 125 Hz		-	127	-	dB
	fo = 62.5 Hz		-	129	-	dB
	fo = 31.25 Hz		-	130	-	dB
Signal-to-Distortion:	MCLK = 1.024 MHz (Note 2)	SDR				
	HBR = 1		100	115	-	dB
	HBR = 0		110	120	-	dB
Intermodulation Distortion	(Note 3)	IMD	-	110	-	dB
dc Accuracy						
Full Scale Error	(Note 4)	FSE	-	1	-	%
Full Scale Drift	(Notes 4, 5)	TC_{FS}	-	5	-	ppm/°C
Offset	(Note 4)	V_{ZSE}	-	10	-	mV
Offset after Calibration	(Note 6)		-	±100	-	µV
Offset Calibration Range	(Note 7)		-	100	-	%F.S.
Offset Drift	(Note 4, 5)	TC_{ZSE}	-	60	-	µV/°C

Notes:
1. fo = CS5322 output word rate. Refer to the CS5322/CS5323 data sheet for details on the CS5322 FIR Filter.
2. Tested with full scale input signal of 50 Hz; f_{OWR} = 500 Hz; OFST = 0 or OFST = 1.
3. Tested with input signals of 30 Hz and 50 Hz, each 6 dB down from full scale f_{OWR} = 1000 Hz.
4. Specification is for the parameter over the specified temperature range and is for the CS5321 device only (VREF=+4.5V). It does not include the effects of external components, OFST = 0.
5. Drift specifications are guaranteed by design and/or characterization.
6. The offset after calibration specification applies to the effective offset voltage for a ± 4.5 volt input to the CS5321 modulator, but is relative to the output digital codes from the CS5322 after ORCAL and USEOR have been made active.
7. The CS5322 offset calibration is performed digitally and includes ± full scale (± 4.5 volts into CS5321). Calibration of offsets greater than ±5% of full scale will begin to subtract from the dynamic range.

* Refer to Parameter Definitions (immediately following pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter*		Symbol	Min	Typ	Max	Units
Specified Temperature Range			-55	-	+85	°C
Input Characteristics						
Input Signal Frequencies	(Note 8)	BW	dc	-	1500	Hz
Input Voltage Range	(Note 9)	V_{IN}	-4.5	-	+4.5	V
Input Overrange Voltage Tolerance	(Note 9)	I_{OVR}	-	-	5	%F.S.
Power Supplies						
DC Power Supply Currents	(Note 10)					
LPWR = 0	Positive Supplies		-	5.5	7.5	mA
	Negative Supplies		-	5.5	7.5	mA
LPWR = 1	Positive Supplies		-	3.0	4.5	mA
	Negative Supplies		-	3.0	4.5	mA
Power Consumption	(Note 10)					
Normal Operating Mode	(Note 11)	P_{DN}	-	55	75	mW
Lower Power Mode	(Note 12)	P_{DL}	-	30	45	mW
Power Down		P_D	-	2	-	mW
Power Supply Rejection	(dc to 128 kHz)(Notes 13, 14)	PSR	-	60	-	dB

Notes:
8. The upper bandwidth limit is determined by the CS5322 digital filter.
9. This input voltage range is for the configuration depicted in Figure 3, the System Connection Diagram, and applies to signal from dc to f3 Hz. Refer to CS5322 Filter Characteristics for the values of f3.
10. All outputs unloaded. All logic inputs forced to V_{dd} or GND respectively.
11. LPWR=0
12. The CS5321 power dissipation can be reduced under the following conditions:
    a) LPWR=1; MCLK=512kHz, HBR=1
    b) LPWR=1; MCLK=1.024MHz, HBR=0
13. Tested with a 100 mVp-p sine wave applied separately to each supply.
14. Refer to the CS5322/CS5323 Data Sheet for values of the Filter Characteristics of the CS5322.

* Refer to Parameter Definitions (immediately following pin descriptions at the end of this data sheet).

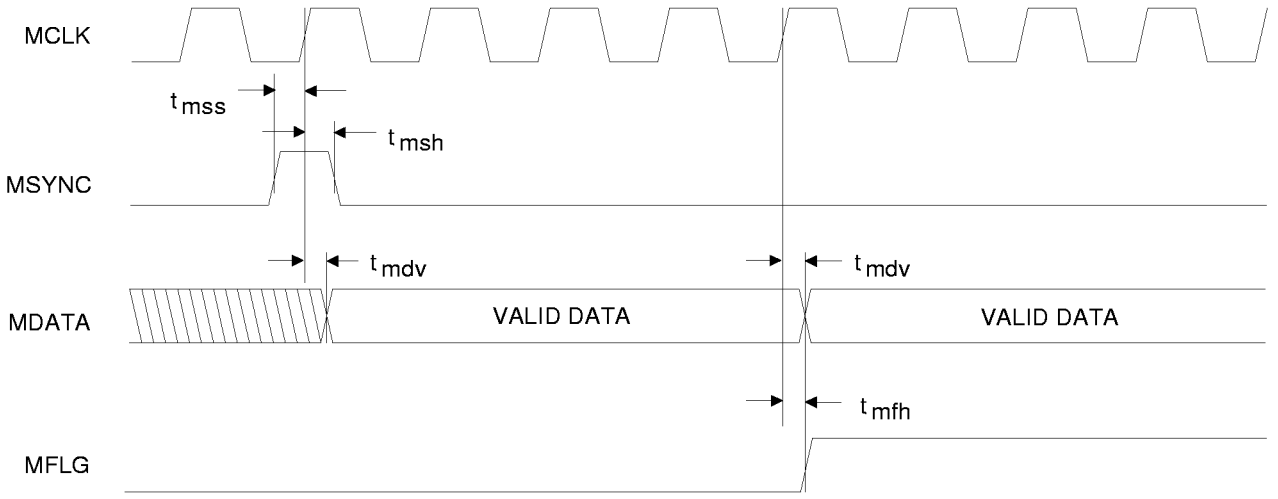
Specifications are subject to change without notice.

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; V_{dd1}, V_{dd2} = 5V±5%; V_{ss1}, V_{ss2} = -5V±5%; Inputs: Logic 0 = 0V Logic 1 = V+; C_L = 50 pF (Note 15))

Parameter			Symbol	Min	Typ	Max	Units
MCLK Frequency		(Note 16)	f_c	0.250	1.024	1.2	MHz
MCLK Duty Cycle				40	-	60	%
MCLK Jitter (In-band)				-	-	300	ps
Rise Times:	Any Digital Input	(Note 17)	t_{risein}	-	-	100	ns
	Any Digital Output		$t_{riseout}$	-	50	200	ns
Fall Times:	Any Digital Input	(Note 17)	t_{fallin}	-	-	100	ns
	Any Digital Output		$t_{fallout}$	-	50	200	ns
MSYNC Setup Time to MCLK rising			t_{mss}	20	-	-	ns
MSYNC Hold Time after MCLK rising			t_{msh}	20	-	-	ns
MCLK rising to Valid MFLG			t_{mfh}	-	140	255	ns
MCLK rising to Valid MDATA			t_{mdv}	-	170	300	ns

Notes: 15. Guaranteed by design, characterization, or test.
16. If MCLK is removed, the CS5321 will enter a power down state.
17. Excludes MCLK input, MCLK should be driven with a signal having rise/fall times of 25ns or faster.

Rise and Fall Times



CS5321 Interface Timing, HBR=1

DIGITAL CHARACTERISTICS (T_A = T_{min} to T_{max}; V_{dd1} = V_{dd2} = 5V±5%; GND = 0V; measurements performed under static conditions)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Drive Voltage	(Note 18)	V_{IH}	(V_{dd})-0.6	-	-	V
Low-Level Input Drive Voltage	(Note 18)	V_{IL}	-	-	1.0	V
High-Level Output Voltage I_{OUT} = -40 µA	(Note 19)	V_{OH}	(V_{dd})-0.3	-	-	V
Low-Level Output Voltage I_{OUT} = +40 µA	(Note 19)	V_{OL}	-	-	0.3	V
Input Leakage Current		I_{LKG}	-	-	±10	µA
Digital Input Capacitance		C_{IN}	-	9	-	pF
Digital Output Capacitance		C_{OUT}	-	9	-	pF

Notes: 18. Device is intended to be driven with CMOS logic levels.
19. Device is intended to be interfaced to CMOS logic. Resistive loads are not recommended on these pins.

RECOMMENDED OPERATING CONDITIONS (GND=0V, see Note 20)

Parameter		Symbol	Min	Typ	Max	Units
DC Supply:	Positive	V_{dd1}, V_{dd2}	4.75	5.0	5.25	V
	Negative	V_{ss1}, V_{ss2}	-4.75	-5.0	-5.25	V
Ambient Operating Temperature		T_A	-55	-	+85	°C

Notes: 20. All voltages with respect to ground.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply:	Positive	V_{dd1}, V_{dd2}	-0.3	6.0	V
	Negative	V_{ss1}, V_{ss2}	+0.3	-6.0	V
Input Current, Any Pin Except Supplies	(Note 21)	I_{in}	-	±10	mA
Output Current		I_{out}	-	25	mA
Total Power (all supplies and outputs)		P_t	-	1	W
Digital Input Voltage		V_{IND}	-0.3	(V_{dd})+0.3	V
Storage Temperature		T_{stg}	-65	150	°C

Notes: 21. Transient currents of up to 100 mA will not cause SCR latch up.

*WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

GENERAL DESCRIPTION

The CS5321 is a fourth-order CMOS monolithic analog modulator designed specifically for very high resolution measurement of signals between dc and 1500 Hz. Configuring the CS5321 with the CS5322 FIR filter results in a high resolution A/D converter system that performs sampling and A/D conversion with dynamic range exceeding 120 dB (Refer to the CS5322/CS5323 data sheet for specific details on the CS5322).

The CS5321 utilizes a fourth-order oversampling architecture to achieve high resolution A/D conversion. The modulator consists of a 1-bit A/D converter embedded in a negative feedback loop. The modulator provides an oversampled serial bit stream at 256 kbits per second (HBR=1) and 128 kbits per second (HBR=0) operating with a clock rate of 1.024 MHz.

The CS5321 offers improved performance, lower power consumption, and greater tolerance to clock jitter than the CS5323.

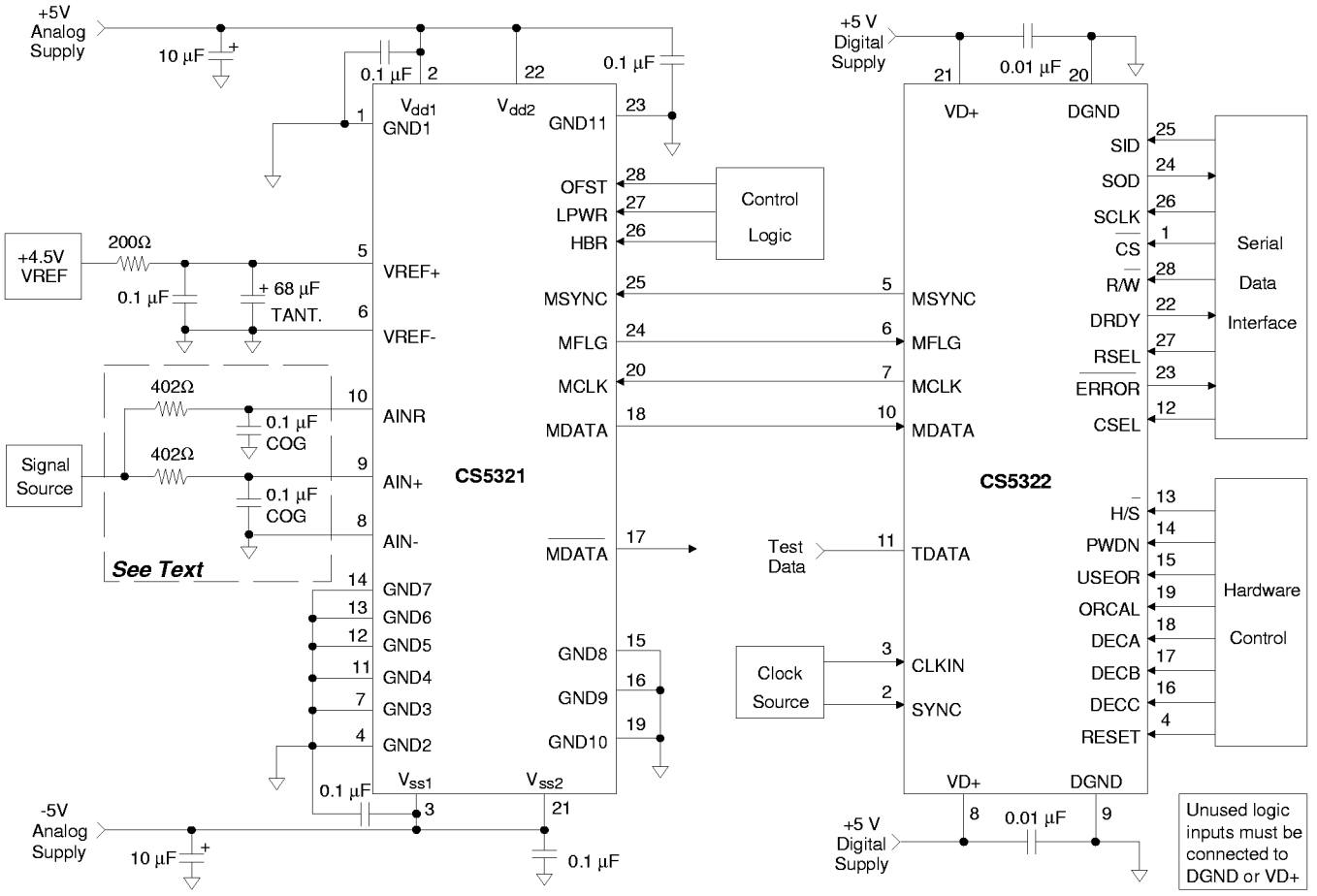


Figure 1. System Connection Diagram

Analog Input

The CS5321 A/D converter uses a switched capacitor architecture for its signal and voltage reference inputs. The signal input uses three pins; AINR, AIN+, and AIN-. The AIN- pin acts as the return pin for the AINR and AIN+ pins. The AINR pin is a switched capacitor "rough charge" input for the AIN+ pin. The input impedance for the rough charge pin (AINR) is 1/fC where f is the two times the modulator sampling clock rate and C is the internal sampling capacitor (about 40 pF). Using a 1.024 MHz master clock (HBR =1) yields an input impedance of about 1/(512 kHz)X(40pF) or about 50 kohms. Internal to the chip the rough charge input precharges the sampling capacitor used on the AIN+ input, therefore the effective input impedance on the AIN+ pin is orders of magnitude above the impedance seen on the AINR pin.

The analog input structure inside the VREF+ pin is very similar to the AINR pin but includes additional circuitry whose operating current can change over temperature and from device to device. Therefore, if gain accuracy is important, the VREF+ pin should be driven from a low source impedance. The current demand of the VREF+ pin will produce a voltage drop of approximately 45 mV across the 200 ohm source resistor of Figure 2-A with MCLK = 1.024 MHz, HBR = 1, and temperature = 25°C.

When the CS5321 modulator is operated with a 4.5 V reference it will accept a 9 V p-p input signal, but modulator loop stability can be adversely affected by high frequency out-of-band signals. Therefore, input signals must be bandlimited by an input filter. The -3 dB corner of the input filter must be equal to the modulator sampling clock divided by 64. The modulator sampling clock is MCLK/4 when HBR = 1 or MCLK/8 when HBR =0. With MCLK =1.024 MHz, HBR = 1, the modulator sampling clock is 256 kHz which requires an input filter with a -3 dB corner of 4 kHz. The bandlimiting may be accomplished in an amplifier stage ahead of the CS5321 modulator or with the RC input filter at the AIN+ and AINR input pins. The RC filter at the AIN+ and AINR pins is recommended to reduce the "charge kick" that the driving amplifier sees as the switched capacitor sampling is performed.

Figure 1 illustrates the CS5321/ CS5322 system connections. The input components on AINR and AIN+ should be identical values for optimum performance. In choosing the components the capacitor should be a minimum of 0.1 uF (C0G dielectric ceramic preferred). For minimum board space, the RC components on the AINR input can be removed, but this will force the driving amplifier to source the full dynamic charging current of the AINR input. This can increase distortion in the driving amplifier and reduce system performance. In choosing the RC filter components, increasing C and minimizing R is preferred. Increasing C reduces the instantaneous voltage change on the pin, but may require paralleling capacitors to maintain smaller size (the recommended 0.1 µF C0G ceramic capacitor is larger than other similar-valued capacitors with different dielectrics). Larger resistor values will increase the voltage drop across the resistor as the recharging current charges the switched capacitor input.

The OFST Pin

The CS5321 modulator can produce "idle tones" which occur in the passband when the input signal is steady state dc signal within about ±50 mV of bipolar zero. In the CS5321 these tones are about 135 dB down from full scale. The user can force these idle tones "out-of-band" by adding 100 mV of dc offset to the signal at the AIN input. Alternately, if the user circuitry has a low offset voltage such that the input signal is within ±50mV of bipolar zero when no AC signal is present, the OFST pin on the CS5321 can be ac-

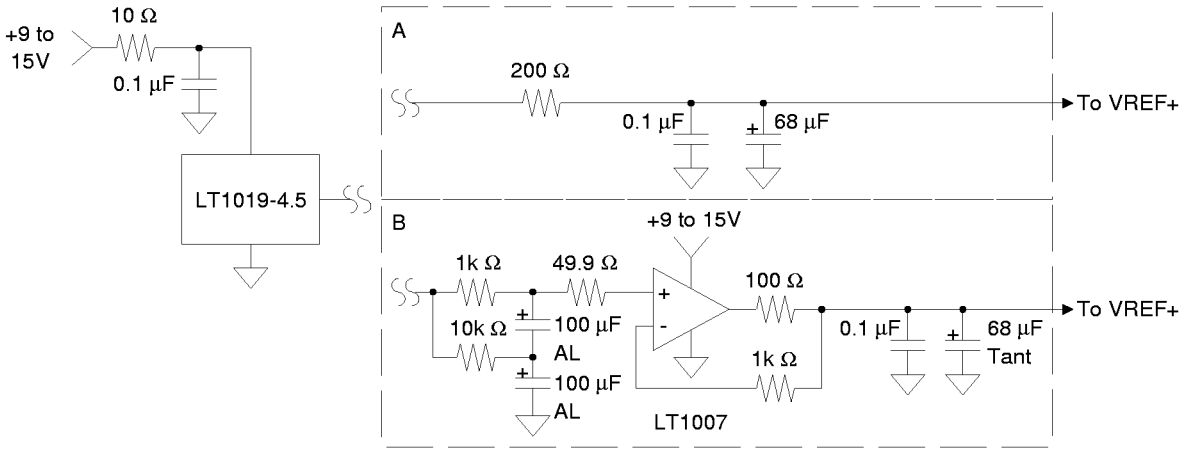


Figure 2. 4.5 Volt Reference with two filter options (see text)

tivated. When OFST = 1, +100 mV of input referred offset will be added internal to the CS5321 and guarantee that any idle tones present will lie out-of-band. The user should be certain that when OFST is active (OFST =1) that the offset voltage generated by the user circuitry does not negate the offset added by the OFST pin.

Input Range and Overrange Conditions

The analog input is applied to the AIN+ and AINR pins with the AIN- pin connected to GND. The input is fully differential but for proper operation the AIN- pin must remain at GND potential.

The analog input span is defined by the voltage applied between the VREF+ and VREF- input pins. See the Voltage Reference section of this data sheet for voltage reference requirements.

The modulator is a fourth order delta-sigma and is therefore conditionally stable. The modulator may go into an oscillatory condition if the analog input is overranged. Input signals which exceed either plus or minus full scale by more than 5 % can introduce instability in the modulator. If an unstable condition is detected, the modulator will be reduced to a first order system until loop stability is achieved. If this occurs the MFLG pin will transition from a low to a high which will result in an error bit being set in the CS5322. The input signal must be reduced to within the full scale range of the converter for at least 32 MCLK cycles for the modulator to recover from this error condition.

Voltage Reference

The CS5321 is designed to operate with a voltage reference in the range of 4.0 to 4.5 volts. The voltage reference is applied to the VREF+ pin with the VREF- pin connected to the GND. A 4.5 V reference will result in the best S/N performance but most 4.5V references require a power supply voltage greater than 5.0 V for operation. A 4.0 V reference can be used for those applications which must operate from only 5.0 V supplies, but will yield a S/N slightly lower (1-2 dB) than when using a 4.5 V reference. The voltage reference should be designed to yield less than 2 µV rms of noise in band at the VREF+ pin of the CS5321. The CS5322 filter selection will determine the bandwidth over which the voltage reference noise will affect the CS5321/CS5322 dynamic range.

For a 4.5 V reference, the LT1019-4.5 voltage reference yields low enough noise if the output is filtered with a low pass RC filter as shown in Figure 2-A. The filter in Figure 2-A is acceptable for most spectral measurement applications, but a buffered version with lower source imped-

ance (Figure 2-B) may be preferred for dc-measurement applications.

Due to its dynamic (switched-capacitor) input the input impedance of the +VREF pin of the CS5321 will change any time MCLK or HBR is changed. Therefore the current required from the voltage reference will change any time MCLK or HBR is changed. This can affect gain accuracy due to the high source impedance of the filter resistor in Figure 2-A. If gain error is to be minimized, especially when MCLK or HBR is changed, the voltage reference should have lower output impedance. The buffer of Figure 2-B offers lower output impedance and will exhibit better system gain stability.

Clock Source

For proper operation, the CS5321 must be provided with a CMOS-compatible clock on the MCLK pin. The MCLK for the CS5321 is usually provided by the CS5322 filter. MCLK is usually 1.024 MHz to set the seven selectable output word rates from the CS5322. The MCLK frequency can be as low as 250 kHz and as high as 1.2 MHz. The choice of clock frequency can affect performance; see the Performance section of the data sheet. The clock must have less than 300 ps jitter to maintain data sheet performance from the device. The CS5321 is equipped with loss of clock detection circuitry which will cause the CS5321 to enter a powered-down state if the MCLK is removed or reduced to a very low frequency. The HBR pin on the CS5321 modifies the sampling clock rate of the modulator. When HBR=1, the modulator sampling clock will be at MCLK/4; with HBR =0 the modulator sampling clock will be at MCLK/8. The chip set will exhibit about 3 dB less S/N performance when the HBR pin is changed from a logic "1" to a logic "0" for the same output word rate from the CS5322.

Low Power Mode

The CS5321 includes a low power operating mode (LPWR =1). hen operated with LPWR = 1, the CS5321 modulator sampling clock must be restricted to rates of 128 kHz or less. Operating in low power mode with modulator sample rates greater than 128 kHz will greatly degrade performance.

Digital Interface and Data Format

The MCLK signal (normally 1.024 MHz) is divided by four, or by eight inside the CS5321 to generate the modulator oversampling clock. The HBR pin determines whether the clock divider inside the CS5321 divides by four (HBR =1) or by eight (HBR =0). The modulator outputs a ones density bit stream from its MDATA and $\overline{\text{MDATA}}$ pins proportional to the analog input signal, but at a bit rate determined by the modulator oversampling clock. For proper synchronization of the bitstream, the CS5321 must be furnished with an MSYNC signal prior to data conversion. The MSYNC signal, generated by the CS5322, resets the MCLK counter-divider in the CS5321 to the correct phase so that the bitstream can be properly sampled by the CS5322 digital filter.

When operated with the CS5322 digital filter the output codes from the CS5321/CS5322 will range from approximately decimal -5,242,880 to +5,242879 for an input to the CS5321 of ±4.5 V. Table 1 illustrates the output coding for various input signal amplitudes. Note that with a signal input defined as a full scale signal (4.5 V with VREF+ =4.5V) the CS5321/CS5322 chip does not output a full scale digital code of 8,388,607 but is scaled to a lower value to allow some overrange capability. Input signals can exceed the defined full scale by up to 5% and still be converted properly.

Modulator Input Signal	CS5322 Filter Output Code	
	HEX	Decimal
> (+VREF + 5%)	Error Flag Possible	
≈ (+VREF + 5%)	53FFFF(H)	+5505023
+VREF	4FFFFF(H)	+5242879
0V	000000(H)	0
-VREF	B00000(H)	-5242880
≈ - (+VREF + 5%)	AC0000(H)	-5505024
> - (+VREF + 5%)	Error Flag Possible	

Table 1. Output Coding for the CS5321 and CS5322 combination.

Performance

Figure 3, 4 and 5 illustrate the spectral performance of the CS5321/CS5322 when operating from a 1.024 MHz master clock. Ten 1024 point FFTs were averaged to produce the plots.

Figure 3 illustrates the chip set with a 100 Hz, -20 dB input signal. The sample rate was set at 1 kHz. Dynamic range is 122 dB.

The dynamic range calculated by the test software is reduced somewhat in Figures 4 and 5 because of jitter in the signal test oscillator. Jitter in the 100 Hz signal source is interpreted by the signal processing software to be increased noise.

The choice of master clock frequency will affect performance. The CS5321 will exhibit the best Signal/ Distortion performance with slower modulator sampling clock rates as slower sample rates allow more time for amplifier settling.

For lowest offset drift, the CS5321 should be operated with MCLK = 1.024 MHz and HBR =1. Slower modulator sampling clock rates will exhibit more offset drift. Changing MCLK to 512 kHz (HBR =1) or changing HBR to zero (MCLK =1.024 MHz) will cause the drift rate to double. Offset drift is not linear over temperature

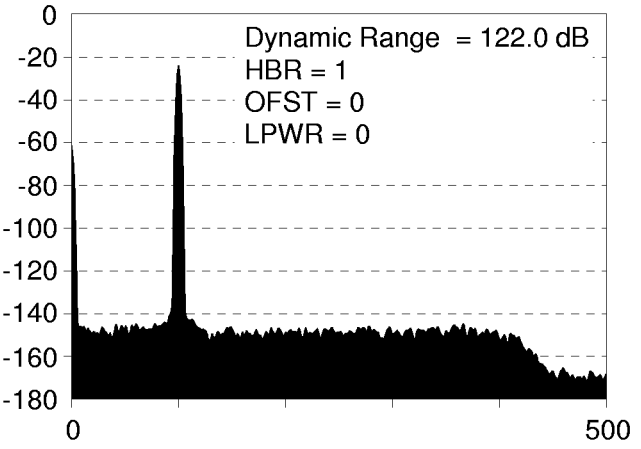


Figure 3. 1024 Point FFT Plot with -20 dB, 100 Hz Input, ten averages

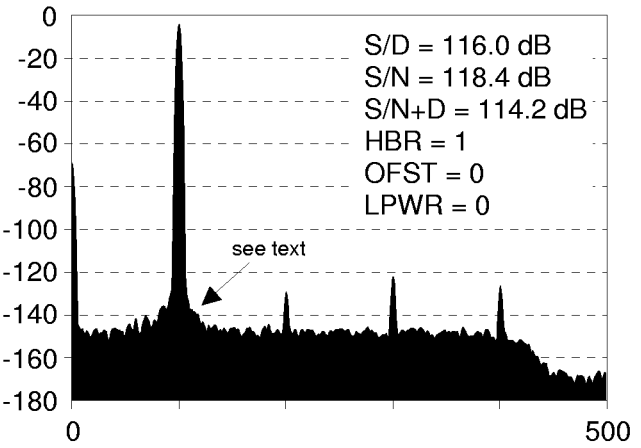


Figure 4. 1024 Point FFT Plot with Full Scale Input, 100 Hz, ten averages

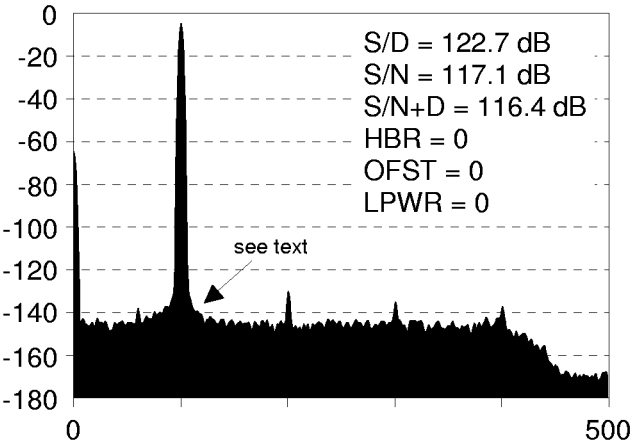


Figure 5. 1024 Point FFT Plot with Full Scale Input, 100 Hz, ten averages

so it is difficult to specify an exact drift rate. Offset drift characteristics vary from part to part and will vary as the power supply voltages vary. Therefore, if the CS5321 is to be used in precision dc measurement applications where offset drift is to be minimized, the power supplies should be well regulated. The CS5321 will exhibit about 6 ppm/°C of offset drift with MCLK = 1 and HBR =1.

Gain drift of the CS5321 itself is about 5 ppm/°C and is not affected by either modulator sample rate or by power supply variation.

Power Supply Considerations

The system connection diagram, Figure 1, illustrates the recommended power supply arrangements. There are two positive power supply pins for the CS5321 and two negative power supply pins. Power must be supplied to all four pins and each of the supply pins should be decoupled with a 0.1 uF capacitor to the nearest ground pin on the device.

When used with the CS5322 digital filter, the maximum voltage differential between the positive supplies of the CS5321 and the positive digital supply of the CS5322 must be less than 0.25 V. Operation beyond this constraint may result in loss of analog performance in the CS5321/ CS5322 system performance.

Many seismic or sonar systems are battery powered, and utilize dc-dc converters to generate the necessary supply voltages for the system. To minimize the effects of power supply interference, it is desirable to operate the dc-dc converter at a frequency which is rejected by the digital filter, or locked to the modulator sample clock rate.

A synchronous dc-dc converter, whose operating frequency is derived from the 1.024 MHz clock used to drive the CS5322, will minimize the potential for "beat frequencies" appearing in the passband between dc and the corner frequency of the digital filter.

Power Supply Rejection Ratio

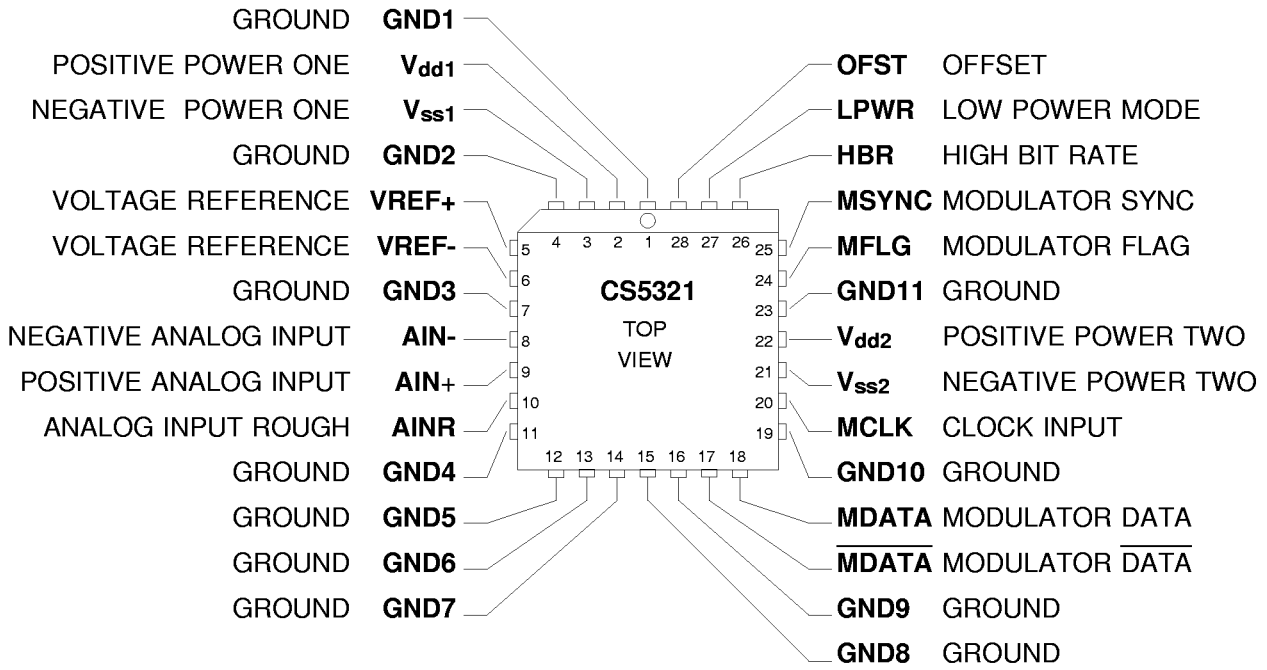
The PSRR of the CS5321 is frequency dependent. The CS5322 digital filter attenuation will aid in rejection of power supply noise for frequencies above the corner frequency setting of the CS5322. For frequencies between dc and the corner frequency of the digital filter, the PSRR is nearly constant at about 60 dB.

Board Layout Considerations

All of the 0.1 µF filter capacitors on the power supplies, AIN+, and AINR, should be placed very close to the chip and connect to the nearest ground pin on the device. The capacitors between VREF+ and VREF- should be located as close to the chip as possible.

The 0.1 µF capacitors on the AIN+ and AINR pins should be placed with their leads on the same axis, not side-by-side. If these capacitors are placed side-by-side their electric fields can interact and cause increased distortion.

The chip should be surrounded with a ground plane. Trace fill should be used around the analog input components. See the *Layout and Design Rules for Data Converters* application note in the Data Book.



CS5321 PIN DESCRIPTIONS

Power Supplies

V_{dd1} – Positive Power One, PIN 2
Positive supply voltage. Nominally +5 Volts.

V_{dd2} – Positive Power Two, PIN 22
Positive supply voltage. Nominally +5 Volts.

V_{ss1} – Negative Power One, PIN 3
Negative supply voltage. Nominally -5 Volts.

V_{ss2} – Negative Power Two, PIN 21
Negative supply voltage. Nominally -5 Volts.

GND1 through GND11 – Ground, PINS 1, 4, 7, 11, 12, 13, 14, 15, 16, 19, 23.
Ground reference.

Analog Inputs

AIN+ - Positive Analog Input, PIN 9
Nominally ± 4.5V

AIN- - Negative Analog Input, PIN 8
This pin is tied to ground.

AINR - Analog Input Rough, PIN 10

Allows a non-linear current to bypass the main external anti-aliasing filter which if allowed to happen, would cause harmonic distortion in the modulator. Please refer to the System Connection Diagram and the Analog Input and Voltage Reference section of the data sheet for recommended use of this pin.

VREF+ – Positive Voltage Reference Input, PIN 5

This pin accepts an external +4.5V voltage reference.

VREF- – Negative Voltage Reference Input, PIN 6

This pin is tied to ground.

Digital Inputs

MCLK – Clock Input, PIN 20

A CMOS-compatible clock input to this pin (nominally 1.024 MHz) provides the necessary clock for operation of the modulator, digital filter and data output portions of the A/D converter.

MSYNC – Modulator Sync, PIN 25

A transition from a low to high level on this input will re-initialize the CS5321. MSYNC resets a divider-counter to align the MDATA output bit stream from the CS5321 with the timing inside the CS5322.

OFST - Offset, PIN 28

When high, adds approximately 100mV of input referred offset to guarantee that any zero input limit cycles are out of band if present. When low, zero offset is added.

LPWR - Low Power Mode, PIN 27

The CS5321 power dissipation can be reduced from its nominal value of 60 mW to 30 mW under the following conditions:
LPWR=1; MCLK $\leq$ 512 kHz, HBR=1; or
LPWR=1; MCLK $\leq$ 1.024 MHz, HBR=0

HBR – High Bit Rate, Pin 26

Selects either $\frac{1}{4}$MCLK (HBR=1) or $\frac{1}{8}$MCLK (HBR=0) for the modulator sampling clock.

Digital Outputs

MDATA – Modulator Data Output, PIN 18

Data will be presented in a one-bit serial data stream at a bit rate of 256 kHz (HBR=1) or 128 kHz (HBR=0) with MCLK operating at 1.024MHz.

$\overline{\text{MDATA}}$ – Modulator $\overline{\text{Data}}$ Output, PIN 17

Inverse of the MDATA output.

MFLG – Modulator Flag, PIN 24

A transition from a low to high level signals that the CS5321 modulator is unstable due to an over-range on the analog input.

PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full-scale (rms) signal to the broadband (rms) noise signal. Broadband noise is measured with the input grounded within the bandwidth of 1 Hz to $f_{OWR}/2$ Hz. Units in db.

Signal-to-Distortion

The ratio of the full-scale (rms) signal to the rms sum of all harmonics up to 1000 Hz. Units in dB.

Intermodulation Distortion

The ratio of the rms sum of the two test frequencies (30 and 50 Hz) which are each 6dB down from full-scale to the rms sum of all intermodulation components within the bandwidth of dc to 1000 Hz. Units in dB.

Full Scale Error

The ratio of the difference between the value of the voltage reference and analog input voltage to the full-scale span (two times the voltage reference value). The ratio is calculated after the effects of offset and the external bias components are removed and the analog input voltage is adjusted. Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in %.

Full Scale Drift

The change in the Full Scale value with temperature. Units in ppm/°C

Offset

The difference between the analog ground and the analog voltage necessary to yield an output code from the CS5321/CS5322 of 000000(H). Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in mV.

Offset Drift

The change in the Offset value with temperature. Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in µV/°C

A DIVISION OF CIRRUS LOGIC

CDB5321

Evaluation Board for CS5321 and CS5322

Features

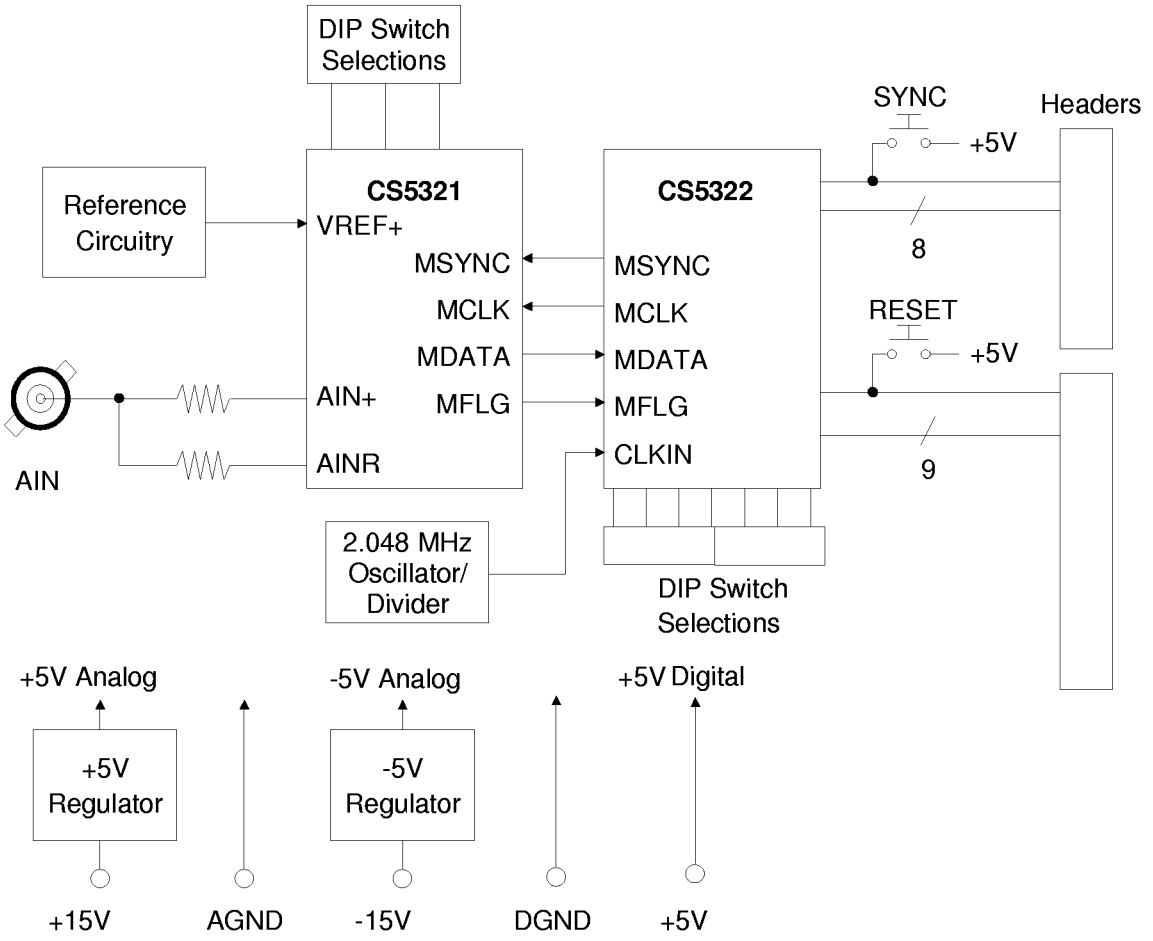
- DIP switch control of all CS5322 logic pins
- Header control of all CS5322 logic pins
- Supports manual operation of RESET and SYNC

Description

The CDB5321 is an evaluation board that allows laboratory characterization of the CS5321/CS5322 A/D converter chip-set. The chip-set supports seven different selectable word rates: 4 kHz, 2 kHz, 1 kHz, 500 Hz 250 Hz, 125 Hz and 62.5 Hz. Input to the board is 9 volts peak-to-peak. Output is via header connections to the CS5322 serial interface.

ORDERING INFORMATION

CDB5321 Evaluation Board



Cirrus Logic, Inc.
Crystal Semiconductor Products Division
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.crystal.com

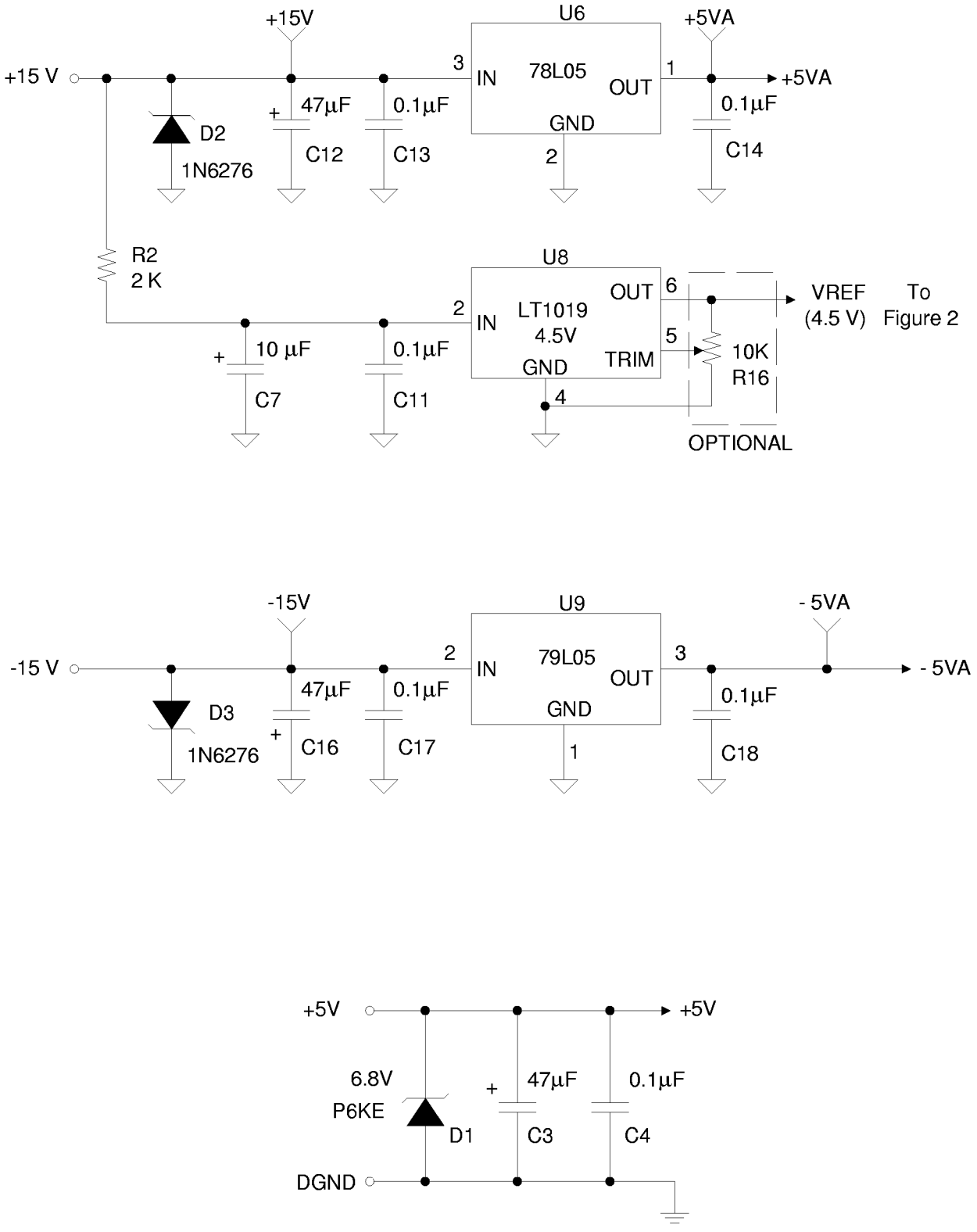


Figure 1. Power Supplies

OVERVIEW

The CDB5321 evaluation board requires three separate power supplies for proper operation. Figure 1 illustrates the power supply connections. The required power supply input voltages consist of +5V, +15V, and -15V. The CS5322 filter and logic support devices on the board operate from the +5V supply. The +15V and -15V inputs are regulated down to provide +5V and -5V supplies necessary for the CS5321 modulator. Figure 1 also illustrates the LT1019 4.5V reference used with the CS5321 modulator.

Figure 2 illustrates the CS5321 modulator circuitry, including the analog BNC input for the test signal source. Most often switch selections on S5 are set to HBR=1, LPWR=0, and

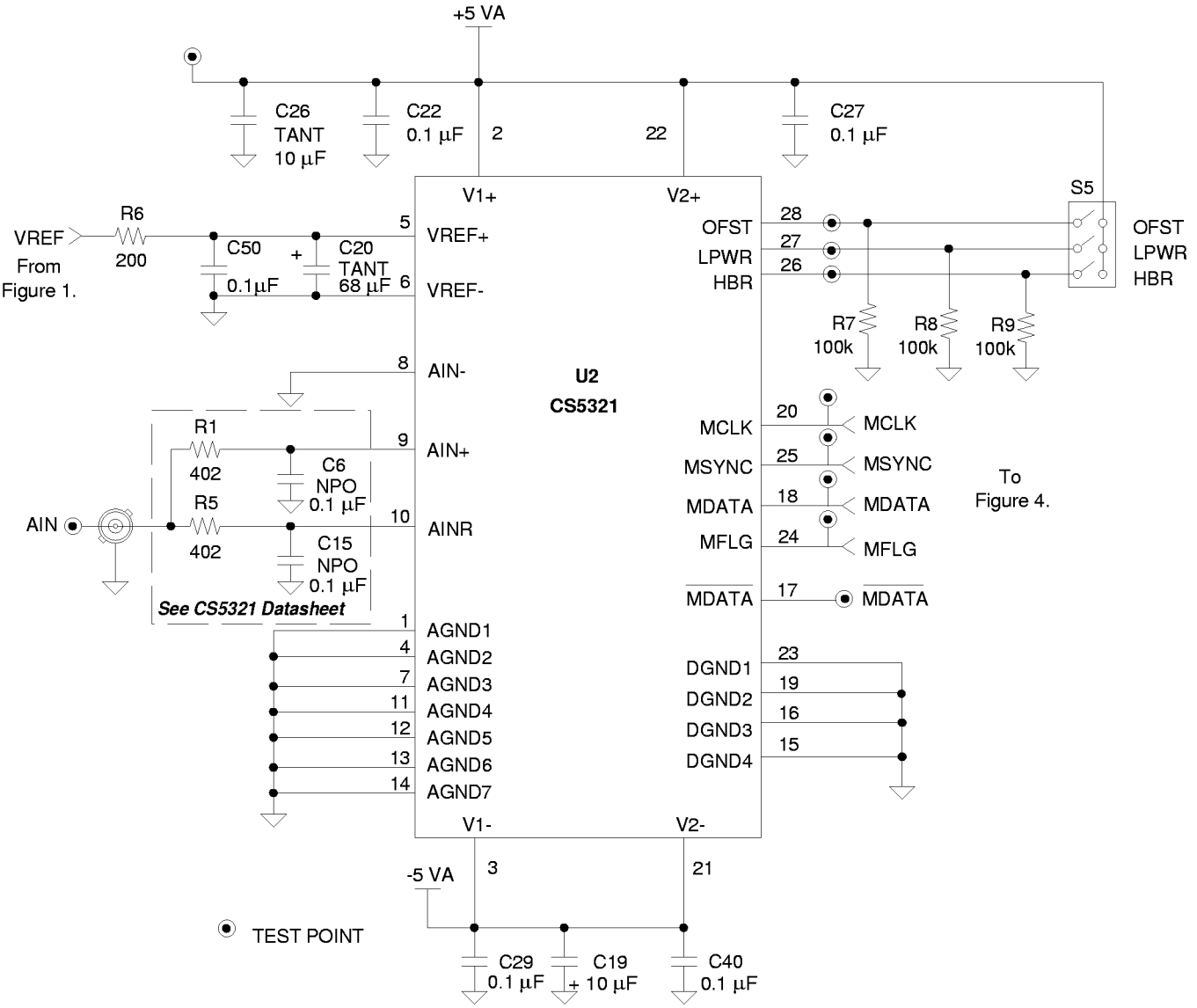


Figure 2. CS5321 Modulator Input Circuitry.

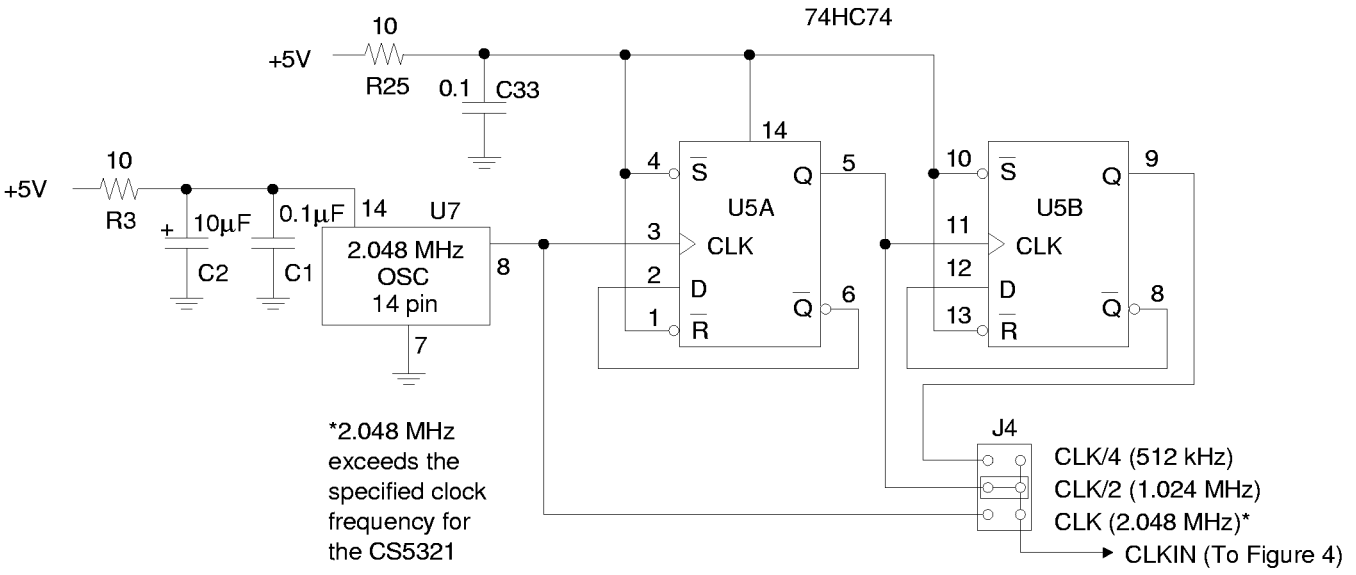


Figure 3. Oscillator / Divider

OFST=1. Figure 3 illustrates the 2.048 MHz oscillator and dual D flip flop clock divider. Note that both the oscillator and the divider are separately decoupled from the +5V supply to reduce clock jitter which can be introduced from noisy supplies. Jumper J4 should be set in the CLK/2 position to source 1.024 MHz to the CS5322 chip for normal operation. If operation from 512 kHz clock is desired, the J4 jumper should be changed to the CLK/4 position. The board can be tested at 512 kHz without modification.

The digital interface pins to the CS5322 filter chip are all available on the header connectors J1, J2, and J3 as shown in Figures 4, 5, and 6. Note that one row of pins on each of the headers is ground. It is advised that any connections made to control lines be done with twisted pair ribbon cable; with each twisted pair containing one signal and one ground connection. This minimizes radiated noise.

CAUTION!

Caution is advised when interfacing the evaluation board to any circuitry powered from another source. For example, when interfacing to a computer I/O card be sure that the evaluation board and the computer are both powered up before connecting to the evaluation board headers. Always disconnect header connections when powering down the board but not the computer. Failure to follow this advice may cause damage to either the computer I/O or to the CS5322, because the computer outputs try to power the CDB5321 board.

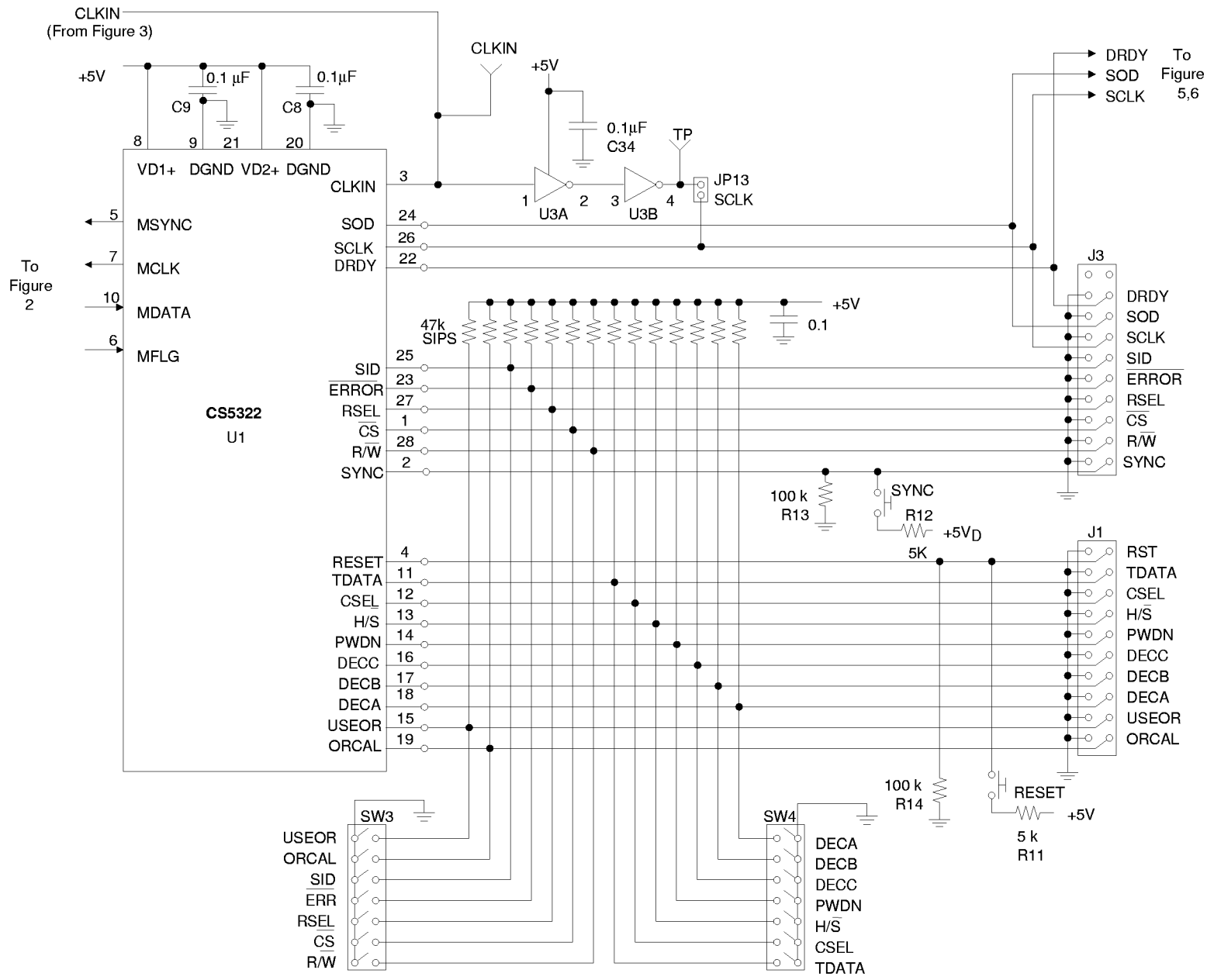


Figure 4. CS5322 Filter Interface

USEOR	ON*	Do not use offset register
	OFF	Use offset register
ORCAL	ON*	Disable offset register calibration
	OFF	Enable offset register calibration
SID	ON	Sets SID to Logic 0
	OFF*	Allows pull-up on SID line
ERR	ON	Sets ERR to logic 0
	OFF*	Allows CS5322 ERROR output
RSEL	ON	Select status register
	OFF*	Select conversion data register
CS	ON*	Chip select active
	OFF	Chip select inactive
R/$\overline{W}$	ON	Enables write mode via SID pin
	OFF*	Enables read mode via SOD pin

OFF = OPEN = 1

*Default to use Figure 6 interface.

Table 1. S3 DIP Switch Selections

DECA	Selection via hardware pins	ABC	Output Word Rate
DECB		0 0 0	62.5
DECC		1 0 0	125
		0 1 0	250
		1 1 0	500
		0 0 1	1000
		1 0 1	2000
		0 1 1	4000
PWDN	ON*	Normal Operation	
	OFF	Power down active	
H/$\overline{S}$	ON	Selects configuration register for operating mode	
	OFF*	Select hardware pins for operating mode	
CSEL	ON*	Selects MDATA from modulator	
	OFF	Selects TDATA as filter input	
TDATA	ON*	Sets TDATA input to logic 0	
	OFF	Enables TDATA from J1 header	

OFF = OPEN = 1

*Default to use Figure 6 interface.

Table 2. S4 DIP switch selections

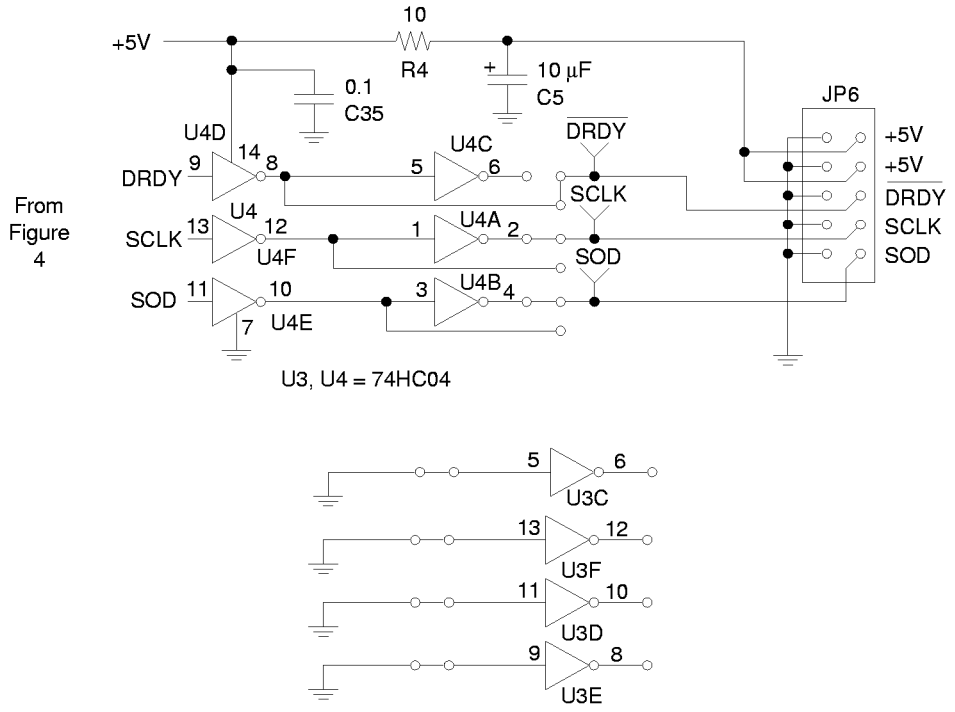


Figure 5. Serial Latch Interface on CDB5321 (Rev B) board

Figures 5 and 6 illustrate the logic used to drive connections at header JP6 (Rev. B Board) or J2 (Rev. C Board).

The Rev. C evaluation board can directly interface to the CDBCAPTURE board through connector J2. A D-type Flip-Flop must be added in the patch area of the Rev. B evaluation board to enable it to interface to the CDBCAPTURE board. The CDBCAPTURE can be used to perform FFT analysis and noise histograms.

Tables 1 and 2 illustrate the DIP switch positions of switches S3 and S4. The switch positions with asterisks indicate preferred settings for driving the interface on the CDBCAPTURE system.

The CS5322 filter should be set up for hardware mode (H/$\overline{S}$ on switch S4 open). DIP switch S4 can then be used to select the desired output word rate. After the selection on the DECA, DECB, and DECC positions of the S4 DIP switch, the S2 RESET switch must be activated, followed by the S1 SYNC switch (unless these signals are controlled via the J1 and J3 header signals).

Figure 7 illustrates the component layout of the board while figures 8 and 9 illustrate the board layout (not to scale).

Using the Evaluation Board

Connect the appropriate power supplies to the binding posts of the board. Twist the +5V digital supply lead with the digital ground lead from the board to the supply. Also twist the supply leads for the analog voltages. Use a high quality power supply which is low in noise and line frequency(50/60 Hz) interference.

Power up the supplies. Then connect a coaxial cable from the analog BNC to the signal source. Note that the performance of the A/D converter chip set will exceed the capability of most signal generators, with respect to noise, distortion, and line frequency interference.

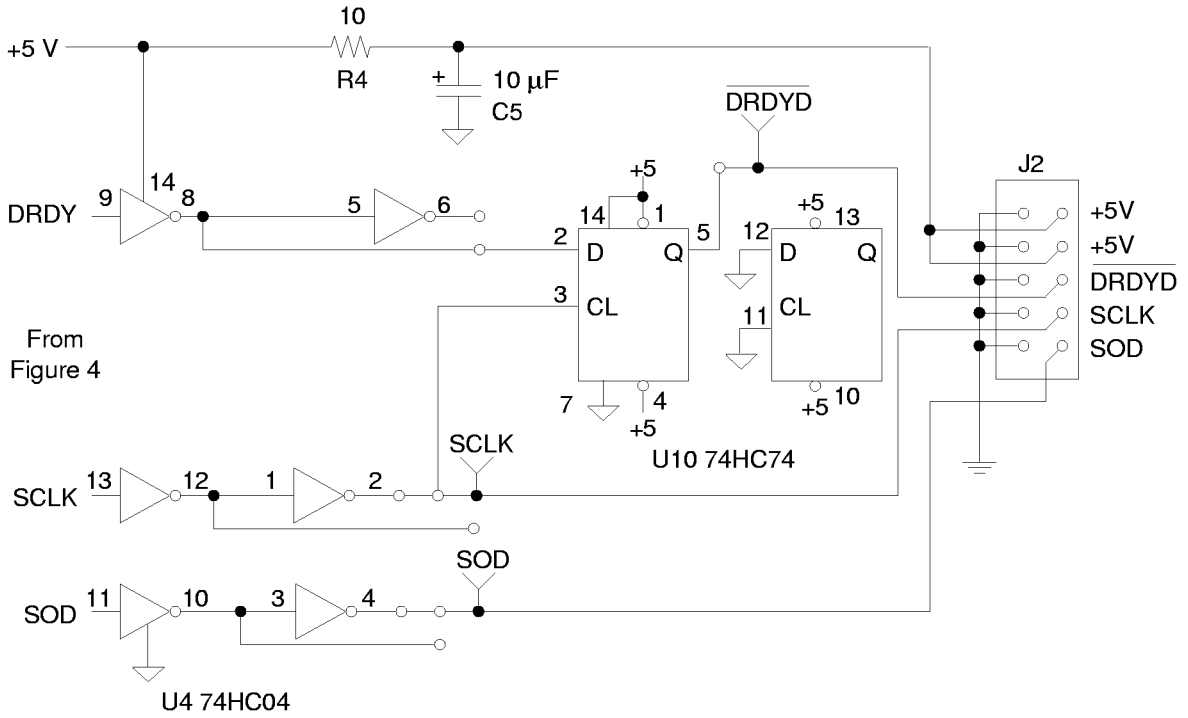


Figure 6. Serial Latch Interface on CDB5321 (Rev C) board.

Once power has been applied to the board, connect the ribbon cable to the appropriate headers (J1, J2, and/or J3). The reset and the sync signals to the CS5322 must be applied before normal operation can commence. This can be done by using the S2 RESET switch and the S1 SYNC switch or by interfacing to these signals via the J1 and J3 headers.

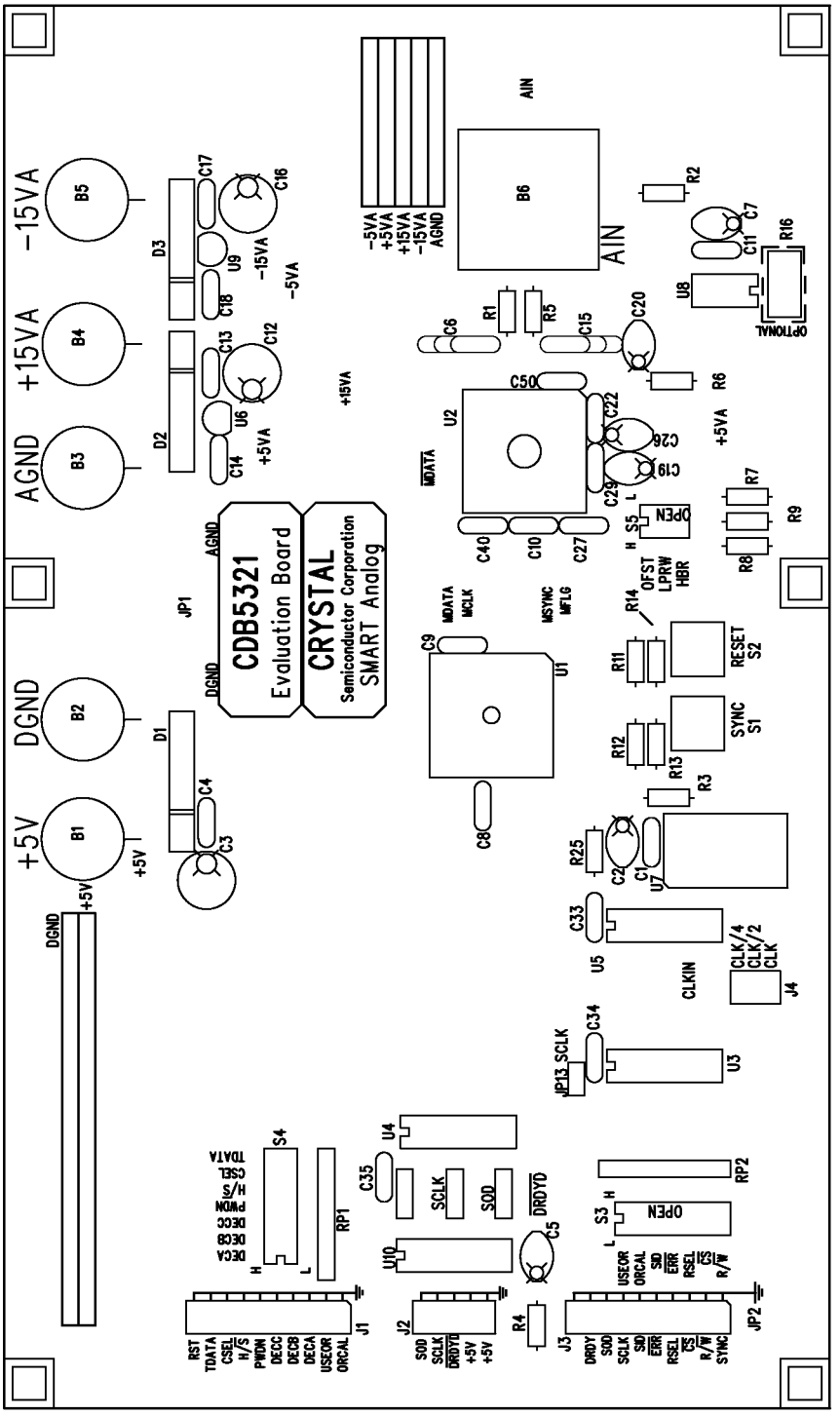


Figure 7. CDB5321 (Rev. C) Silk Screen Layout (Not to Scale)

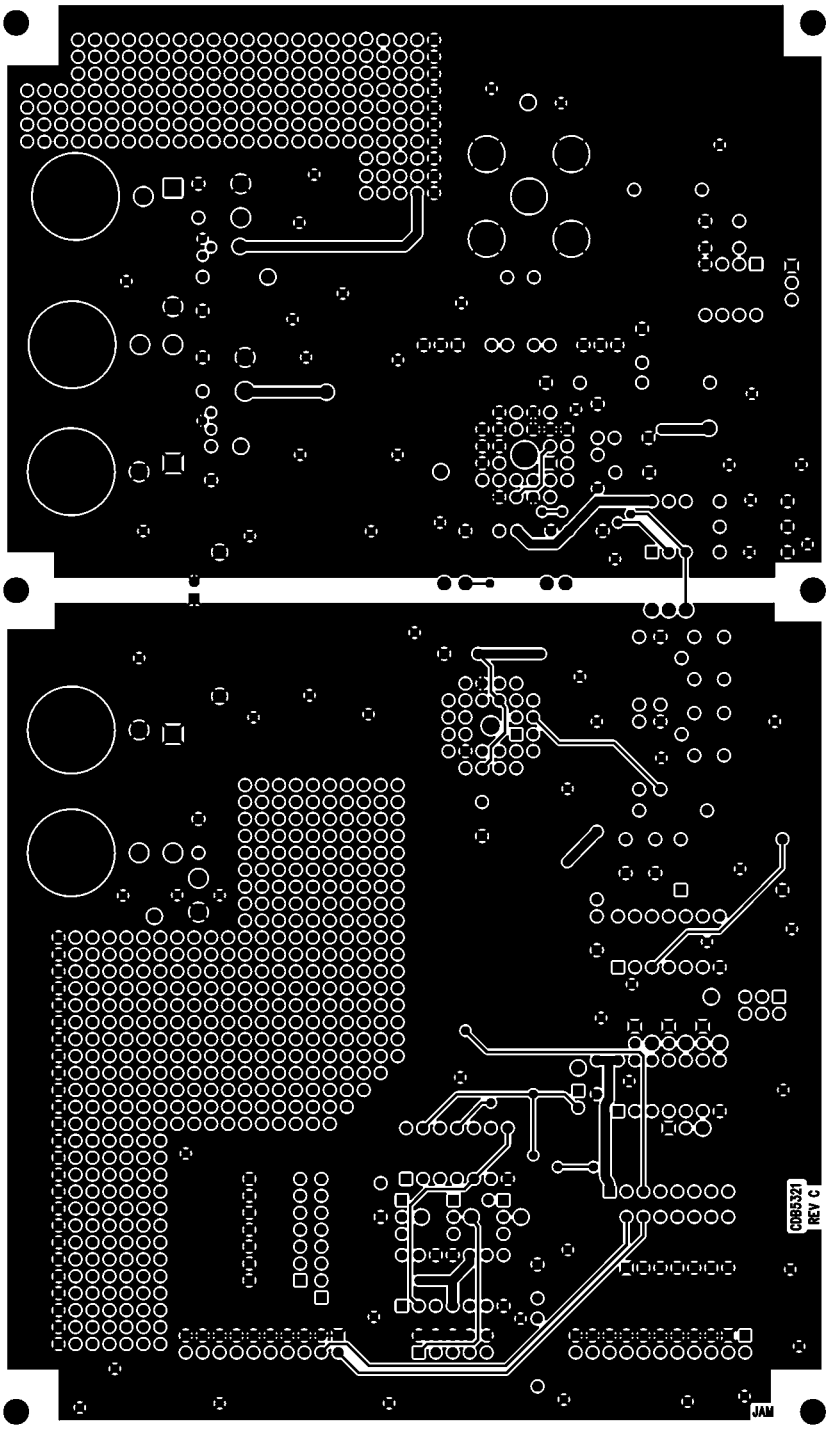


Figure 8. CDB5321 (Rev. C) Component Side Layer (Not to Scale)

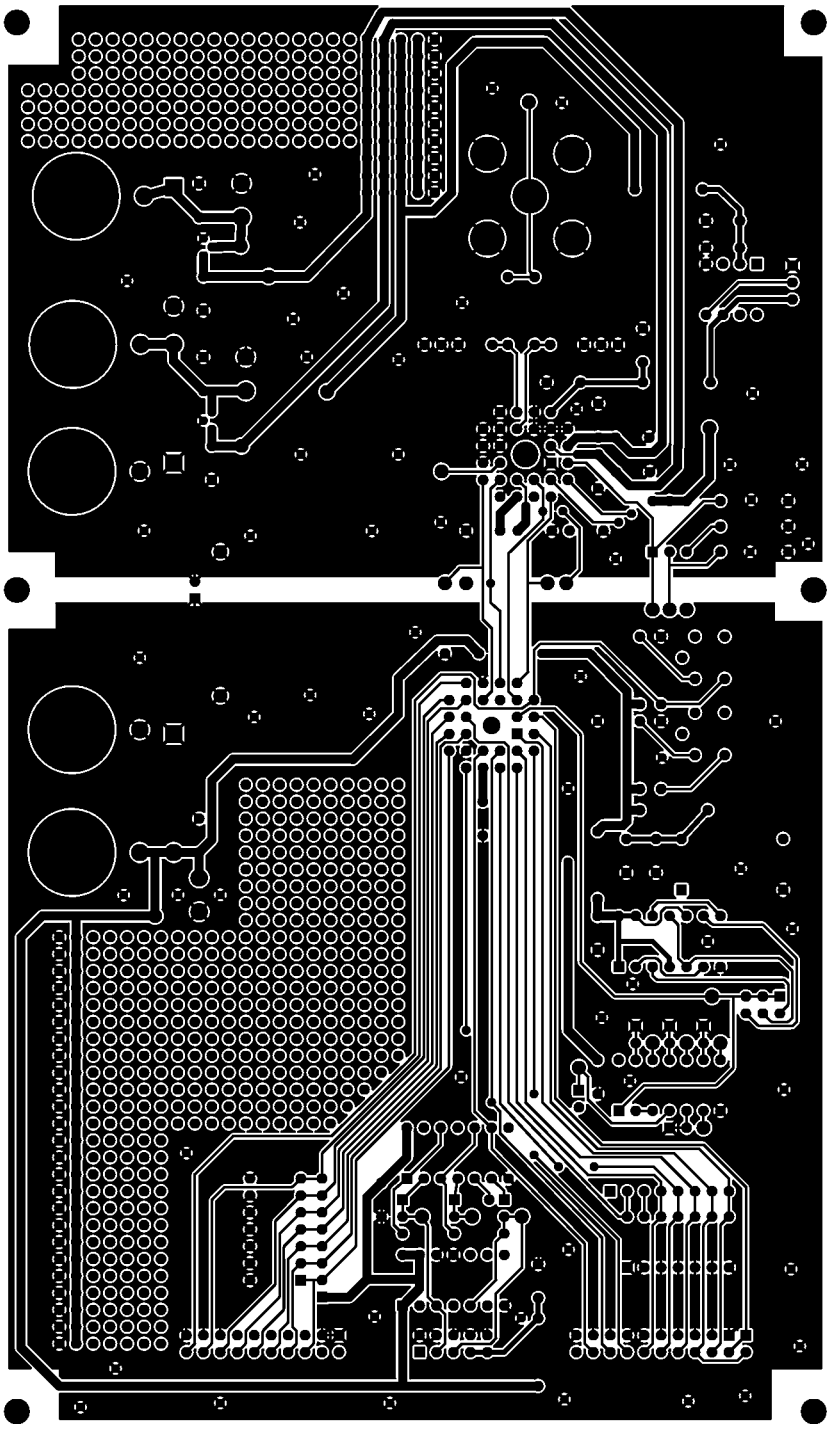


Figure 9. CDB5321 (Rev. C) Solder Side Layer (Not to Scale)