WM8718

24 Bit Differential Stereo DAC with Volume Control

DESCRIPTION

The WM8718 is a high performance differential stereo DAC designed for audio applications such as DVD, home theatre systems and digital TV. The WM8718 supports PCM data input word lengths from 16 to 32-bits and sampling rates up to 192kHz. The WM8718 consists of a serial interface port, digital interpolation filters, multi-bit sigma delta modulators and differential stereo DAC in a small 20-lead SSOP package. The WM8718 includes a digitally controllable mute, an attenuate function and zero flag output for each channel.

The 3-wire serial control port provides access to a wide range of features including on-chip mute, attenuation and phase reversal.

The WM8718 is an ideal device to interface to AC-3™, DTS™, and MPEG audio decoders for surround sound applications, or for use in DVD players including those supporting DVD-A.

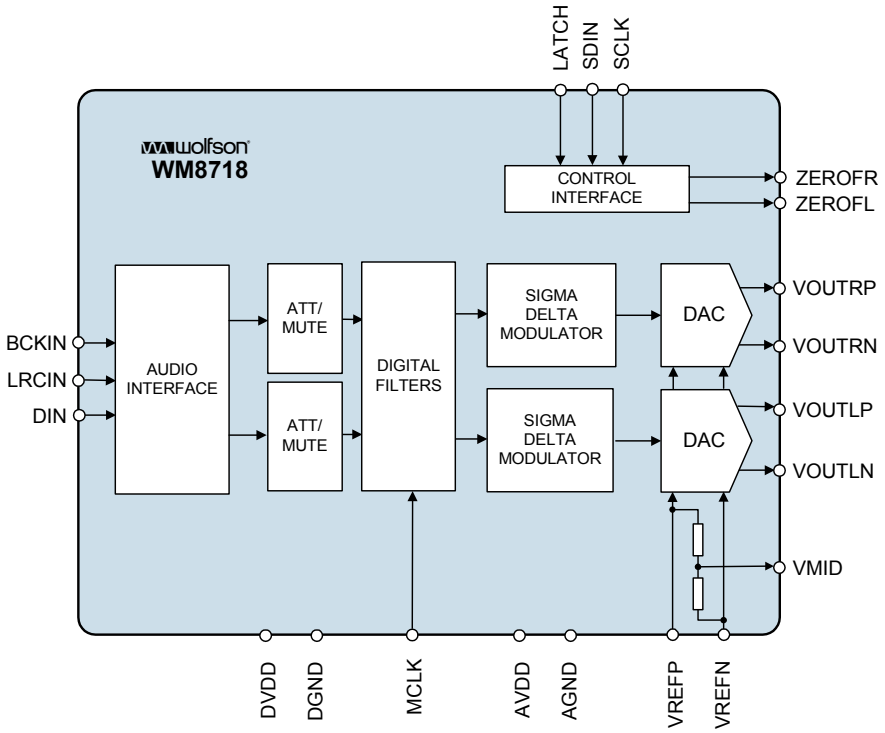
FEATURES

- 24 bit Stereo DAC
- Fully Differential Voltage Outputs
- Audio Performance
  - 111dB SNR ('A' weighted @ 48kHz) DAC
  - -100dB THD
- DAC Sampling Frequency: 8kHz - 192kHz
- 3 Wire Serial Control Interface
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified, DSP
  - 16/20/24/32 bit Word Lengths
- Independent Digital Volume Control on Each Channel with 127.5dB Range in 0.5dB Steps
- Independent Zero Flag Outputs
- 3.0V - 5.5V Supply Operation
- 20-lead SSOP Package

APPLICATIONS

- CD, DVD, and DVD-Audio Players
- Home theatre systems
- Professional mixing desks

BLOCK DIAGRAM



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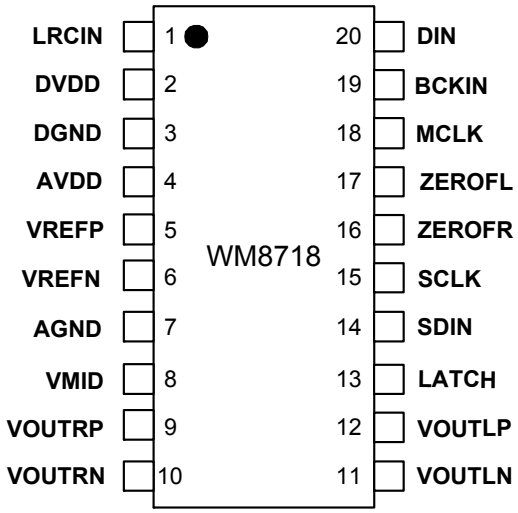
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8718SEDS/V	-40 to +85°C	20-lead SSOP (Pb-free)	MSL2	260°C
WM8718SEDS/RV	-40 to +85°C	20-lead SSOP (Pb-free, tape and reel)	MSL2	260°C

Note:
Reel quantity = 2,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	LRCIN	Digital Input	PCM DAC Sample Rate Clock Input
2	DVDD	Supply	Positive Digital Supply
3	DGND	Supply	Ground Digital Supply
4	AVDD	Supply	Positive Analogue Supply
5	VREFP	Supply	Positive DAC reference Supply
6	VREFN	Supply	Negative DAC reference Supply
7	AGND	Supply	Ground Analogue Supply
8	VMID	Analogue Output	Mid Rail Decoupling Point
9	VOUTRP	Analogue Output	Right Channel DAC Output Positive
10	VOUTRN	Analogue Output	Right Channel DAC Output Negative
11	VOUTLN	Analogue Output	Left Channel DAC Output Negative
12	VOUTLP	Analogue Output	Left Channel DAC Output Positive
13	LATCH	Digital Input P.U.	Serial Control Load Input
14	SDIN	Digital Input	Serial Control Data Input
15	SCLK	Digital Input P.D.	Serial Control Data Input Clock
16	ZEROFR	Digital Output (Open drain)	Infinite ZERO Detect Flag for Right Channel
17	ZEROFL	Digital Output (Open drain)	Infinite ZERO Detect Flag for Left Channel
18	MCLK	Digital Input	Master Clock Input
19	BCLKIN	Digital Input	PCM Audio Data Bit Clock Input
20	DIN	Digital Input	PCM Serial Audio Data Input

Note:

Digital input pins have Schmitt trigger input buffers. Pins marked `P.U.` or `P.D.` have an internal pull-up or pull-down resistor.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage (DVDD)	-0.3V	+7V
Analogue supply voltage (AVDD)	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T_A	-40°C	+85°C
Storage temperature after soldering	-65°C	+150°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		3.0		5.5	V
Analogue supply range	AVDD		3.0		5.5	V
Ground	AGND, DGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V
Supply current		AVDD = 3.3V	0.191[1]	19		mA
		AVDD = 5V	0.191[1]	22		mA
Supply current		DVDD = 3.3V	160 uA	7.1		mA
		DVDD = 5V	160 uA	8.3		mA

Notes:

1. This value represents the current usage when there are no switching digital inputs, MCLK is applied and the chip is in power down mode
2. Digital supply DVDD must never be more than 0.3V greater than AVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (TTL Levels)						
Input LOW level	V_{IL}				0.8	V
Input HIGH level	V_{IH}		2.0			V
Output LOW	V_{OL}	I_{OL} = 1mA			DGND + 0.3V	V
Output HIGH	V_{OH}	I_{OH} = 1mA	DVDD – 0.3V			V
Analogue Reference Levels						
Reference voltage		VMID	AVDD/2 - 50mV	AVDD/2	AVDD/2 + 50mV	V
Potential divider resistance	R_{VMID}			8.7		kΩ
DAC Output (Load = 10kΩ 50pF)						
SNR (Note 1,2,3)		A-weighted, @ fs = 48kHz	105	111		dB
SNR (Note 1,2,3)		A-weighted @ fs = 96kHz		109		dB
SNR (Note 1,2,3)		A-weighted @ fs = 192kHz		109		dB
SNR (Note 1,2,3)		A-weighted, @ fs = 48kHz AVDD = 3.3V		105		dB
SNR (Note 1,2,3)		A-weighted @ fs = 96kHz AVDD = 3.3V		102		dB
SNR (Note 1,2,3)		Non 'A' weighted @ fs = 48kHz		108		dB
THD (Note 1,2,3)		1kHz, 0dBFs		-100	-80	dB
THD+N (Dynamic range, Note 2)		1kHz, -60dBFs	105	111		dB
DAC channel separation				100		dB

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Output Levels						
Differential Output level		Load = 10kΩ, 0dBFS		2.0		V_{RMS}
		Load = 10kΩ, 0dBFS, (AVDD = 3.3V)		1.32		V_{RMS}
Gain mismatch channel-to-channel				±1		%FSR
Minimum resistance load		To midrail or a.c. coupled		1		kΩ
		To midrail or a.c. coupled (AVDD = 3.3V)		600		Ω
Maximum capacitance load		5V or 3.3V		100		pF
Output d.c. level				(AVDD-GND)/2		V
Power On Reset (POR)						
POR threshold				2.0		V

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all ZEROS into the digital input, over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full-scale output and the output with a ZERO signal applied. (No Auto-ZERO or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full-scale signal down one channel and measuring the other.
6. Pass-Band Ripple – Any variation of the frequency response in the pass-band region.

MASTER CLOCK TIMING

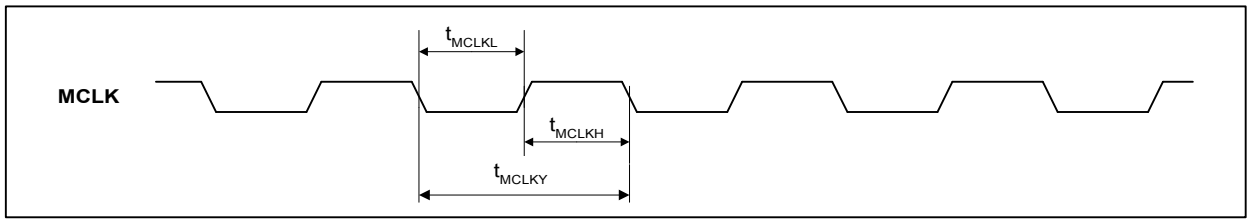


Figure 1 Master Clock Timing Requirements

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing Information						
MCLK Master clock pulse width high	t_{MCLKH}		13			ns
MCLK Master clock pulse width low	t_{MCLKL}		13			ns
MCLK Master clock cycle time	t_{MCLKY}		26			ns
MCLK Duty cycle			40:60		60:40	

DIGITAL AUDIO INTERFACE TIMINGS

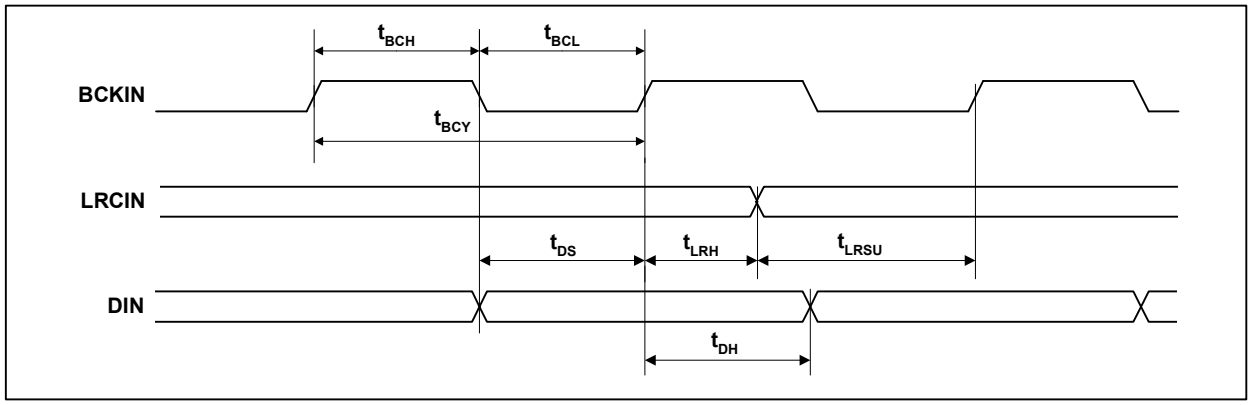


Figure 2 Digital Audio Data Timing

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCKIN cycle time	t_{BCY}		40			ns
BCKIN pulse width high	t_{BCH}		16			ns
BCKIN pulse width low	t_{BCL}		16			ns
LRCIN set-up time to BCKIN rising edge	t_{LRSU}		8			ns
LRCIN hold time from BCKIN rising edge	t_{LRH}		8			ns
DIN set-up time to BCKIN rising edge	t_{DS}		8			ns
DIN hold time from BCKIN rising edge	t_{DH}		8			ns

3-WIRE SERIAL CONTROL INTERFACE TIMING

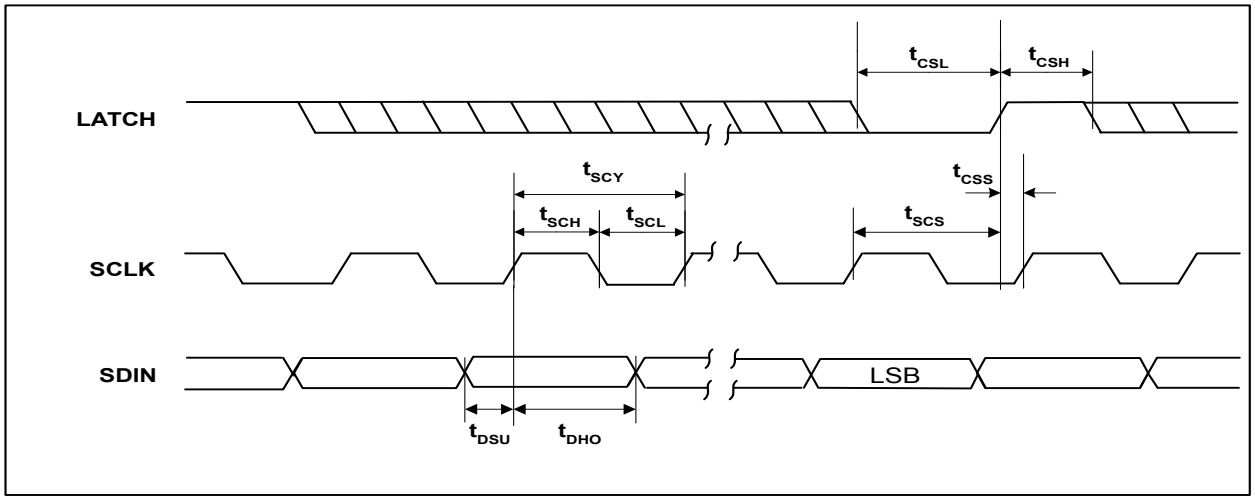


Figure 3 Program Register Input Timing - 3-Wire Serial Control Mode

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCLK rising edge to LATCH rising edge	t_{SCS}		40			ns
SCLK pulse cycle time	t_{SCY}		80			ns
SCLK pulse width low	t_{SCL}		20			ns
SCLK pulse width high	t_{SCH}		20			ns
SDIN to SCLK set-up time	t_{DSU}		20			ns
SCLK to SDIN hold time	t_{DHO}		20			ns
LATCH pulse width low	t_{CSL}		20			ns
LATCH pulse width high	t_{CSH}		20			ns
LATCH rising to SCLK rising	t_{CSS}		20			ns

INTERNAL POWER ON RESET CIRCUIT

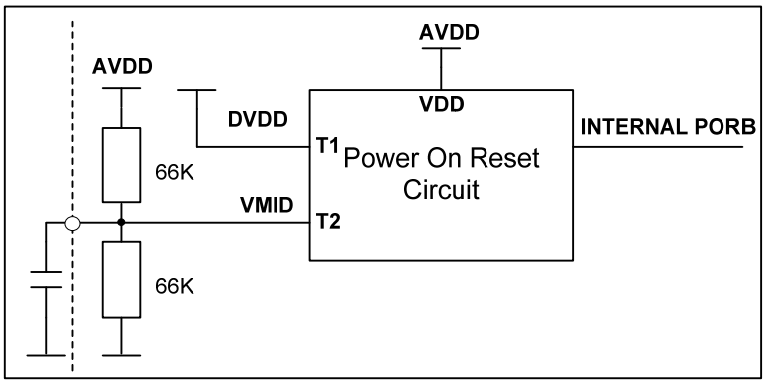


Figure 4 Internal Power On Reset Circuit Schematic

The WM8718 includes an internal Power On Reset Circuit which is used reset the digital logic into a default state after power up.

Figure 4 shows a schematic of the internal POR circuit. The POR circuit is powered from AVDD. The circuit monitors DVDD and VMID and asserts PORB low if DVDD or VMID are below the minimum threshold Vpor_off.

On power up, the POR circuit requires AVDD to be present to operate. PORB is asserted low until AVDD and DVDD and VMID are established. When AVDD, DVDD, and VMID have been established, PORB is released high, all registers are in their default state and writes to the digital interface may take place.

On power down, PORB is asserted low whenever DVDD or VMID drop below the minimum threshold Vpor_off.

If AVDD is removed at any time, the internal Power On Reset circuit is powered down and PORB will follow AVDD.

In most applications the time required for the device to release PORB high will be determined by the charge time of the VMID node.

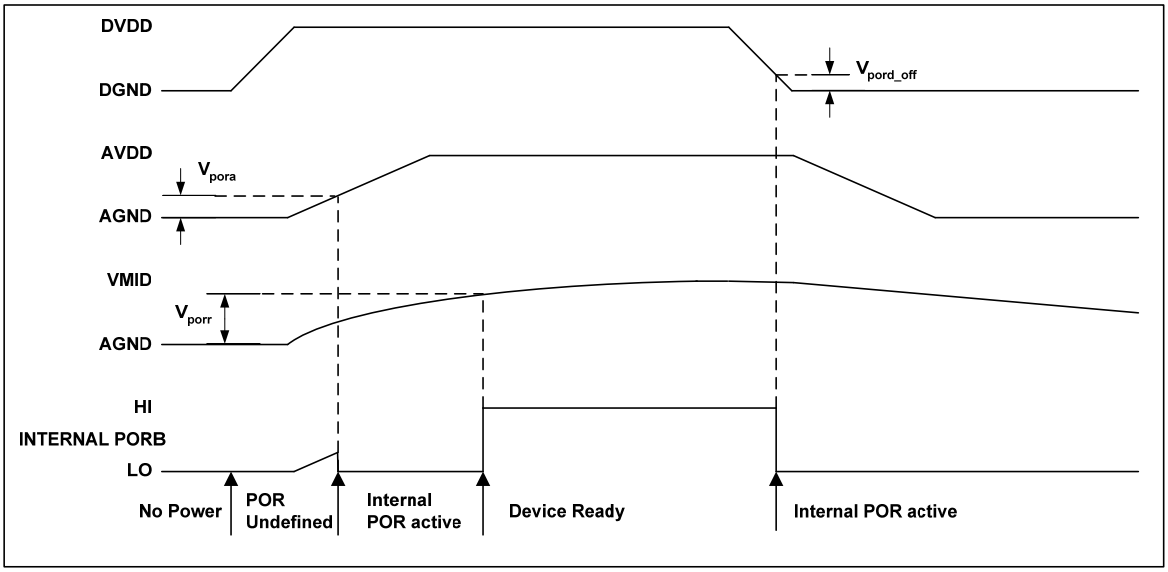


Figure 5 Typical Power Up Sequence Where DVDD is Powered Before AVDD

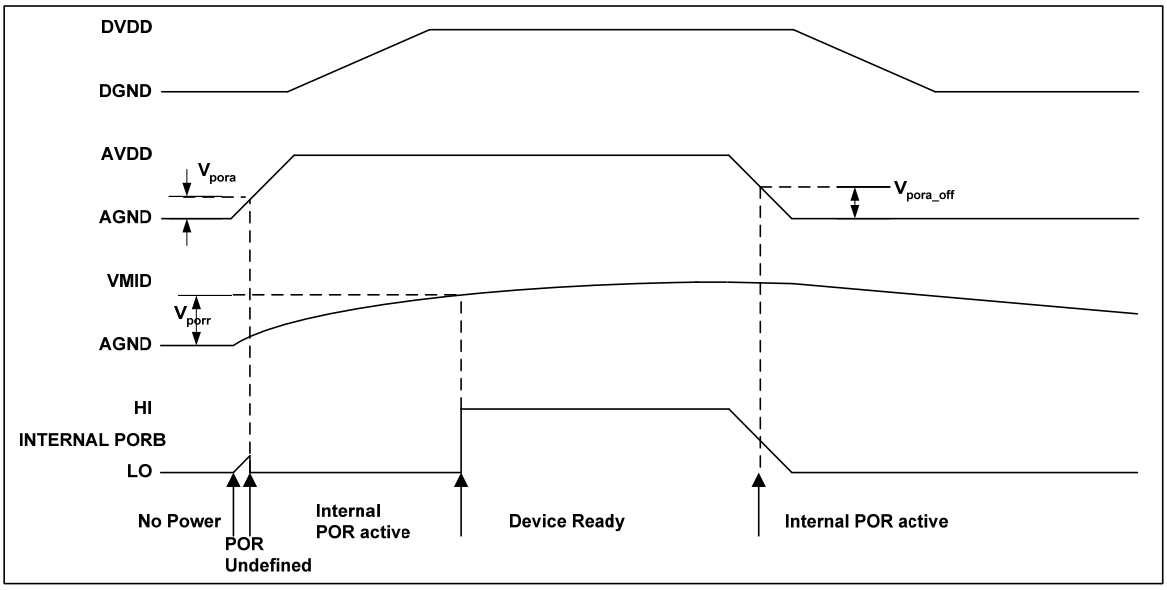


Figure 6 Typical Power Up Sequence Where AVDD is Powered Before DVDD

Typical POR Operation (typical values, not tested)

SYMBOL	MIN	TYP	MAX	UNIT
V_{pora}	0.5	0.7	1.0	V
V_{porr}	0.5	0.7	1.1	V
V_{pora_off}	1.0	1.4	2.0	V
V_{pord_off}	0.6	0.8	1.0	V

In a real application the designer is unlikely to have control of the relative power up sequence of AVDD and DVDD. Using the POR circuit to monitor VMID ensures a reasonable delay between applying power to the device and Device Ready.

Figure 5 and Figure 6 show typical power up scenarios in a real system. Both AVDD and DVDD must be established and VMID must have reached the threshold Vporr before the device is ready and can be written to. Any writes to the device before Device Ready will be ignored.

Figure 5 shows DVDD powering up before AVDD. Figure 6 shows AVDD powering up before DVDD. In both cases, the time from applying power to Device Ready is dominated by the charge time of VMID.

A 10uF cap is recommended for decoupling on VMID. The charge time for VMID will dominate the time required for the device to become ready after power is applied. The time required for VMID to reach the threshold is a function of the VMID resistor string and the decoupling capacitor. The Resistor string has a typical equivalent resistance of 33kohm (+/-20%). Assuming a 10uF capacitor, the time required for VMID to reach threshold of 1V is approx 74ms.

DEVICE DESCRIPTION

INTRODUCTION

The WM8718 is a high performance DAC designed for digital consumer audio applications. Its range of features makes it ideally suited for use in DVD players, AV receivers and other high-end consumer audio equipment.

WM8718 is a complete 2-channel differential stereo audio digital-to-analogue converter, including digital interpolation filter, multi-bit sigma delta with dither, switched capacitor multi-bit stereo DAC. The WM8718 includes an on-chip digital volume control, configurable digital audio interface and a 3 wire MPU control interface. The WM8718 has left and right zero flag output pins, allowing the user to control external muting circuits. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs.

The software control interface may be asynchronous to the audio data interface. The control data will be re-synchronised to the audio processing internally.

Operation using a master clock of 256fs, 384fs, 512fs or 768fs is provided, selection between clock rates being automatically controlled. Sample rates (fs) from less than 8kHz to 192kHz are allowed, provided the appropriate master clock is input. The audio data interface supports right justified, left justified and I^2S (Philips left justified, one bit delayed) interface formats along with a highly flexible DSP serial port interface.

The device is packaged in a small 20-lead SSOP.

CLOCKING SCHEMES

In a typical digital audio system there is one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master system clock can be applied directly through the MCLK input pin with no software configuration necessary for sample rate selection.

Note that on the WM8718, MCLK is used to derive clocks for the DAC path. The DAC path consists of DAC sampling clock, DAC digital filter clock and DAC digital audio interface timing. In a system where there are a number of possible sources for the reference clock, it is recommended that the clock source with the lowest jitter be used to optimise the performance of the DAC.

DIGITAL AUDIO INTERFACE

Audio data is applied to the internal DAC filters via the Digital Audio Interface. Five popular interface formats are supported:

- Left Justified mode
- Right Justified mode
- I^2S mode
- DSP Mode A
- DSP Mode B

All five formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits with the exception that 32 bit data is not supported in right justified mode. DIN and LRCIN maybe configured to be sampled on the rising or falling edge of BCKIN.

In left justified, right justified and I^2S modes, the digital audio interface receives data on the DIN input. Audio Data is time multiplexed with LRCIN indicating whether the left or right channel is present. LRCIN is also used as a timing reference to indicate the beginning or end of the data words. The minimum number of BCKINs per LRCIN period is 2 times the selected word length. LRCIN must be high for a minimum of word length BCKINs and low for a minimum of word length BCKINs. Any mark to space ratio on LRCIN is acceptable provided the above requirements are met.

The WM8718 will automatically detect when data with a LRCIN period of exactly 32 BCKINs is sent, and select 16-bit mode - overriding any previously programmed word length. Word length will revert to a programmed value only if a LRCIN period other than 32 BCKINs is detected.

In DSP Mode A or DSP Mode B, the data is time multiplexed onto DIN. LRCIN is used as a frame sync signal to identify the MSB of the first word. The minimum number of BCKINs per LRCIN period is 2 times the selected word length. Any mark to space ratio is acceptable on LRCIN provided the rising edge is correctly positioned. (See Figure 10 and Figure 11)

LEFT JUSTIFIED MODE

In left justified mode, the MSB is sampled on the first rising edge of BCKIN following a LRCIN transition. LRCIN is high during the left data word and low during the right data word.

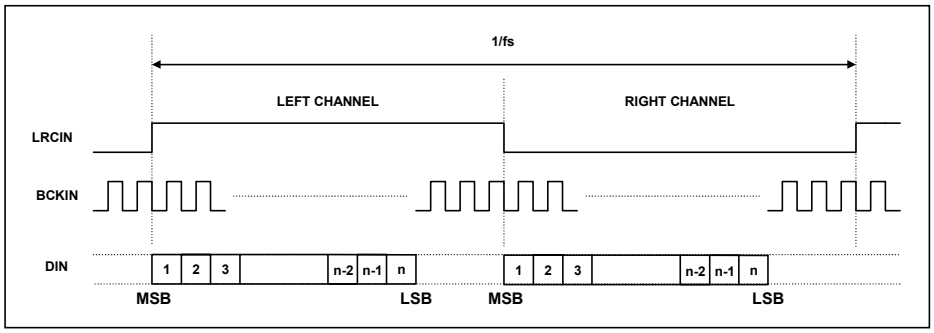


Figure 7 Left Justified Mode Timing Diagram

RIGHT JUSTIFIED MODE

In right justified mode, the LSB is sampled on the rising edge of BCKIN preceding a LRCIN transition. LRCIN is high during the left data word and low during the right data word.

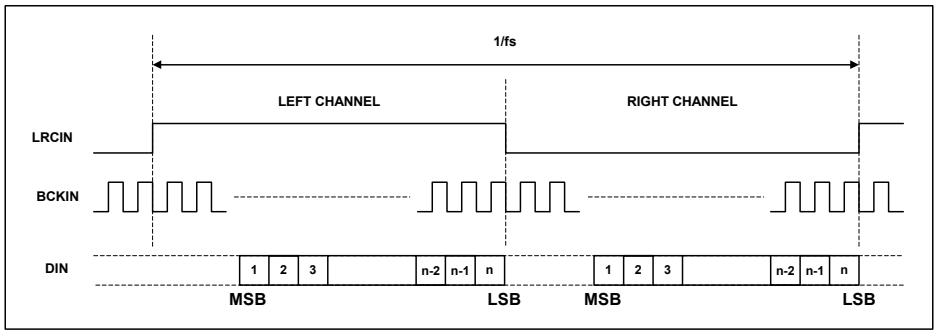


Figure 8 Right Justified Mode Timing Diagram

I²S MODE

In I²S mode, the MSB is sampled on the second rising edge of BCKIN following a LRCIN transition. LRCIN is low during the left data word and high during the right data word.

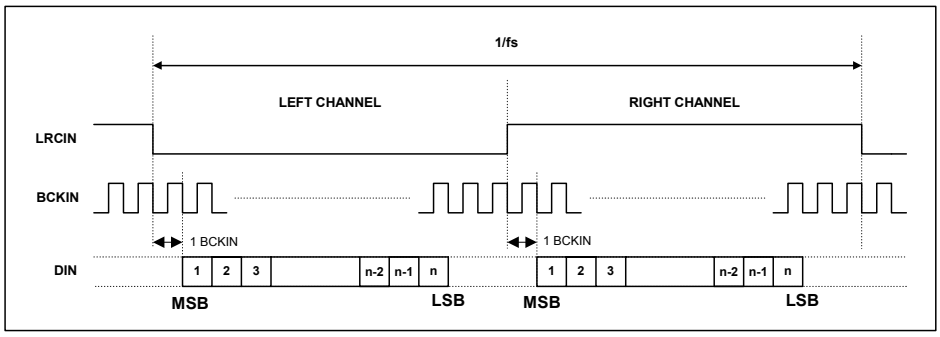


Figure 9 I²S Mode Timing Diagram

DSP MODE A

In DSP Mode A, the first bit is sampled on the BCKIN rising edge following the one that detects a low to high transition on LRCIN. No BCKIN edges are allowed between the data words. The word order is DIN left, DIN right.

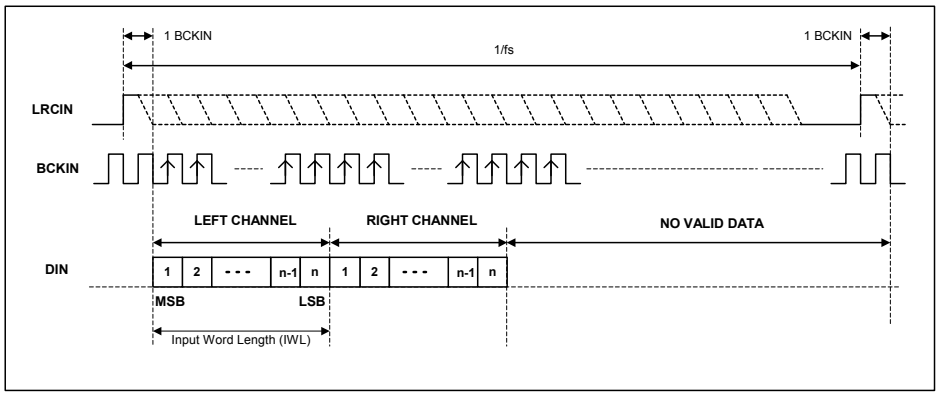


Figure 10 DSP Mode A Timing Diagram

DSP MODE B

In DSP Mode B, the first bit is sampled on the BCKIN rising edge, which detects a low to high transition on LRCIN. No BCKIN edges are allowed between the data words. The word order is DIN left, DIN right.

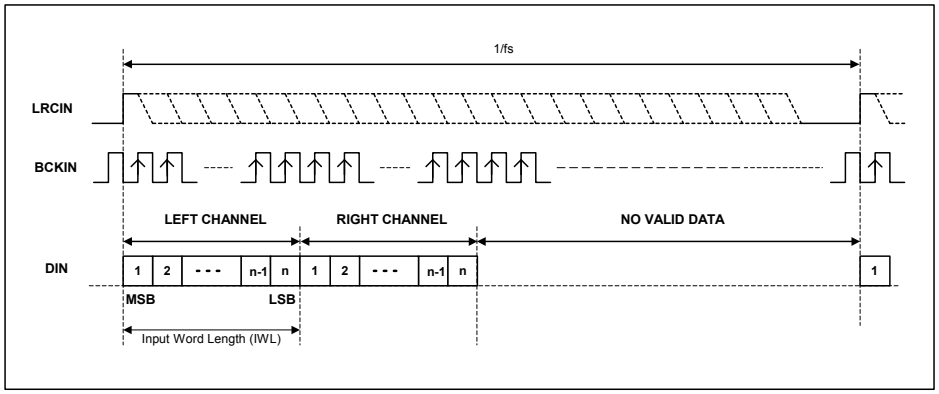


Figure 11 DSP Mode B Timing Diagram

AUDIO DATA SAMPLING RATES

The master clock for WM8718 can range from 128fs to 768fs where fs is the audio sampling frequency (LRCIN), typically 32kHz, 44.1kHz, 48kHz, 96kHz or 192kHz. The master clock is used to operate the digital filters and the noise shaping circuits.

The WM8718 has a master clock detection circuit that automatically determines the relationship between the master clock frequency and the sampling rate (to within +/- 32 system clocks). If there is greater than 32 clocks error, the system will default to 768fs. The master clock should be synchronised with LRCIN, although the WM8718 is tolerant of phase differences or jitter on this clock. See Table 1.

SAMPLING RATE (LRCIN)	MASTER CLOCK FREQUENCY (MHz) (MCLK)					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
48kHz	6.144	9.216	12.288	18.432	24.576	36.864
88.2kHz	11.2896	16.9344	22.5792	33.8688	Unavailable	Unavailable
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
176.4kHz	22.5792	33.8688	Unavailable	Unavailable	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

Table 1 Typical Relationships between Master Clock Frequency and Sampling Rate

SOFTWARE CONTROL INTERFACE

The software control interface may be operated using a 3-wire (SPI-compatible) interface. In this mode, SDIN is used for the program data, SCLK is used to clock in the program data and LATCH is used to latch in the program data. The 3-wire interface protocol is shown in Figure 12.

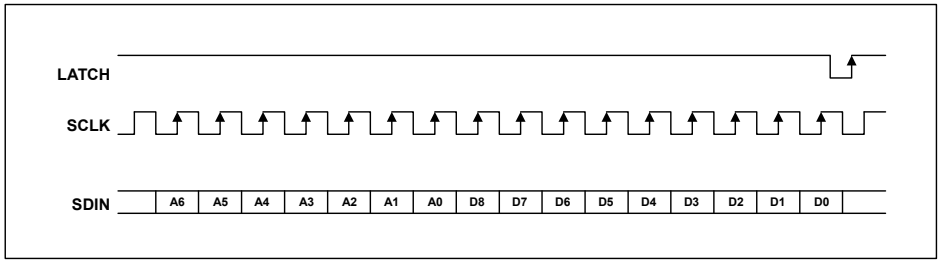


Figure 12 3-Wire Serial Control Interface

Notes:

1. A[6:0] are Control Address Bits
2. D[8:0] are Control Data Bits

REGISTER MAP

WM8718 uses a total of 4 program registers, which are 16-bits long. These registers are all loaded through input pin SDIN, using the 3-wire serial control mode as shown in 9.

	A6	A5	A4	A3	A2	A1	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0
M0	0	0	0	0	0	0	0	UPDATEL	LAT7	LAT6	LAT5	LAT4	LAT3	LAT2	LAT1	LAT0
M1	0	0	0	0	0	0	1	UPDATER	RAT7	RAT6	RAT5	RAT4	RAT3	RAT2	RAT1	RAT0
M2	0	0	0	0	0	1	0	ZCDINIT	ZEROFLR	0[1]	0[1]	0[1]	0[1]	PWDN	DEEMPH	MUT
M3	0	0	0	0	0	1	1	0[1]	REV	BCP	ATC	LRP	FMT[1]	FMT[0]	IWL[1]	IWL[0]
	ADDRESS							**DATA**								

Table 2 Mapping of Program Registers

Note:

1. These register bits must be written as 0 otherwise device function cannot be guaranteed.

REGISTER ADDRESS (A3,A2,A1,A0)	BITS	NAME	DEFAULT	DESCRIPTION
0000 DACL Attenuation	[7:0]	LAT[7:0]	11111111 (0dB)	Attenuation data for left channel in 0.5dB steps, see Table 5
	8	UPDATEL	0	Attenuation data load control for left channel. 0: Store DACL in intermediate latch (no change to output) 1: Store DACL and update attenuation on both channels.
0001 DACR Attenuation	[7:0]	RAT[7:0]	11111111 (0dB)	Attenuation data for right channel in 0.5dB steps, see Table 5
	8	UPDATER	0	Attenuation data load control for right channel. 0: Store DACR in intermediate latch (no change to output) 1: Store DACR and update attenuation on both channels.
0010 Mode Control	0	MUT	0	Left and Right DACs Soft Mute Control. 0: No mute 1: Mute
	1	DEEMPH	0	De-emphasis Control. 0: De-emphasis off 1: De-emphasis on
	2	PWDN	0	Left and Right DACs Power-down Control 0: All DACs running, output is active 1: All DACs in power saving mode, output muted
	7	ZEROFLR	0	Zero Flag Pin Control. 0: Channel independent 1: AND of both channels on ZEROFL output pin
	8	ZCDINIT	0	Zero Cross Detect Control. 0: Zero cross detect enabled 1: Zero cross detect disabled
0011 Format Control	[1:0]	IWL[1:0]	10	Input Word Length. 00: 16-bit mode 01: 20-bit mode 10: 24-bit mode 11: 32-bit mode(not supported in right justified mode)

REGISTER ADDRESS (A3,A2,A1,A0)	BITS	NAME	DEFAULT	DESCRIPTION
	[3:2]	FMT[1:0]	10	Audio Data Format Select. 00: right justified mode 01: left justified mode 10: I^2S mode 11: DSP mode
	4	LRP	0	Polarity Select for LRCIN/DSP Mode Select. 0: normal LRCIN polarity/DSP late mode 1: inverted LRCIN polarity/DSP early mode
	5	ATC	0	Attenuator Control. 0: All DACs use attenuation as programmed. 1: Right channel DACs use corresponding left DAC attenuation
	6	BCP	0	BCKIN Polarity 0: normal polarity 1: inverted polarity
	7	REV	0	Output Phase Reversal, see Table 10

Table 3 Register Bit Descriptions

ATTENUATION CONTROL

Each DAC channel can be attenuated digitally before being applied to the digital filter. Attenuation is 0dB by default but can be set between 0 and 127.5dB in 0.5dB steps using the 8 Attenuation control bits. All attenuation registers are double latched allowing new values to be pre-latched to both channels before being updated synchronously. Setting the UPDATE bit on any attenuation write will cause all pre-latched values to be immediately applied to the DAC channels.

REGISTER ADDRESS	BITS	LABEL	DEFAULT	DESCRIPTION
0000 Attenuation DACL	[7:0]	LAT[7:0]	11111111 (0dB)	Attenuation data for Left Channel DACL in 0.5dB steps.
	8	UPDATEL	0	Controls simultaneous update of all Attenuation Latches 0: Store DACL in intermediate latch (no change to output) 1: Store DACL and update attenuation on all channels.
0001 Attenuation DACR	[7:0]	RAT[7:0]	11111111 (0dB)	Attenuation data for Right channel DACR in 0.5dB steps.
	8	UPDATER	0	Controls simultaneous update of all Attenuation Latches 0: Store DACR in intermediate latch (no change to output) 1: Store DACR and update attenuation on all channels.

Table 4 Attenuation Register Map

Note:

1. The UPDATE bit is not latched. If UPDATE=0, the Attenuation value will be written to the pre-latch but not applied to the relevant DAC. If UPDATE=1, all pre-latched values and the current value being written will be applied on the next input sample.
2. Care should be used in reducing the attenuation as rapid large volume changes can introduce zipper noise if the ZCDINIT register bit has been set, (disabled).

DAC OUTPUT ATTENUATION

Registers DACR and DACL control the left and right channel attenuation. Table 9 shows how the attenuation levels are selected from the 8-bit words.

DACX[7:0]	ATTENUATION LEVEL
00(hex)	∞dB (mute)
01(hex)	127.5dB
:	:
:	:
:	:
FE(hex)	0.5dB
FF(hex)	0dB

Table 5 Attenuation Control Levels

MUTE MODES

Figure 13 shows the application and release of MUTE whilst a full amplitude sinusoid is being played at 48kHz sampling rate. When MUTE (lower trace) is asserted, the output (upper trace) begins to decay exponentially from the DC level of the last input sample. The output will decay towards V_{MID} with a time constant of approximately 64 input samples. When MUTE is de-asserted, the output will restart almost immediately from the current input sample.

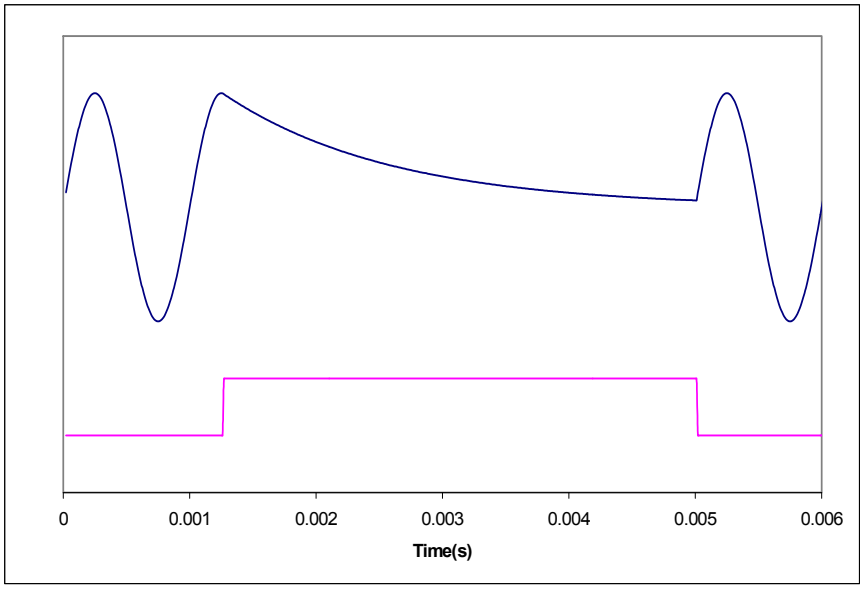


Figure 13 Application and Release of Soft Mute

Setting the MUT register bit will apply a 'soft' mute to the input of the digital filters:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0010 Mode Control	0	MUT	0	Soft Mute select 0: Normal Operation 1: Soft mute both channels

DE-EMPHASIS MODE

Setting the DEEMPH register bit puts the digital filters into de-emphasis mode:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0010 Mode Control	1	DEEMPH	0	De-emphasis mode select: 0: De-emphasis Off 1: De-emphasis On

POWERDOWN MODE

Setting the PWDN register bit immediately connects all outputs to V_{MID} and selects a low power mode. All trace of the previous input samples is removed, but all control register settings are preserved. When PWDN is cleared again the first 16 input samples will be ignored, as the FIR will repeat it's power-on initialisation sequence.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0010 Mode Control	2	PWDN	0	Power Down Mode Select: 0: Normal Mode 1: Power Down Mode

ZERO FLAG OUTPUTS

The WM8718 has two zero flag outputs pins. The WM8718 asserts a low on the corresponding zero flag pin when a sequence of more than 1024 mid-rail signal is input to the chip. The user can use the zero flag pins to control external muting circuits if required. To simplify external circuitry there is an option to have both zero flag output's ANDed internally and output on both pins.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0010 Mode Control	7	ZEROFLR	0	ZERO Flag Outputs: 0: Both pins enabled. 1: AND of both channels to both pins.

ZERO CROSS DETECT

When the WM8718 receives updates to the volume levels it will, by default, wait for the signal to pass through mid-rail for each channel before applying the update for that particular channel. This ensures that there is minimum distortion seen on the output when the volume is changed.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0010 Mode Control	8	ZCDINIT	0	Zero Cross Detect Control: 0: Enabled 1: Disabled

SELECTION OF LRCIN POLARITY

In left justified, right justified or I^2S modes, the LRP register bit controls the polarity of LRCIN. If this bit is set high, the expected polarity of LRCIN will be the opposite of that shown in Figure 7, Figure 8 and Figure 9. Note that if this feature is used as a means of swapping the left and right channels, a 1 sample phase difference will be introduced.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0011 Format Control	4	LRP	0	LRCIN Polarity (normal) 0: normal LRCIN polarity 1: inverted LRCIN polarity

Table 6 LRCIN Polarity Control

In DSP modes, the LRCIN register bit is used to select between early and late modes (see Figure 10 and Figure 11.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0011 Format Control	4	LRP	0	DSP Format (DSP modes) 0: Late DSP mode 1: Early DSP mode

Table 7 DSP Format Control

In DSP early mode, the first bit is sampled on the BCKIN rising edge following the one that detects a low to high transition on LRCIN. In DSP late mode, the first bit is sampled on the BCKIN rising edge, which detects a low to high transition on LRCIN. No BCKIN edges are allowed between the data words. The word order is DIN left, DIN right.

ATTENUATOR CONTROL MODE

Setting the ATC register bit causes the left channel attenuation settings to be applied to both left and right channel DACs from the next audio input sample. No update to the attenuation registers is required for ATC to take effect. (The right channels registry settings are preserved.)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0011 PCM Control	5	ATC	0	Attenuator Control Mode: 0: Right channels use Right attenuation 1: Right Channels use Left Attenuation

Table 8 Attenuation Control Select

BCKIN POLARITY

By default, LRCIN and DIN are sampled on the rising edge of BCKIN and should ideally change on the falling edge. Data sources which change LRCIN and DIN on the rising edge of BCKIN can be supported by setting the BCP register bit. Setting BCP to 1 inverts the polarity of BCKIN to the inverse of that shown in Figure 7, Figure 8, Figure 9, Figure 10 and Figure 11

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0011 PCM Control	6	BCP	0	BCKIN 0: normal polarity 1: inverted polarity

Table 9 BCKIN Polarity Control

OUTPUT PHASE REVERSAL

The REV register bit controls the phase of the output signal. Setting the REV bit causes the phase of the output signal to be inverted.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0011 PCM Control	7	REV	0	Analogue Output Phase 0: Normal 1: Inverted

Table 10 Output Phase Control

DIGITAL AUDIO INTERFACE CONTROL REGISTERS

The WM8718 has a fully featured PCM digital audio interface whose interface format is selected via the FMT [1:0] and IWL[1:0] register bits in register M3.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0010 Format Control	1:0	IWL[1:0]	00	Interface format Select
0010 Format Control	3:2	FMT[1:0]	00	Interface format Select

Table 11 Interface Format Controls

FMT[1]	FMT[0]	IWL[1]	IWL[0]	AUDIO INTERFACE DESCRIPTION (NOTE 1)
0	0	0	0	16 bit right justified mode
0	0	0	1	20 bit right justified mode
0	0	1	0	24 bit right justified mode
0	0	1	1	Not available
0	1	0	0	16 bit left justified mode
0	1	0	1	20 bit left justified mode
0	1	1	0	24 bit left justified mode
0	1	1	1	32 bit left justified mode
1	0	0	0	16 bit I^2S mode
1	0	0	1	20 bit I^2S mode
1	0	1	0	24 bit I^2S mode
1	0	1	1	32 bit I^2S mode
1	1	0	0	16 bit DSP mode
1	1	0	1	20 bit DSP mode
1	1	1	0	24 bit DSP mode
1	1	1	1	32 bit DSP mode

Table 12 Audio Data Input Format

Note:

1. In all modes, the data is signed 2's complement. The digital filters always input 24-bit data. If the DAC is programmed to receive 16 or 20 bit data, the WM8718 pads the unused LSBs with ZEROS. If the DAC is programmed into 32-bit mode, the 8 LSBs are treated as zero.

DIGITAL FILTER CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband Edge		-3dB		0.487fs		
Passband Ripple		f < 0.444fs			±0.05	dB
Stopband Attenuation		f > 0.555fs	-60			dB
Group Delay				28		fs

Table 13 Digital Filter Characteristics

DAC FILTER RESPONSES

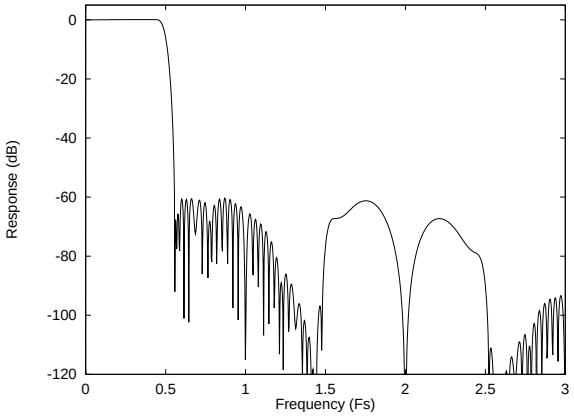


Figure 14 DAC Digital Filter Frequency Response – 44.1, 48 and 96kHz

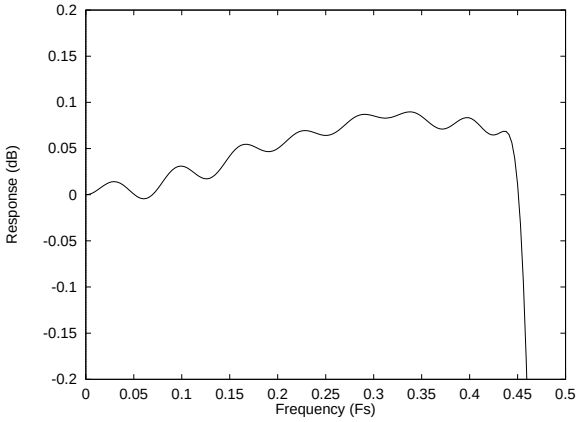


Figure 15 DAC Digital Filter Ripple – 44.1, 48 and 96kHz

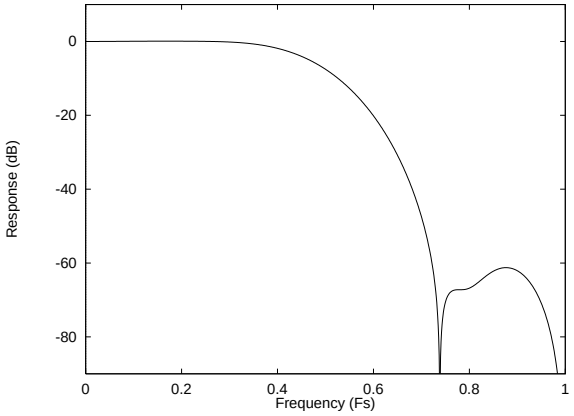


Figure 16 DAC Digital Filter Frequency Response – 192kHz

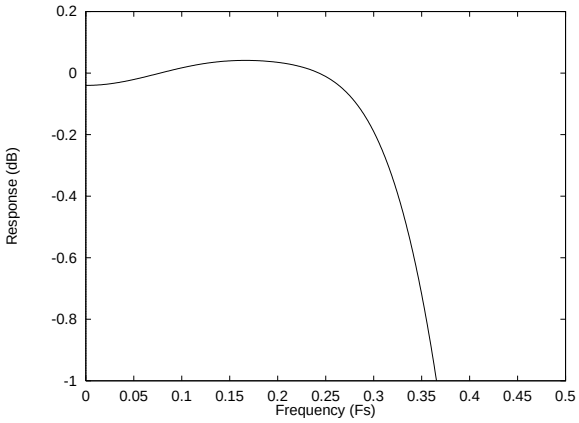


Figure 17 DAC Digital Filter Ripple – 192kHz

DIGITAL DE-EMPHASIS CHARACTERISTICS

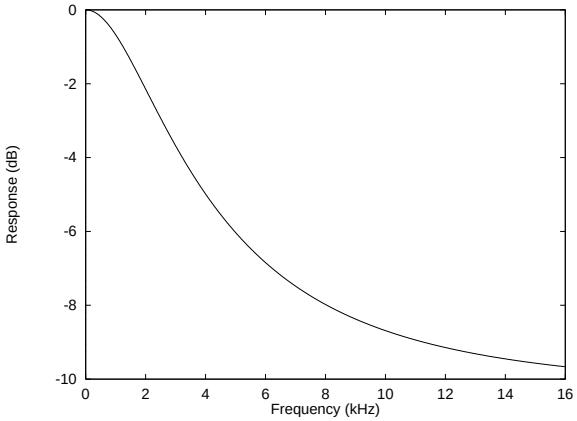


Figure 18 De-Emphasis Frequency Response (32kHz)

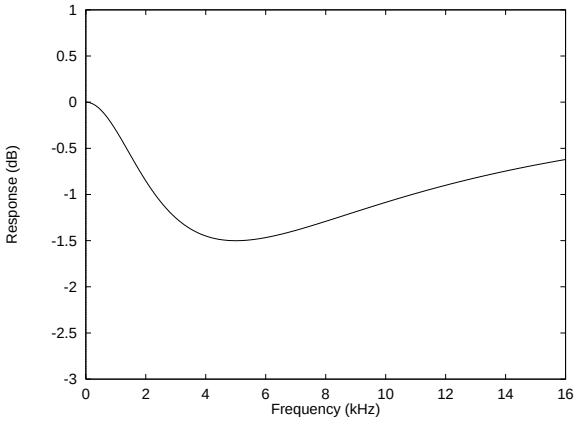


Figure 19 De-Emphasis Error (32kHz)

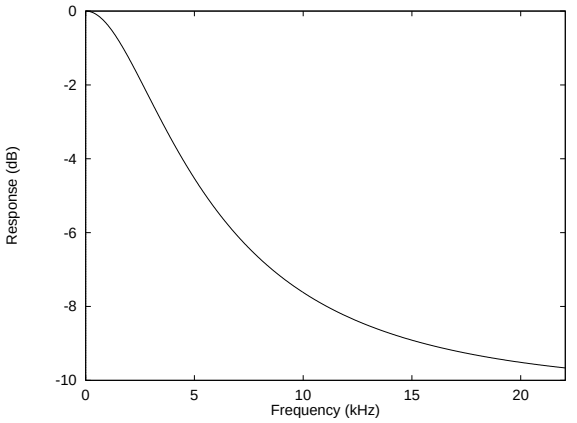


Figure 20 De-Emphasis Frequency Response (44.1kHz)

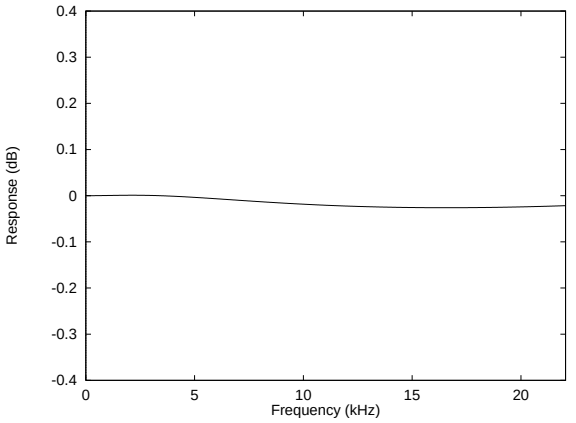


Figure 21 De-Emphasis Error (44.1kHz)

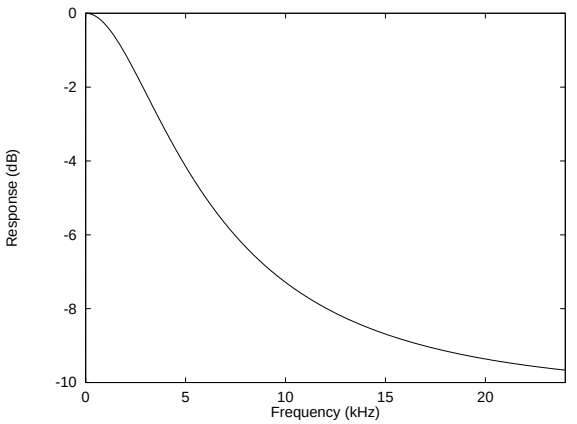


Figure 22 De-Emphasis Frequency Response (48kHz)

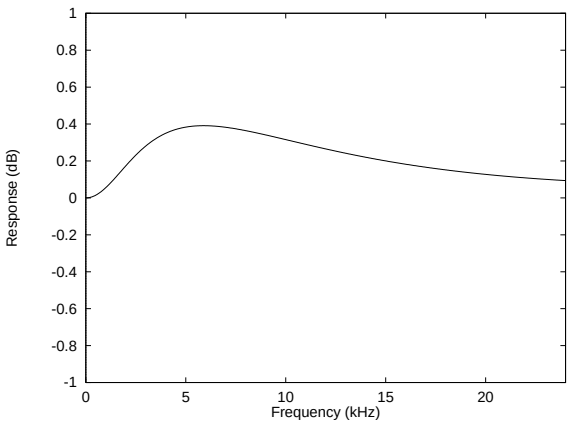


Figure 23 De-Emphasis Error (48kHz)

TYPICAL PERFORMANCE

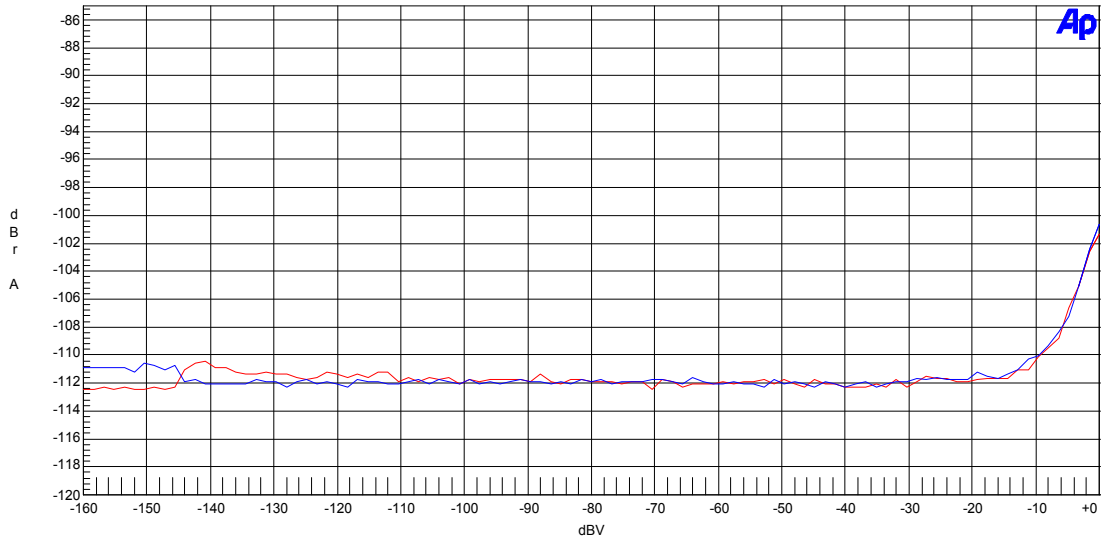


Figure 24 THD+N versus Input Amplitude (@ 1kHz, 'A' weighted)

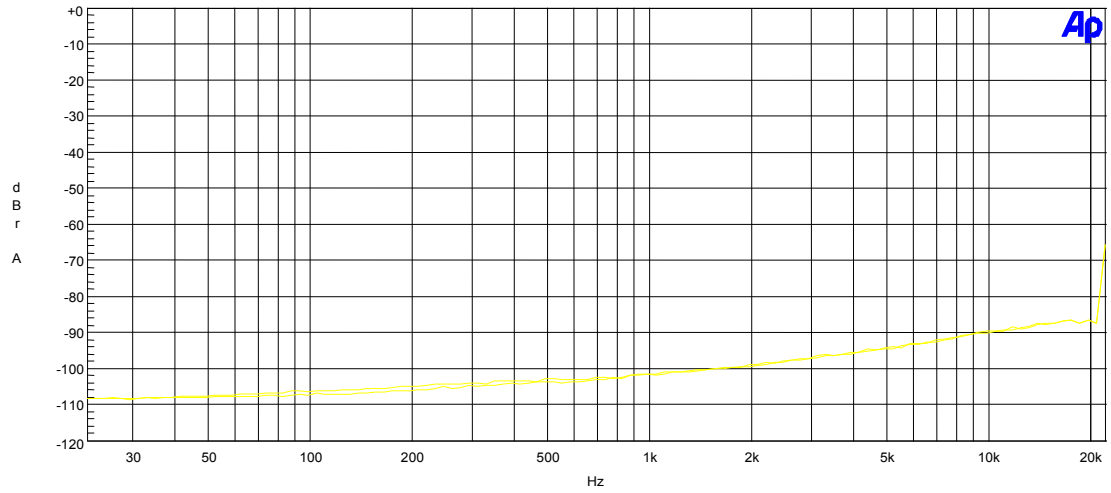
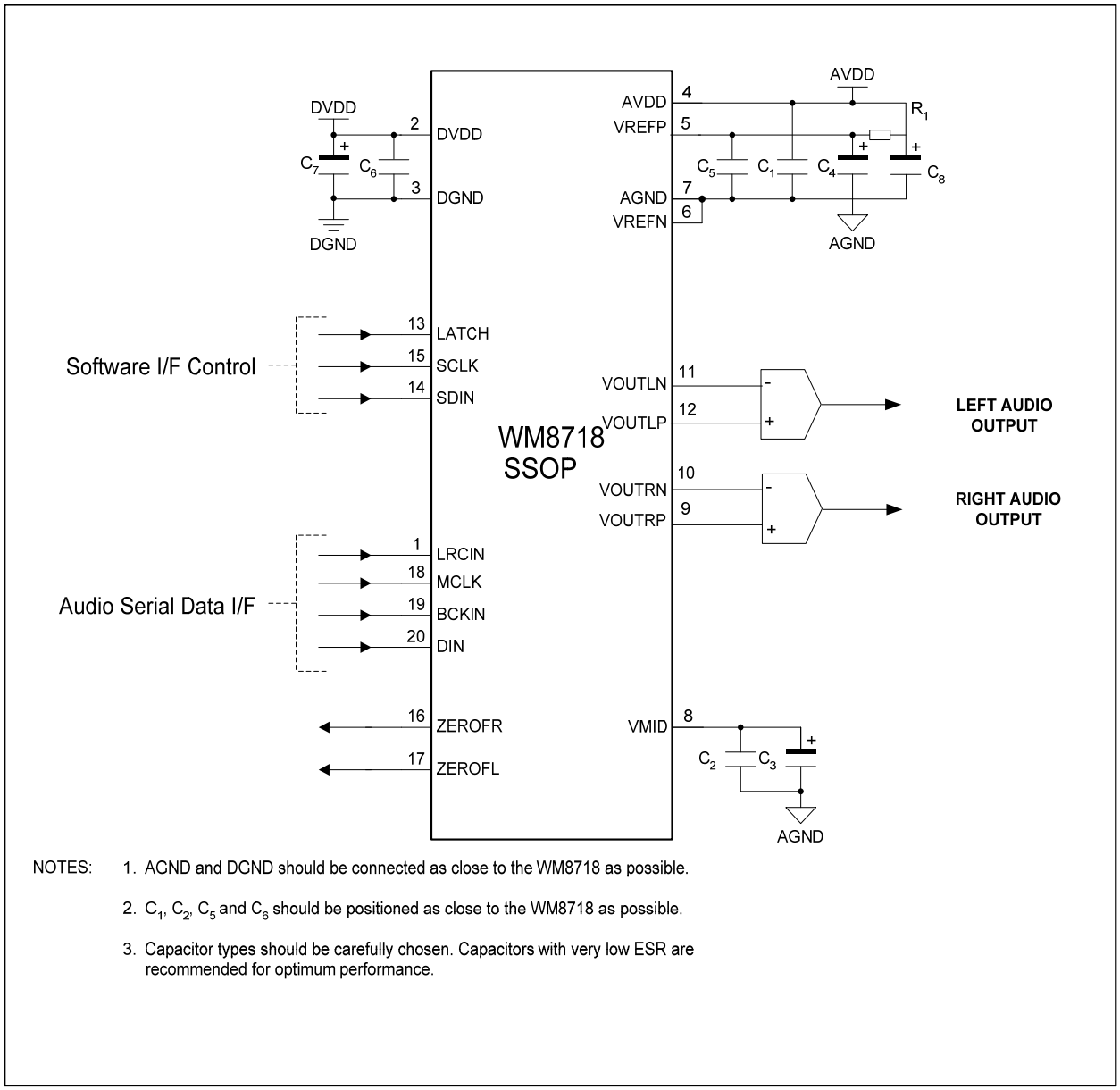


Figure 25 THD+N versus Frequency ('A' weighted)

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS



NOTES:
1. AGND and DGND should be connected as close to the WM8718 as possible.
2. C_1, C_2, C_5 and C_6 should be positioned as close to the WM8718 as possible.
3. Capacitor types should be carefully chosen. Capacitors with very low ESR are recommended for optimum performance.

Figure 26 External Components Diagram

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C4 and C7	10μF	De-coupling for DVDD and AVDD
C1 and C6	0.1μF	De-coupling for DVDD and AVDD
C5	0.1uF	De-coupling for VREFP positive DAC reference supply
C2	0.1μF	Reference de-coupling capacitors for VMID pin.
C3	10μF	
C8	10μF	Filtering for VREFP. Omit if AVDD low noise.
R1	33Ω	Filtering for VREP. Use 0Ω if AVDD low noise.

Table 14 External Components Description

RECOMMENDED ANALOGUE LOW PASS FILTER FOR PCM DATA FORMAT (OPTIONAL)

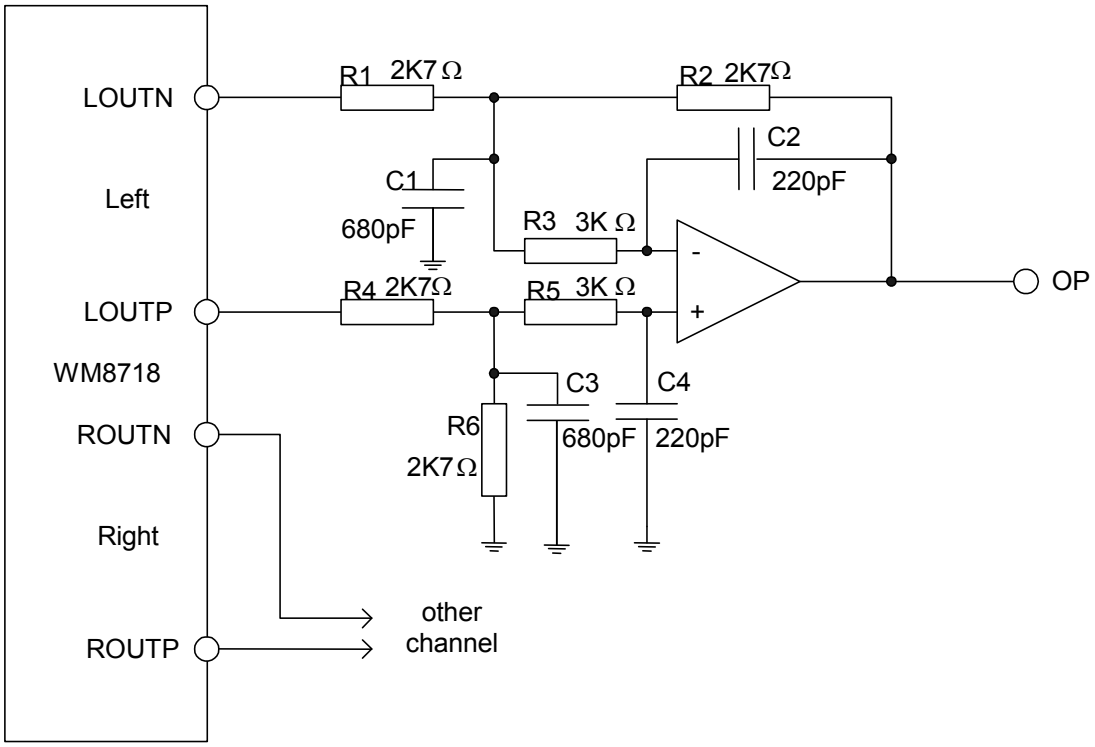


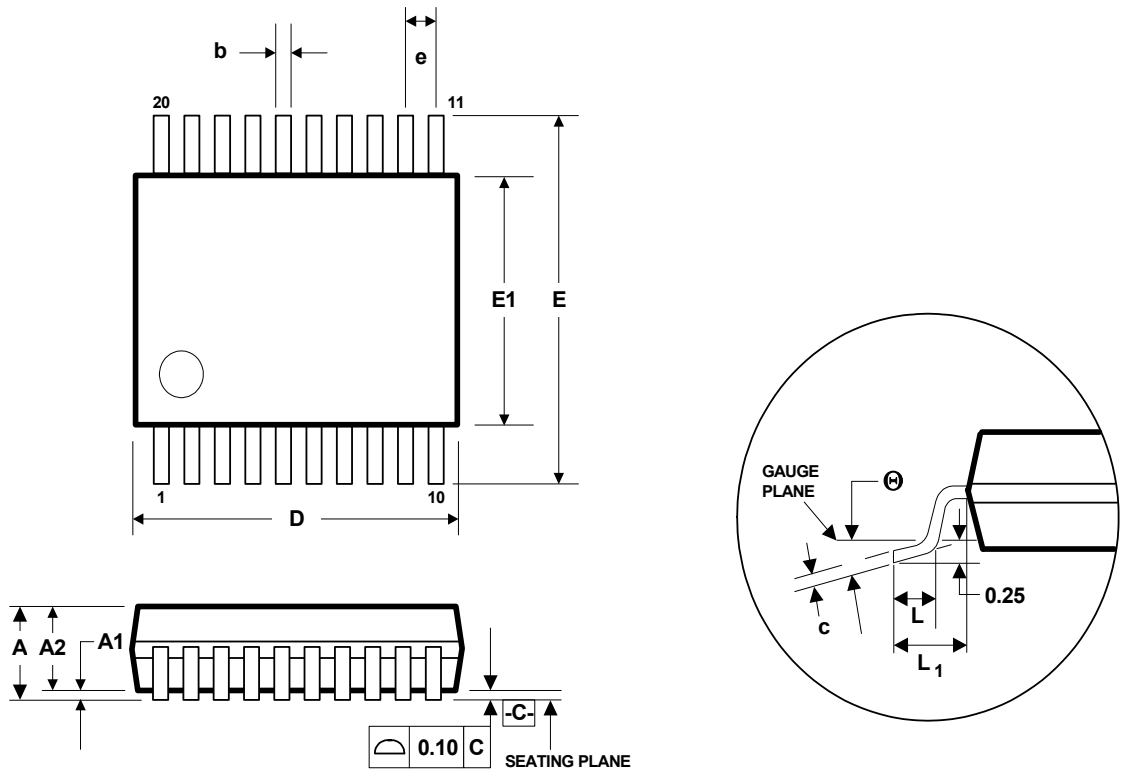
Figure 27 Recommended Low Pass Filter (Optional)

Note:

1. Additional information on suitable output filters can be found in Application Note WAN0171.

PACKAGE DIMENSIONS

DS: 20 PIN SSOP (7.2 x 5.3 x 1.75 mm) **DM0015.C**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	-----
A_2	1.65	1.75	1.85
b	0.22	0.30	0.38
c	0.09	-----	0.25
D	6.90	7.20	7.50
e		0.65 BSC	
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
L_1		1.25 REF	
θ	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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REVISION HISTORY

DATE	REV	ORIGINATOR	CHANGES
29/08/11	4.6	JMacD	WM8718GEFL/V / WM8718GEFL/RV and QFN references removed.