CS1084

AUTOMOTIVE GRADE

Vacuum Fluorescent Display Tube Driver

Description

The VFD Driver is a microprocessor interface IC that drives a multiplexed VF (Vacuum Fluorescent) display tube. It consists of a 32-bit shift register, a 32-bit transparent data latch, a metal mask ROM, six 20mA anode output drivers, twenty-three 2mA anode output drivers, and three 50mA grid drivers with output enables. The metal mask programmable ROM (at factory request) allows the 29 anode outputs and 3 grid outputs to be assigned to any of the 32 serial data bits.

Features

- Metal Mask ROM
- Six 20mA Anode drivers
- Twenty-three, 2mA Anode Drivers
- Three, 50mA Grid Drivers
- Power on Reset
- Display Dimming Possible

Absolute Maximum Ratings

Supply Voltage (V_{BB}) ....-0.6V to 18.0V
Input Voltages (D_{IN}, CLK, STB, GREN) ....-0.6V to 6.0V
Maximum Power Dissipation (@T_A = 105°C)...1.0W
Junction Temperature Range ....-40°C to 150°C
Storage Temperature Range..-55°C to 150°C
ESD Susceptibility (Human Body Model) 2kV
ESD Susceptibility (Machine Model) 200V
Lead Temperature Soldering
    Wave Solder(through hole styles only)...........10 sec. max, 260°C peak
    Reflow (SMD styles only)...........60 sec. max above 183°C, 230°C peak
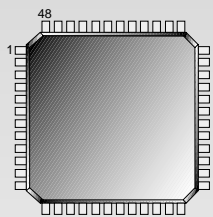
Package Options

40 Lead PDIP
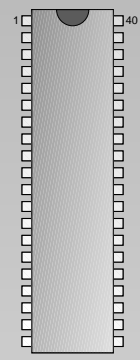
44 Lead PLCC
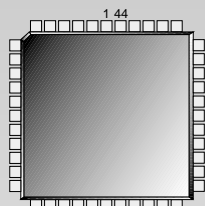
48 Lead LQFP

Application Diagram
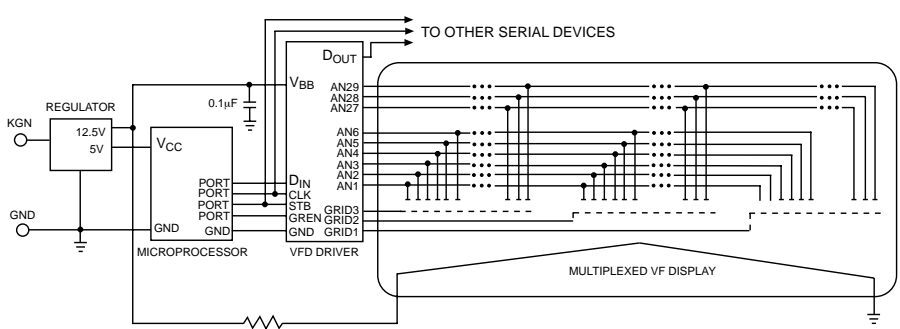
Cherry Semiconductor

Electrical Characteristics: $8.0V \leq V_{BB} \leq 16.5V$, Gnd = 0V, $-40°C \leq T_A \leq 105°C$, the sign (+ or -) refers to the direction of the current (positive current goes into the lead); unless otherwise stated					
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ V_{BB} Input					
V_{BB} input voltage		8.0		16.5	V
I_{BB0} Current	No outputs active, V_{BB} = 12.5V		29	38	mA
	No outputs active, V_{BB} = 16.5V		30	40	mA
I_{BB2} Current per active 2mA output	No load on grid and anode outputs, V_{BB} = 16.5V		0.20	0.45	mA
I_{BB20} Current per active 20mA output	No load on grid and anode outputs, V_{BB} = 16.5V		2.0	4.0	mA
I_{BB50} Current per active 50mA output	No load on grid and anode outputs, V_{BB} = 16.5V		6.0	9.0	mA
■ DIN, CLK, STB Inputs					
V_{ILl}, input low voltage				1.575	V
V_{IH}, input high voltage		3.325			V
I_{IL}, input current	$V_{IN} = V_{IH}$	0		20	μA
■ GREN Input					
V_{IL}, input low voltage				1.575	V
V_{IH}, input high voltage		3.325			V
I_{IH}, input pull-down current	V_{IN} = 3.325V	30	90	170	μA
■ GRID1, GRID2, GRID3 Outputs					
V_{OL}	I_{OUT} = 1mA			0.5	V
V_{OH}	I_{OUT} = -50mA	V_{BB} - 0.5		V_{BB}	V
■ AN24-AN29 Outputs					
V_{OL}	I_{OUT} = 400μA			0.5	V
V_{OH}	I_{OUT} = -20mA	V_{BB} - 0.5		V_{BB}	V
■ AN1-AN23 Outputs					
V_{OL}	I_{OUT} = 100μA			0.5	V
V_{OG}	I_{OUT} = -2mA	V_{BB} - 0.5		V_{BB}	V
■ D_{OUT} Output					
V_{OL}	I_{OUT} = 1mA			0.5	V
V_{OH}	I_{OUT} = -1mA	3.8		5.0	V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics: $8.0V \leq V_{BB} \leq 16.5V$, Gnd = 0V, -40°C $\leq T_A \leq$ 105°C, the sign (+ or -) refers to the direction of the current (positive current goes into the lead); unless otherwise stated					

■ AC characteristics: Input and output timing

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_C, CLK Frequency		dc		600	kHz
T_{CL}, CLK low time		300			ns
T_{CH}, CLK high time		300			ns
T_{CR}, CLK rise time				100	ns
T_{CF}, CLK fall time				100	ns
T_{CD}, CLK low to D_{OUT} propagation delay				500	ns
T_{CS}, CLK low to STB high time		200			ns
T_{SC}, STB low to CLK high time		200			ns
T_{ST}, STB high time		500			ns
T_{AN}, STB high to anode output propagation delay				5.0	μs
T_{GL}, grid enable time				5.0	μs
T_{G0}, grid disable time				10.0	μs
T_{GR}, grid rise time		0.250		5.0	μs
T_{GF}, grid fall time		0.250		5.0	μs
T_{AR}, anode rise time		0.150		5.0	μs
T_{TF}, anode fall time		0.150		5.0	μs

Note: Grid and anode rise/fall times are measured from 10% and 90% points.

Output currents are at the maximum rated currents for the respective stages.

Package Lead Description

PACKAGE LEAD #			LEAD SYMBOL	FUNCTION
40L DIP	44L PLCC	48L LQFP	(29 Anode Configuration)	
1	14	8	GRID1	50mA grid output.
2	15	9	GRID2	50mA grid output.
3	16	10	GRID3	50mA grid output.
4	17	11	AN1	2mA anode output.
5	18	13	AN2	2mA anode output.
6	19	14	AN3	2mA anode output.
7	20	15	AN4	2mA anode output.
8	21	16	AN5	2mA anode output.
9	22	17	AN6	2mA anode output.
10	24	19	AN7	2mA anode output.
11	25	20	AN8	2mA anode output.
12	26	21	AN9	2mA anode output.
13	27	22	AN10	2mA anode output.
14	28	23	AN11	2mA anode output.
15	29	25	AN12	2mA anode output.
16	30	26	AN13	2mA anode output.

Package Lead Description: continued

| PACKAGE LEAD #			LEAD SYMBOL	FUNCTION
40L DIP	44L PLCC	48L LQFP	(29 Anode Configuration)	
17	31	27	AN14	2mA anode output.
18	32	28	AN15	2mA anode output.
19	33	29	AN16	2mA anode output.
20	35	31	Gnd	Ground connection.
21	36	32	AN17	2mA anode output.
22	37	33	AN18	2mA anode output.
23	38	34	AN19	2mA anode output.
24	39	35	AN20	2mA anode output.
25	40	37	AN21	2mA anode output.
26	41	38	AN22	2mA anode output.
27	42	39	AN23	2mA anode output.
28	43	40	AN24	20mA anode output.
29	44	41	AN25	20mA anode output.
30	2	43	AN26	20mA anode output.
31	3	44	AN27	20mA anode output.
32	4	45	AN28	20mA anode output.
33	5	46	AN29	20mA anode output.
34	6	47	D_{OUT}	Shift register data output.
35	7	1	D_{IN}	Shift register data input.
36	8	2	CLK	Shift register clock input.
37	9	3	STB	Transfer contents of shift registers to output stages.
38	10	4	GREN	Grid outputs enable.
39	1, 11, 12, 23, 34	5, 6, 12, 18, 24, 30, 36, 42, 48	NC	No Connection.
40	13	7	V_{BB}	Supply voltage input.

Operation Description

Upon the initial application of power, the power on reset function will cause all of the anode and grid driver outputs to be off and all shift register outputs to be set low. Data is fed into the shift register through the D_{IN} pin at the rising edge of the CLK input. Thirty two bits of data are capable of being stored by the shift register. Once the desired pattern is stored in the shift register, it can be transferred to the latch by setting the STB input high. The output of each latch drives its corresponding output stage. A logic high input to the shift register/latch will cause the corresponding output to turn on. A logic low input to the shift register/latch will cause the corresponding output to turn off. Please note that if the STB is held high, the outputs of the latch reflect the outputs of the corresponding shift register bits and will change if data is shifted in.

The three GRID outputs are gated by the GREN input. When GREN is low, the GRID outputs are forced low regardless of the state of the corresponding latch output. When GREN is high, the GRID outputs correspond to the state of their respective latch outputs. The anode outputs, AN1 to AN29 are always enabled.

The D_{OUT} pin is the output of the last stage of the shift register to allow serial cascading of this IC with other devices. Data from the last stage of the shift register is supplied to the D_{OUT} pin delayed by 1/2 CLK cycle. Data on the D_{OUT} output changes with the falling edges of the CLK to prevent logic race conditions between the CLK and the D_{IN} of the next IC in the serial chain.

Block Diagram

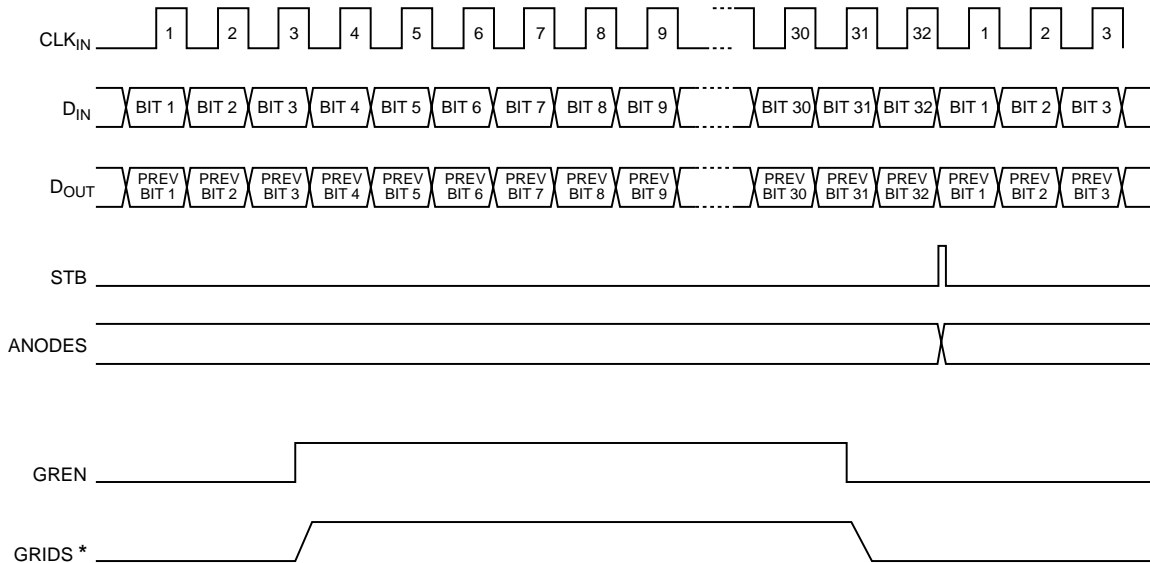

Output Drive Capability
Grid Outputs: 50mA
AN24 - AN29: 20mA
AN1 - AN23: 2mA
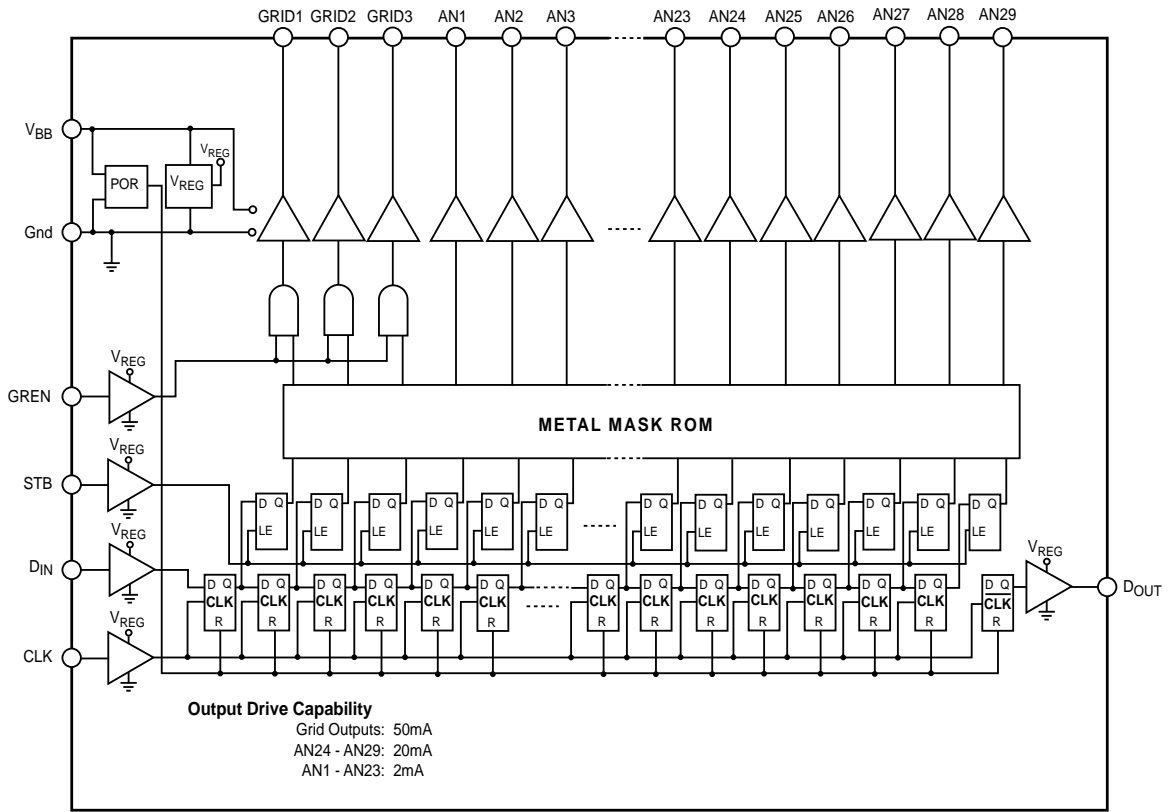
Application Information

Bit #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	G1	G2	G3	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13

Bit #	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A14	A15	A16	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29

Table 1: Bit Pattern, G = Grid, A = Anode.

Typical Operation

* Selected grid goes high only if input bit pattern from shift register to grid is high.

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PACKAGE DIMENSIONS IN mm (INCHES)

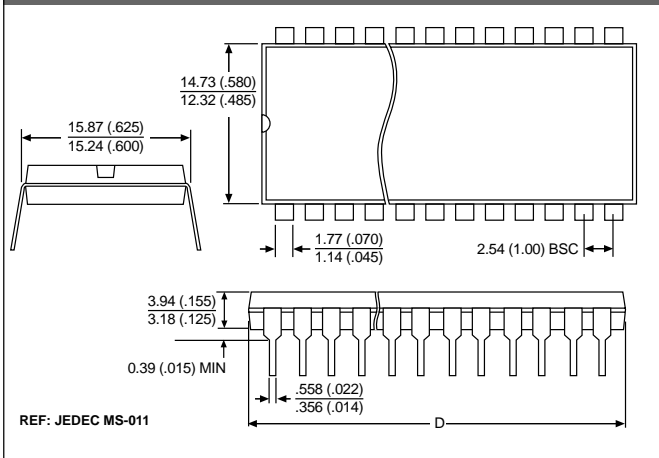| Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
40L PDIP	50.30	53.20	1.980	2.095

Lead Count	A	B	A	B
	Metric		English	
	Max	Min	Max	Min	Max	Min	Max	Min
44L PLCC	17.65	17.40	16.66	16.51	.695	.685	.656	.650

PACKAGE THERMAL DATA

Thermal Data		40L PDIP	44L PLCC	48L LQFP	
$R_{\Theta JC}$	typ	20	16	–	˚C/W
$R_{\Theta JA}$	typ	45	55	–	˚C/W

Plastic DIP (N); 600 mil wide

14.73 (.580) / 12.32 (.485)

15.87 (.625) / 15.24 (.600)

1.77 (.070) / 1.14 (.045)

2.54 (1.00) BSC

3.94 (.155) / 3.18 (.125)

0.39 (.015) MIN

.558 (.022) / .356 (.014)

D

REF: JEDEC MS-011

PLCC (FN)

4.06 (.160) / 3.69 (.145)

.51 (.020) Min

.53 (.021) / .33 (.013)

.81 (.032) / .66 (.026)

1.27 (.050) BSC

REF JEDEC MO-047

48 Lead LQFP (FL) 7 × 7mm Body

See Detail A

1.45 (.057) / 1.35 (.053)

1.60 (.063) max

9.00 (.354) BSC

7.00 (.276) BSC

0.15 (.006) / 0.05 (.002)

0.27 (.011) / 0.17 (.007)

7.00 BSC (.276)

9.00 BSC (.354)

DETAIL A

0.20 (.008) / 0.09 (.004)

0.75 (.030) / 0.45 (.018)

1.00 (.039) Ref

0.50 (.020) BSC

REF JEDEC MS-026
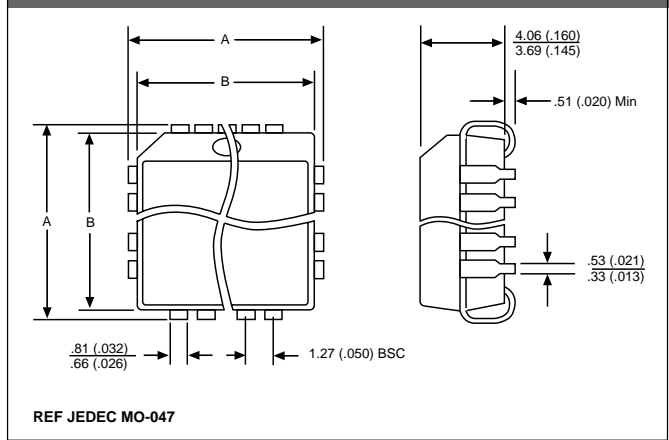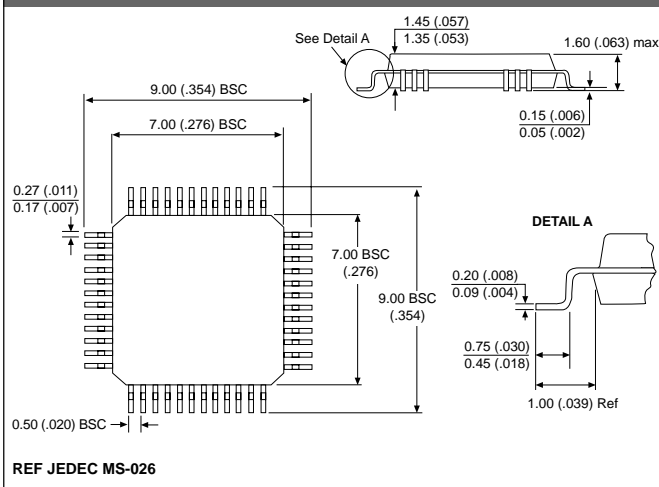
Ordering Information

Part Number	Description
CS1084XN40	40 Lead PDIP
CS1084XFN44	44 Lead PLCC
CS1084XFNR44	44 Lead PLCC *(tape & reel)*
CS1084XFL48	48 Lead LQFP
CS1084XFLR48	48 Lead LQFP *(tape & reel)*

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