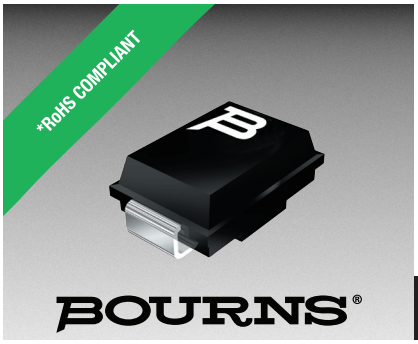


ASYMMETRICAL-BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTOR

TISP4A250H3BJ Overvoltage Protector

RING Line Protection for:
-LCAS (Line Card Access Switch)
such as Le75181, Le75183 and Le75282

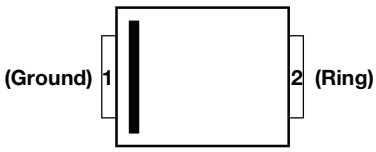
Voltages Optimized for:
-Battery-Backed Ringing Circuits
Maximum Ringing a.c..... 104 Vrms
Maximum Battery Voltage ..... -52 V

Device Name	V_{DRM} V	$V_{(BO)}$ V
TISP4A250H3BJ	+100	+125
	-200	-250

Rated for International Surge Wave Shapes

Wave Shape	Standard	I_{PPSM} A
2/10 µs	GR-1089-CORE	500
8/20 µs	IEC 61000-4-5	300
10/160 µs	TIA-968-A	250
10/700 µs	ITU-T K.20/21/45	200
10/560 µs	TIA-968-A	160
10/1000 µs	GR-1089-CORE	100

SMB Package (Top View)



Terminal typical application names shown in parenthesis

MD-SMB-006-a

Device Symbol



SD-TISP4A-001-a

Additional Information

Click these links for more information:

PRODUCT SELECTOR | TECHNICAL LIBRARY | INVENTORY | SAMPLES | CONTACT

Agency Recognition

Description	
UL	File Number: E215609

.....UL Recognized Component

Description

The TISP4A250H3BJ is an asymmetrical bidirectional overvoltage protector. It is designed to limit the peak voltages on the Ring line terminal of the LCAS (Line Card Access Switch) such as Le75181, Le75183 and Le75282. The TISP4A250H3BJ must be connected with bar-indexed terminal 1 to the protective Ground, and terminal 2 to the Ring conductor.

The TISP4A250H3BJ voltages are chosen to give adequate LCAS ring line terminal protection for all switch conditions. The most potentially stressful condition is low level power cross when the LCAS switches are closed. Under this condition, the TISP4A250H3BJ limits the voltage and corresponding LCAS dissipation until the LCAS thermal trip operates and opens the switches.

Under open-circuit ringing conditions, the line Ring conductor will have high peak voltages. For battery backed ringing, the Ring conductor will have a larger peak negative voltage than positive, i.e. the peak voltages are asymmetric. The TISP4A250H3BJ has a similar voltage asymmetry and will allow the maximum possible ringing voltage, while giving the most effective protection. On a connected line, the Tip conductor will have much smaller voltage levels than the open-circuit Ring conductor values. Here a TISP4xxxH3BJ series symmetrical voltage protector gives adequate protection.

Overvoltages are initially clipped by breakdown clamping. If sufficient current is available from the overvoltage, the breakdown voltage will rise to the breakover level, which causes the device to switch into a low-voltage on-state condition. This switching action removes the high voltage stress from the following circuitry and causes the current resulting from the overvoltage to be safely diverted through the protector. The high holding (switch off) current helps prevent d.c. latchup as the diverted current subsides.

WARNING Cancer and Reproductive Harm
www.P65Warnings.ca.gov

NOVEMBER 2006 – REVISED APRIL 2023

*RoHS Directive 2015/863, Mar 31, 2015 and Annex.
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How to Order

Device	Package	Carrier	Order As	Marking Code	Standard Quantity
TISP4A250H3BJ	SMB	Embossed Tape Reeled	TISP4A250H3BJR-S	4A250H	3000

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage (see Note 1)	V_{DRM}	+100 -200	V
Non-repetitive peak impulse current (see Notes 2 and 3) 2/10 µs (GR-1089-CORE, 2/10 µs voltage wave shape) 8/20 µs (IEC 61000-4-5, 1.2/50 µs voltage, 8/20 µs current combination wave generator) 10/160 µs (TIA-968-A, 10/160 µs voltage wave shape) 5/310 µs (ITU-T K.44, 10/700 µs voltage wave shape used in K.20/21/45) 5/320 µs (TIA-968-A, 9/720 µs voltage wave shape) 10/560 µs (TIA-968-A, 10/560 µs voltage wave shape) 10/1000 µs (GR-1089-CORE, 10/1000 µs voltage wave shape)	I_{PPSM}	 ±500 ±300 ±250 ±200 ±200 ±160 ±100	A
Non-repetitive peak on-state current (see Notes 2, 3 and 4) 20 ms, 50 Hz (full sine wave) 16.7 ms, 60 Hz (full sine wave) 1000 s, 50 Hz or 60 Hz a.c.	I_{TSM}	 55 60 2.2	A
Initial rate of rise of on-state currrent, exponential current ramp. Maximum ramp value < 200 A	di_T/dt	400	A/µs
Junction temperature	T_J	-40 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. See Figure 6 for voltages at other temperatures.
2. Initially the device must be in thermal equilibrium with T_J = 25 °C.
3. The surge may be repeated after the device returns to its initial conditions.
4. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. See Figure 5 for the current ratings at other durations. Derate current values at -0.61 %/°C for ambient temperatures above 25 °C.

Overload Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Maximum overload on-state current without open circuit, 50 Hz or 60 Hz a.c. (see note 5) 0.03 s 0.07 s 1.6 s 5.0 s 1000 s	$I_{T(OV)M}$	 60 40 8 7 2.2	A rms

NOTE: 5. Peak overload on-state current during a.c. power cross tests of GR-1089-CORE and UL 1950/60950. These electrical stress levels may damage the TISP4A250H3BJ silicon die. After test, the pass criterion is either that the device is functional or, if it is faulty, that it has a short-circuit fault mode. In the short-circuit fault mode, the following equipment is protected as the device is a permanent short across the line. The equipment would be unprotected if an open-circuit fault mode developed.

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Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = V_{DRM}$	T_A = 25 °C T_A = 85 °C			±5 ±10	µA
$V_{(BO)}$	Breakover voltage	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω				+125 -250	V
$I_{(BO)}$	Breakover current	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω		±150		±600	mA
V_T	On-state voltage	I_T = ±5 A, t_w = 100 µs				±3	V
I_H	Holding current	I_T = ±5 A, di/dt = ±30 mA/ms		±150		±600	mA
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp Maximum ramp value < 0.85V_{DRM}		±5			kV/µs
C_O	Off-state capacitance	f = 1 MHz, V_d = 1 V rms	V_D = 2 V			72	pF

Thermal Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$ (see Note 6)			113	°C/W
		265 mm x 210 mm populated line card, 4-layer PCB, $I_T = I_{TSM(1000)}$		50		

NOTE: 6. EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

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Parameter Measurement Information

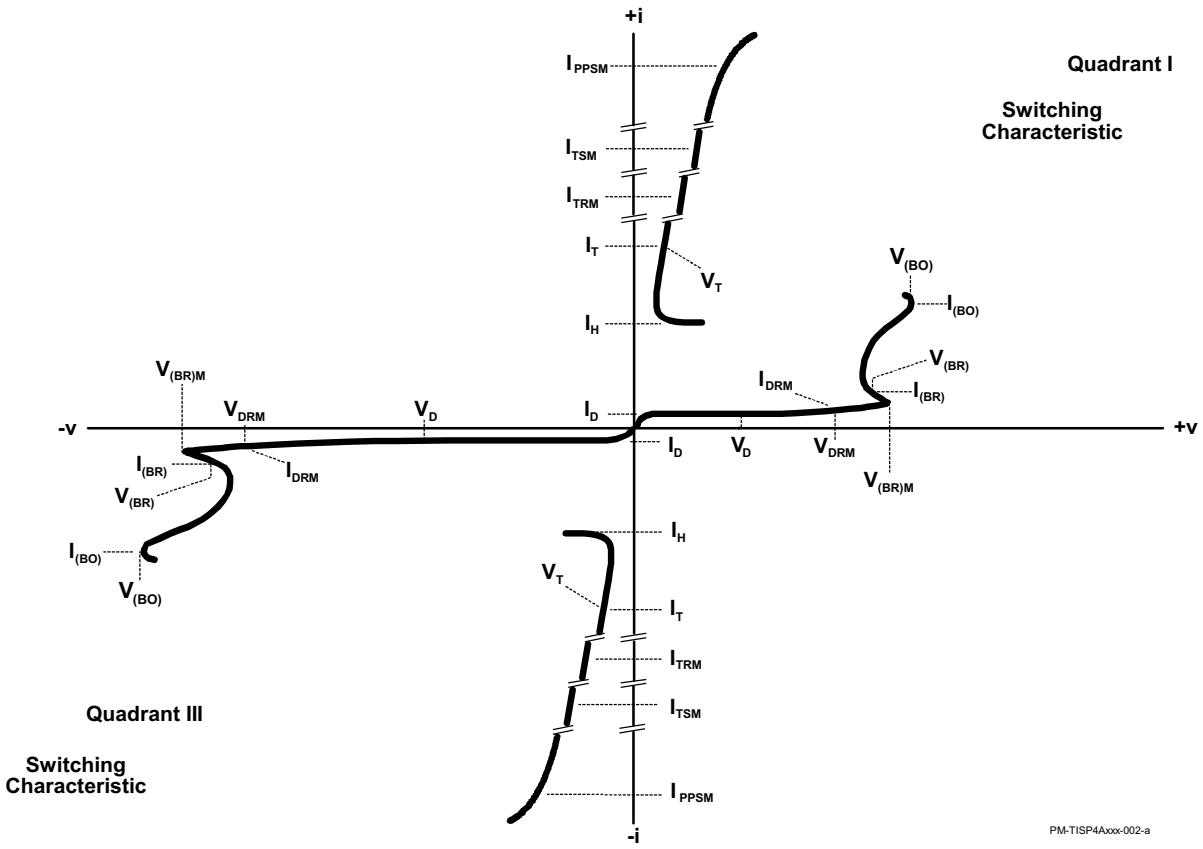


Figure 1. Voltage-Current Characteristic for the Ring and Ground Terminals
All Measurements are Referenced to the Ground Terminal

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Typical Characteristics

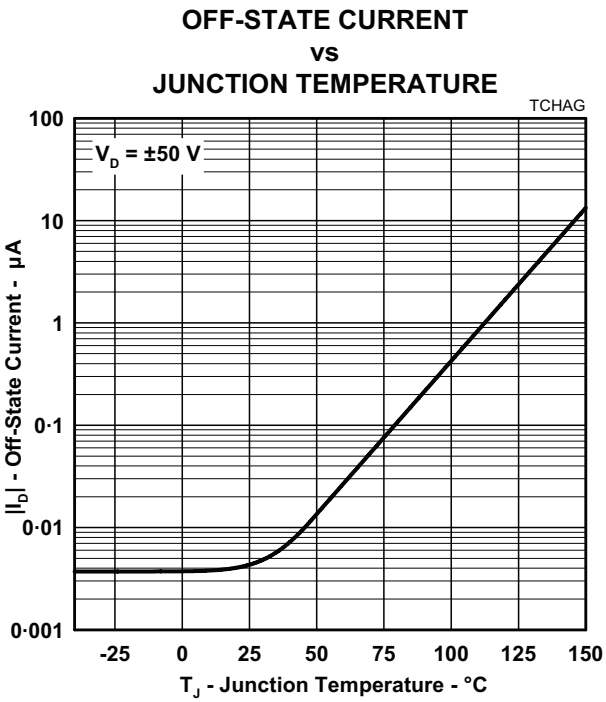


Figure 2.

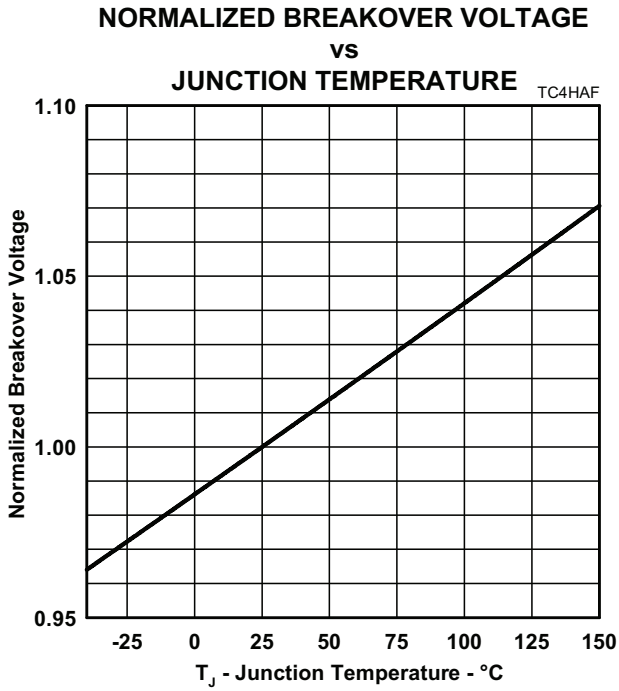


Figure 3.

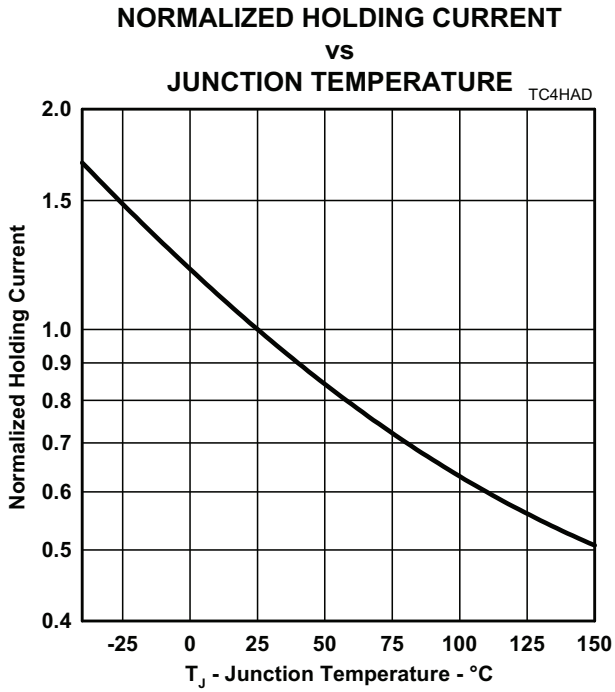


Figure 4.

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Rating and Thermal Information

NON-REPETITIVE PEAK ON-STATE CURRENT vs CURRENT DURATION

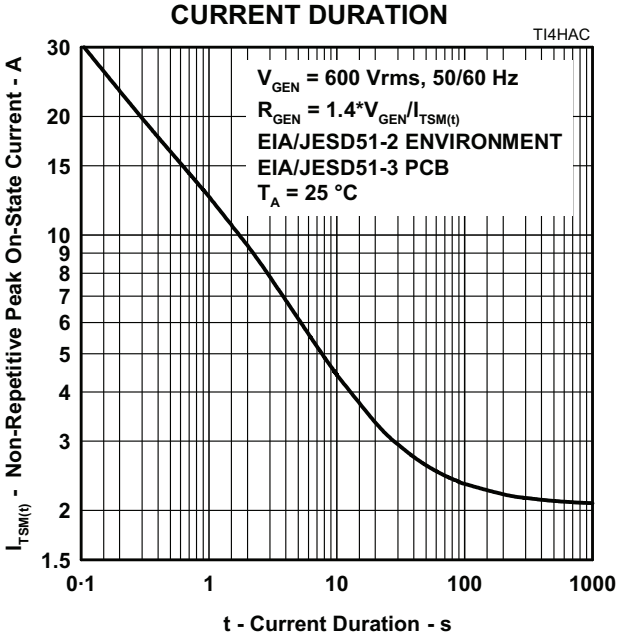


Figure 5.

V_{DRM} DERATING FACTOR vs MINIMUM AMBIENT TEMPERATURE

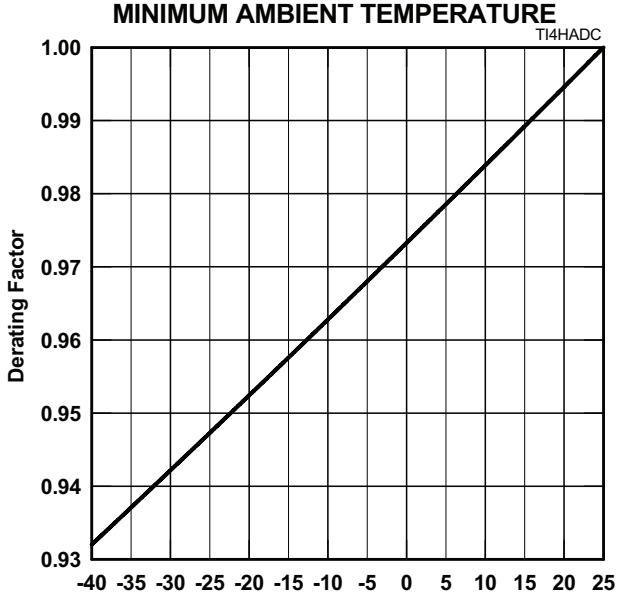


Figure 6.

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Applications Information

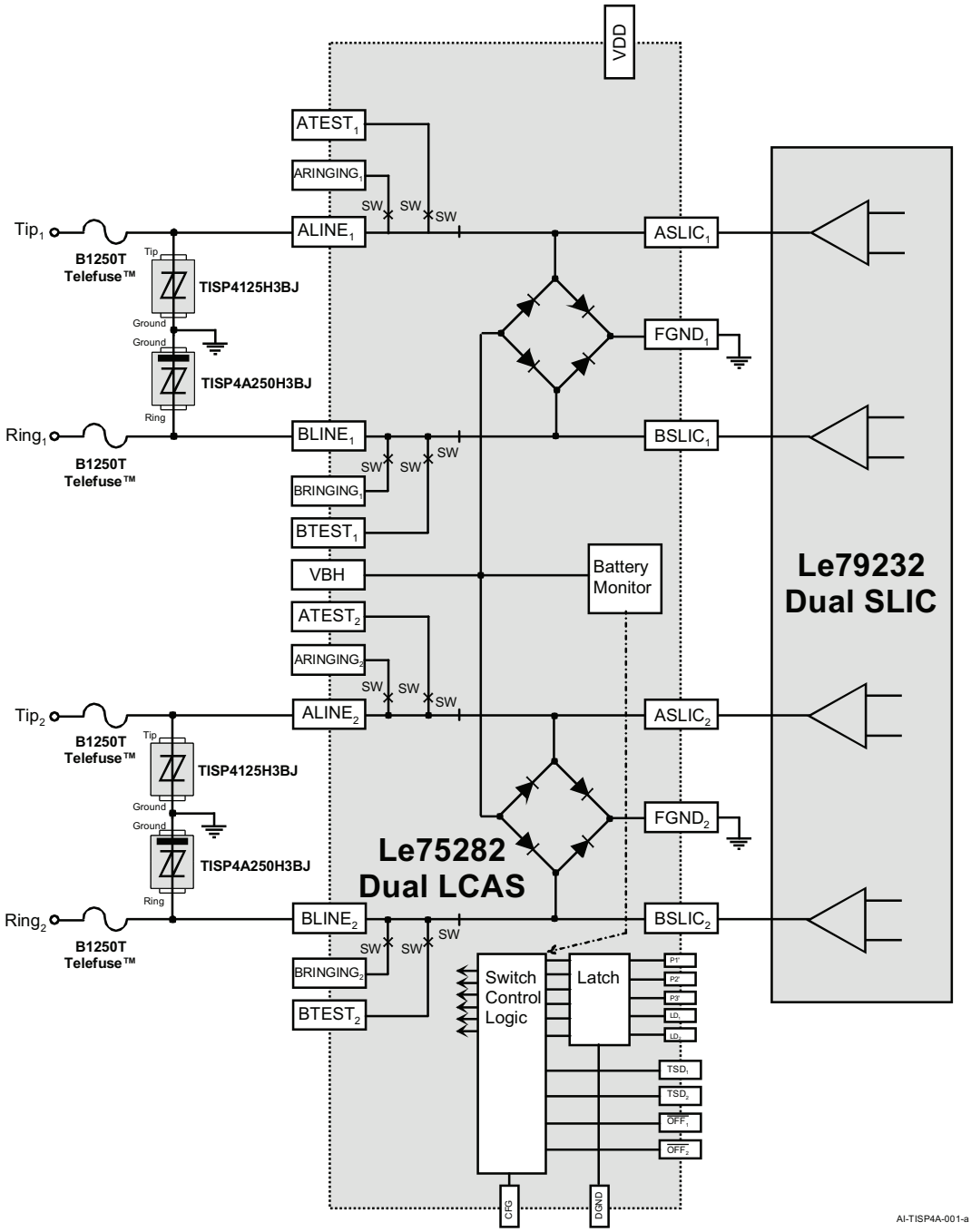


Figure 7. Typical Application Circuit

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