Data Sheet

ACPL-C87BU, ACPL-C87AU

Precision Optically Isolated Voltage Sensor with Wide Operating Temperature

Description

The Broadcom® ACPL-C87BU/C87AU voltage sensors are optical isolation amplifiers that are designed specifically for voltage sensing. Their 2V input range and high 1-GΩ input impedance make them well suited for isolated voltage-sensing requirements in electronic power converters applications, including motor drives and renewable energy systems. In a typical voltage-sensing implementation, a resistive voltage divider is used to scale the DC-link voltage to suit the input range of the voltage sensor. A differential output voltage that is proportional to the input voltage is created on the other side of the optical isolation barrier.

For general applications, the ACPL-C87AU (±1% gain tolerance) is recommended. For high-precision requirements, the ACPL-C87BU (±0.5% gain tolerance) can be used. The ACPL-C87BU/C87AU family operates from a single 5V supply and provides excellent linearity. An active-high shutdown pin is available, which reduces the IDD1 current to only 15A, making them suitable for battery-powered and other power-sensitive applications.

The high common-mode transient immunity (15 kV/ms) of the ACPL-C87BU/C87AU provides the precision and stability needed to accurately monitor DC-link voltage in high-noise environments. Combined with superior optical coupling technology, the ACPL-C87BU/C87AU implements sigma-delta (Σ-Δ) modulation, chopper stabilized amplifiers, and differential outputs to provide unequaled isolation-mode noise rejection, low offset, high-gain accuracy, and stability. This performance is delivered in a compact, auto-insertable stretched SO-8 (SSO-8) package that meets worldwide regulatory safety standards.

Features

- Advanced sigma-delta (Σ-Δ) modulation technology
- Unity gain 1 V/V, ±0.5% high gain accuracy (ACPL-C87BU)
- 1-GΩ input impedance
- 0V to 2V nominal input range
- –35-ppm/°C low gain drift
- 21-µV/°C offset voltage drift
- 0.1% nonlinearity maximum
- Active-high shutdown pin
- 100-kHz wide bandwidth
- 3V to 5.5V wide supply range for output side
- –40°C to +125°C operating temperature range
- 15-kV/µs common-mode transient immunity
- Compact, auto-insertable stretched SO-8 package
- Safety and regulatory approvals:
  - IEC/EN/DIN EN 60747-5-5: 1414-V_{peak} working insulation voltage
  - UL 1577: 5000-V_{rms}/1-minute double protection rating
  - CSA: Component Acceptance Notice #5

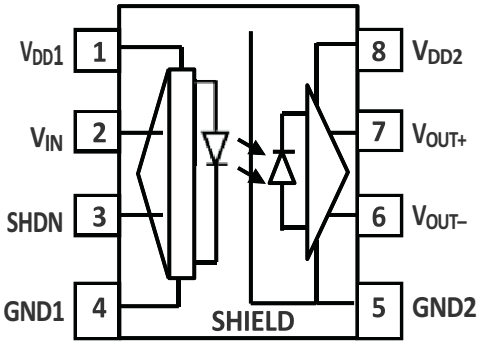
Applications

- Isolated voltage sensing in AC and servo motor drives
- Isolated DC-bus voltage sensing in solar inverters and wind turbine inverters
- Isolated sensor interfaces
- Signal isolation in data acquisition systems
- General-purpose voltage isolation

CAUTION! Take normal static precautions in handling and assembling this component to prevent damage and/or degradation that might be induced by electrostatic discharge (ESD). The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Functional Diagram

Figure 1: Functional Diagram



NOTE: A 0.1-µF bypass capacitor must be connected between pins 1 and 4 and between pins 5 and 8.

Table 1: Pin Description

Pin No.	Symbol	Description
1	V_{DD1}	Supply voltage for input side (4.5V to 5.5V), relative to GND1
2	V_{IN}	Voltage input
3	SHDN	Shutdown pin (active high)
4	GND1	Input side ground
5	GND2	Output side ground
6	$V_{OUT–}$	Negative output
7	V_{OUT+}	Positive output
8	V_{DD2}	Supply voltage for output side (3V to 5.5V), referenced to GND2

Ordering Information

The ACPL-C87BU/C87AU is UL recognized with a 5000-V_{rms}/1-minute rating per UL 1577.

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-C87AU	-000E	Stretched SO-8	X		X	80 per tube
ACPL-C87BU	-500E		X	X	X	1000 per reel

To form an order entry, choose a part number from the Part Number column and combine it with the desired option from the Option column.

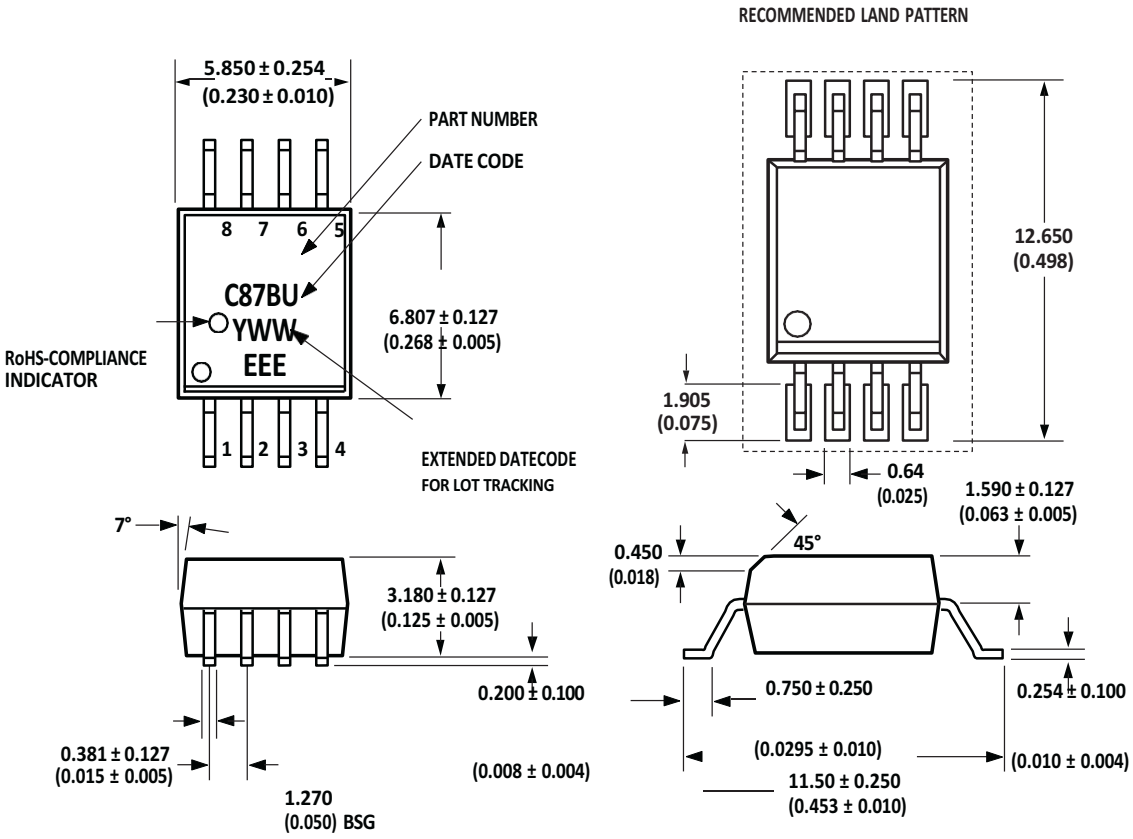
Example:

Use ACPL-C87AU-500E to order the product in a surface-mount package with tape and reel packaging, IEC/EN/DIN EN 60747-5-5 safety approval, and RoHS compliance.

Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawing

Figure 2: Stretched SSO-8 Package (SSO-8)



Dimensions in millimeters and (inches).

Note:
Lead coplanarity = 0.1 mm (0.004 inches).
Floating lead protrusion = 0.25 mm (10 mils) max.

Recommended Pb-Free IR Profile

Recommended reflow condition is as per JEDEC Standard, J-STD-020 (latest revision). Nonhalide flux should be used.

Regulatory Information

The ACPL-C87BU/C87AU is approved by the following organizations.

IEC/EN/DIN EN 60747-5-5	Approval with maximum working insulation voltage V_{IORM} = 1414 V_{peak}.
UL	Approval under UL 1577, component recognition program up to V_{ISO} = 5000 V_{rms}/1 minute. File 55361.
CSA	Approval under CSA Component Acceptance Notice #5.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Unit	Conditions
Minimum External Air Gap (External Clearance)	L(101)	8.0	mm	Measured from input terminals to output terminals, shortest distance through the air.
Minimum External Tracking (External Creepage)	L(102)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along the body.
Minimum Internal Plastic Gap (Internal Clearance)	—	0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and the photodetector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group	—	IIIa	—	Material Group (DIN VDE 0110, 1/89, Table 1).

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics[a]

Description	Symbol	Value	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
For Rated Mains Voltage ≤ 150 V_{rms}	—	I-IV	—
For Rated Mains Voltage ≤ 300 V_{rms}		I-IV	
For Rated Mains Voltage ≤ 450 V_{rms}		I-IV	
For Rated Mains Voltage ≤ 600 V_{rms}		I-IV	
For Rated Mains Voltage ≤ 1000 V_{rms}		I-III	
Climatic Classification	—	40/125/21	—
Pollution Degree (DIN VDE 0110/1.89)	—	2	—
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{peak}
Input to Output Test Voltage, Method b V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 second, Partial Discharge < 5 pC	V_{PR}	2652	V_{peak}
Input to Output Test Voltage, Method a V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 seconds, Partial Discharge < 5 pC	V_{PR}	2262	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60 seconds)	V_{IOTM}	8000	V_{peak}
Safety-Limiting Values (maximum values allowed in the event of a failure)			
Case Temperature	T_S	175	°C
Input Current	$I_{S,INPUT}$	230	mA
Output Power	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	≥ 10^9	Ω

a. Insulation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits within the application.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	–55	+150	°C
Ambient Operating Temperature	T_A	–40	+125	°C
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	6.0	V
Steady-State Input Voltage[a, b]	V_{IN}	–2	V_{DD1} + 0.5	V
Two-Second Transient Input Voltage[c]	V_{IN}	–6	V_{DD1} + 0.5	V
Logic Input	V_{SD}	–0.5	V_{DD1} + 0.5	V
Output Voltages	V_{OUT+}, $V_{OUT–}$	–0.5	V_{DD2} + 0.5	V
Lead Solder Temperature	260° C for 10 seconds, 1.6 mm below seating plane			

a. DC voltage of up to –2V on the inputs does not cause latch-up or damage to the device.

b. Absolute maximum DC current on the inputs = 100 mA; no latch-up or device damage occurs.

c. Transient voltage of 2 seconds up to –6V on the inputs does not cause latch-up or damage to the device.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Ambient Operating Temperature	T_A	–40	+125	°C
V_{DD1} Supply Voltage	V_{DD1}	4.5	5.5	V
V_{DD2} Supply Voltage	V_{DD2}	3.0	5.5	V
Input Voltage Range[a]	V_{IN}	0	2.0	V
Shutdown Enable Voltage	V_{SD}	V_{DD1} – 0.5	V_{DD1}	V

a. 2V is the nominal input range. Full scale input range (FSR) is 2.46V.

Electrical Specifications

Unless otherwise noted, T_A = –40°C to +125°C, V_{DD1} = 4.5V to 5.5V, V_{DD2} = 3.3V to 5.5V, V_{IN} = 0V to 2V, and V_{SD} = 0V.

Parameter	Symbol	Min.	Typ.[a]	Max.	Unit	Test Conditions	Figure	Note
DC Characteristics								
Input Offset Voltage	V_{OS}	–10	–0.3	10	mV	T_A = 25°C	3	
Magnitude of Input Offset Change vs. Temperature	$\lvert dV_{OS}/dT_A \rvert$	—	21	—	µV/°C	T_A = –40°C to +125°C; Direct short across inputs	4	
Gain (ACPL-C87BU, ± 0.5%)	G0	0.995	1	1.005	V/V	T_A = 25°C; V_{DD2} = 5V	6	b
Gain (ACPL-C87AU, ± 1%)	G1	0.99	1	1.01	V/V	T_A = 25°C	6	b
Magnitude of Gain Change vs. Temperature	dG/dT_A	—	25	—	ppm/°C	T_A = –40°C to +125°C	5	
Nonlinearity	NL	—	0.05	0.12	%	V_{IN} = 0V to 2V, T_A = 25°C	7	
Inputs and Outputs								
Recommended Input Range	VINR	—	2	—	V	Referenced to GND1		
Full-Scale Differential Voltage Input Range	FSR	—	2.46	—	V	Referenced to GND1		
Shutdown Logic Low Input Voltage	V_{IL}	—	0.8	—	V	T_A = 25°C		
Shutdown Logic High Input Voltage	V_{IH}	V_{DD} – 0.5	5	—	V	T_A = 25°C		
Input Bias Current	I_{IN}	–0.1	–0.001	0.1	µA	V_{IN} = 0V		
Magnitude of I_{IN} Change vs. Temperature	dI_{IN}/dT_A	—	1	—	nA/°C	—		
Equivalent Input Impedance	R_{IN}	—	1000	—	MΩ	—		
Output Common-Mode Voltage	V_{OCM}	—	1.23	—	V	V_{OUT+} or $V_{OUT–}$		
Output Voltage Range	V_{OUTR}	—	V_{OCM} ± 1.23	—	V	V_{SD} = 0V	10	c
Output Short-Circuit Current	$\lvert I_{OSC} \rvert$	—	30	—	mA	V_{OUT+} or $V_{OUT–}$, Shorted to GND2 or V_{DD2}		
Output Resistance	R_{OUT}	—	36	—	Ω	V_{OUT+} or $V_{OUT–}$		
AC Characteristics								
V_{OUT} Noise	N_{OUT}	—	1.3	—	mV_{rms}	V_{IN} = 2V; BW = 1 kHz	9	d
Small-Signal Bandwidth (–3 dB)	$f_{-3\ dB}$	70	100	—	kHz	Guaranteed by design		
Input-to-Output Propagation Delay								
50% to 10%	t_{PD10}	—	2.2	3.0	µs	Step input	15	
50% to 50%	t_{PD50}	—	3.7	6.0	µs	Step input	15	
90% to 90%	t_{PD90}	—	5.3	7.0	µs	Step input	15	
Output Rise/Fall Time (10% to 90%)	$t_{R/F}$	—	2.7	4.0	µs	Step input (t_{PD90} – t_{PD10})		
Shutdown Delay	t_{SD}	—	25	40	µs	V_{IN} = 2V	11	
Enable Delay	t_{ON}	—	150	200	µs	V_{IN} = 2V	11	
Common Mode Transient Immunity	CMTI	10	15	—	kV/µs	V_{CM} = 1 kV, T_A = 25°C		
Power Supply Rejection	PSR	—	–78	—	dB	1-Vpp 1-kHz sine wave ripple on V_{DD1}, differential output		

Parameter	Symbol	Min.	Typ.[a]	Max.	Unit	Test Conditions	Figure	Note
Power Supplies								
Input Side Supply Current	IDD1	—	10.5	15	mA	V_{SD} = 0V		
		—	20	—	µA	V_{SD} = 5V		
	IDD2	—	6.5	12	mA	5V supply		
		—	6.1	11	mA	3.3V supply		

a. All typical values are under typical operating conditions at T_A = 25°C, V_{DD1} = 5V, V_{DD2} = 5V.

b. Gain is defined as the slope of the best-fit line of differential output voltage ($V_{OUT+} – V_{OUT-}$) versus input voltage over the nominal range, with the offset error adjusted.

c. When V_{SD} = 5V or when shutdown is enabled, V_{OUT+} is close to 0V and V_{OUT-} is at close to 2.46V. This is similar to when V_{DD1} is not supplied.

d. Noise is measured at the output of the differential to single-ended post amplifier.

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000	—	—	V_{rms}	RH < 50%, t = 1 minute, T_A = 25°C	a, b
Resistance (Input-Output)	R_{I-O}	—	10^{14}	—	Ω	V_{I-O} = 500 V_{DC}	c
Capacitance (Input-Output)	C_{I-O}	—	0.5	—	pF	f = 1 MHz	c

a. In accordance with UL 1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 V_{rms} for 1 second (leakage detection current limit, I_{I-O} 5A). This test is performed before the 100% production test for partial discharge (method b) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristic table.

b. The input-output momentary withstand voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics table and your equipment level safety specification.

c. This is a two-terminal measurement: pins 1 to 4 are shorted together, and pins 5 to 8 are shorted together.

Typical Performance Plots

All ±3 (sigma symbol) plots are based on characterization test results at the point of product release. For guaranteed specifications, refer to the Electrical Specifications section.

Figure 3: Input Offset vs. Supply Voltage

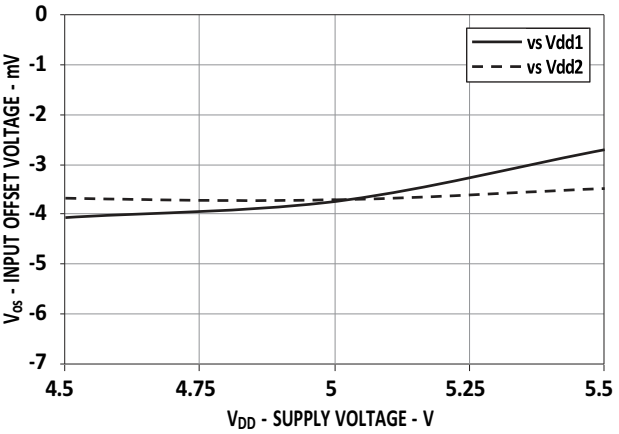


Figure 4: Input Offset vs. Temperature

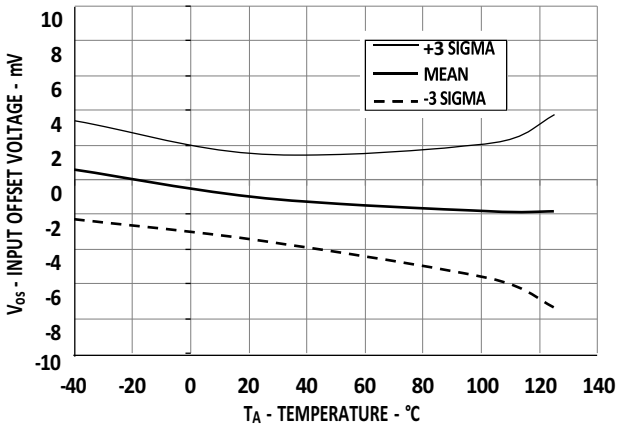


Figure 5: Gain vs. Temperature

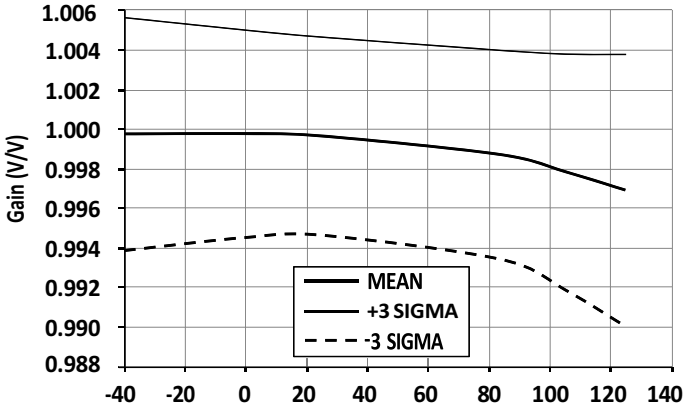


Figure 6: Gain vs. Supply Voltage

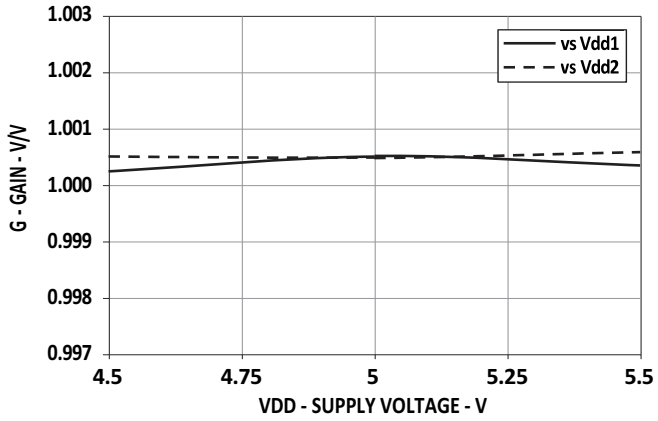


Figure 7: Nonlinearity vs. Supply Voltage

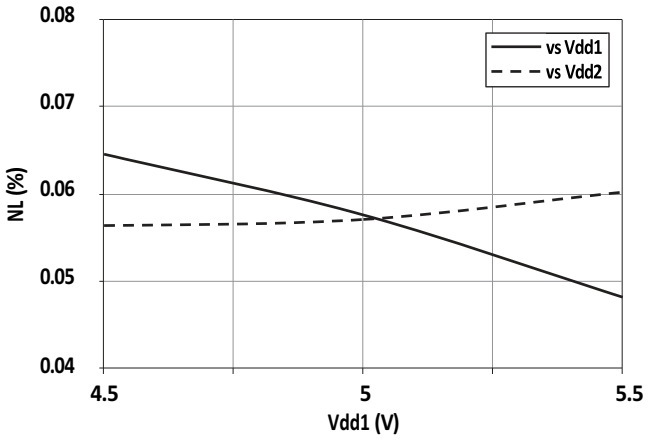


Figure 8: Nonlinearity vs. Temperature

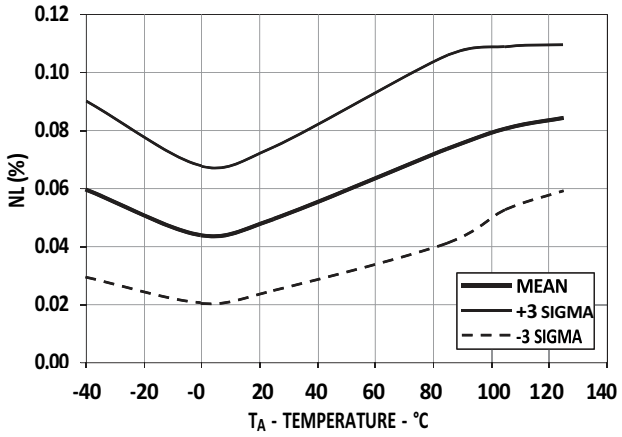


Figure 9: AC Noise vs. Filter Frequency vs. V_{IN}

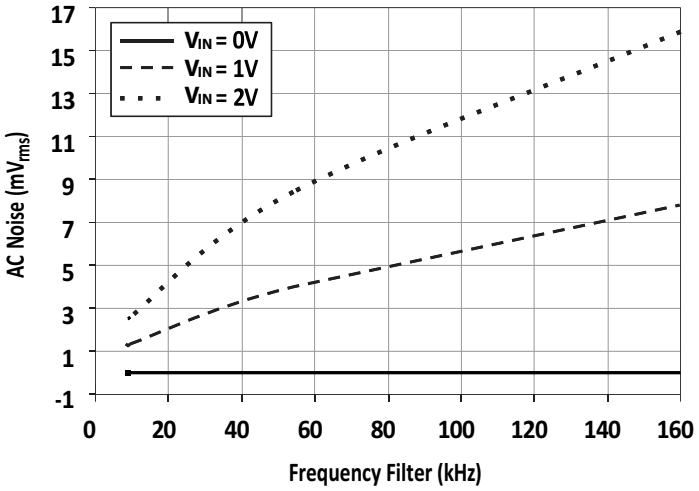


Figure 10: V_{IN} vs. V_{OUT+}, V_{OUT}

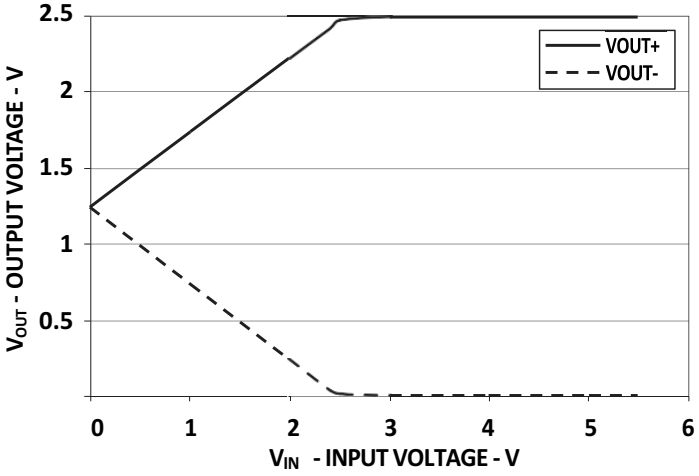


Figure 11: Frequency Response

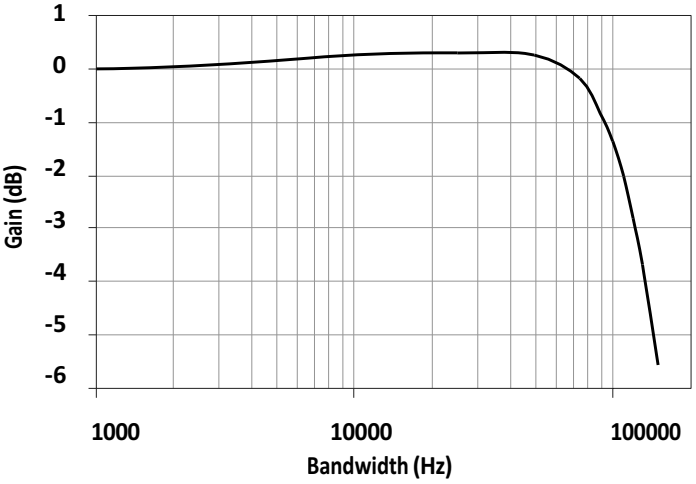


Figure 12: Phase Response

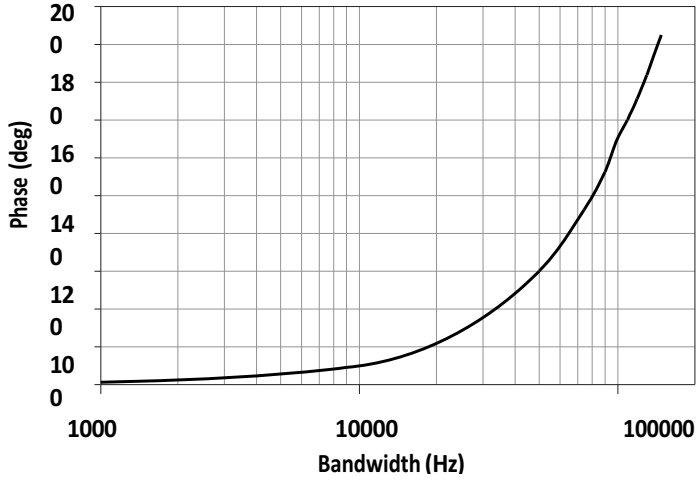


Figure 13: Propagation Delay vs. Temperature

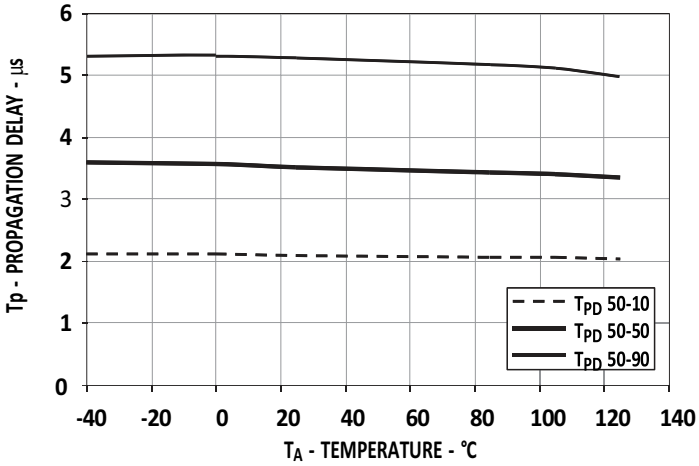


Figure 14: Shutdown and Wakeup Input to Output Timing Diagram: $V_{Out\ Diff} = V_{Out+} - V_{Out-}$

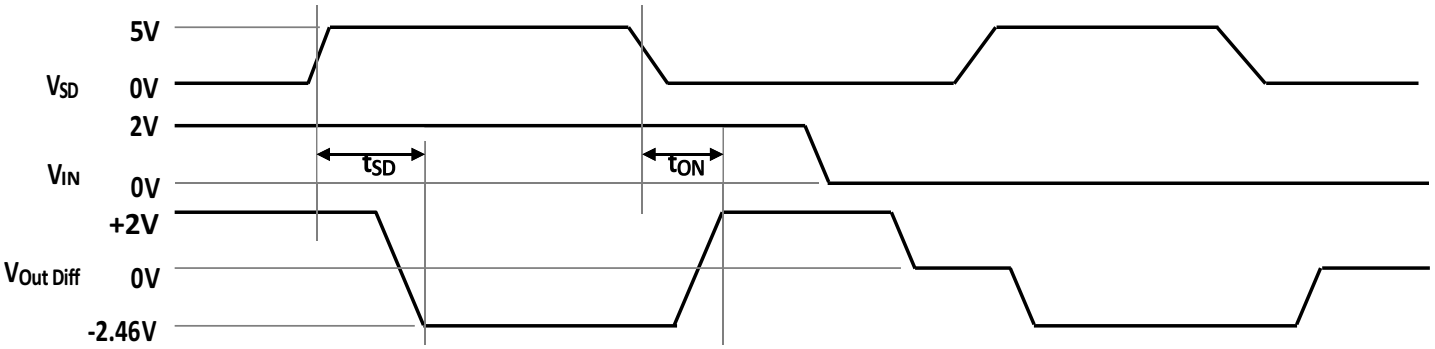
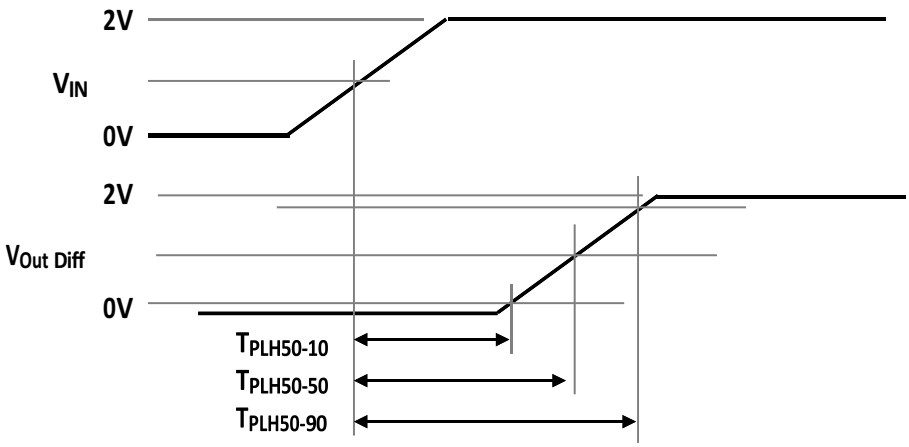


Figure 15: Input to Output Propagation Delay Timing Diagram: $V_{Out\ Diff} = V_{Out+} - V_{Out-}$



Definitions

Gain

Gain is defined as the slope of the best-fit line of differential output voltage ($V_{OUT+} - V_{OUT-}$) over the nominal input range, with the offset error adjusted out.

Nonlinearity

Nonlinearity is defined as half of the peak-to-peak output deviation from the best-fit gain line, expressed as a percentage of the full-scale differential output voltage.

Common Mode Transient Immunity

Common mode transient immunity (CMTI), also known as common mode rejection, is tested by applying an exponentially rising/falling voltage step on pin 4 (GND1) with respect to pin 5 (GND2). The rise time of the test waveform is set to approximately 50 ns. The amplitude of the step is adjusted until the differential output ($V_{OUT+} - V_{OUT-}$) exhibits more than a 200-mV deviation from the average output voltage for more than1 µs. The ACPL-C87xU will continue to function if more than 10-kV/µs common mode slopes are applied, as long as the breakdown voltage limitations are observed.

Power Supply Rejection

Power supply rejection (PSR) is the ratio of the differential amplitude of the ripple outputs over the power supply ripple voltage, referred to the input, expressed in dB.

Application Information

Application Circuit

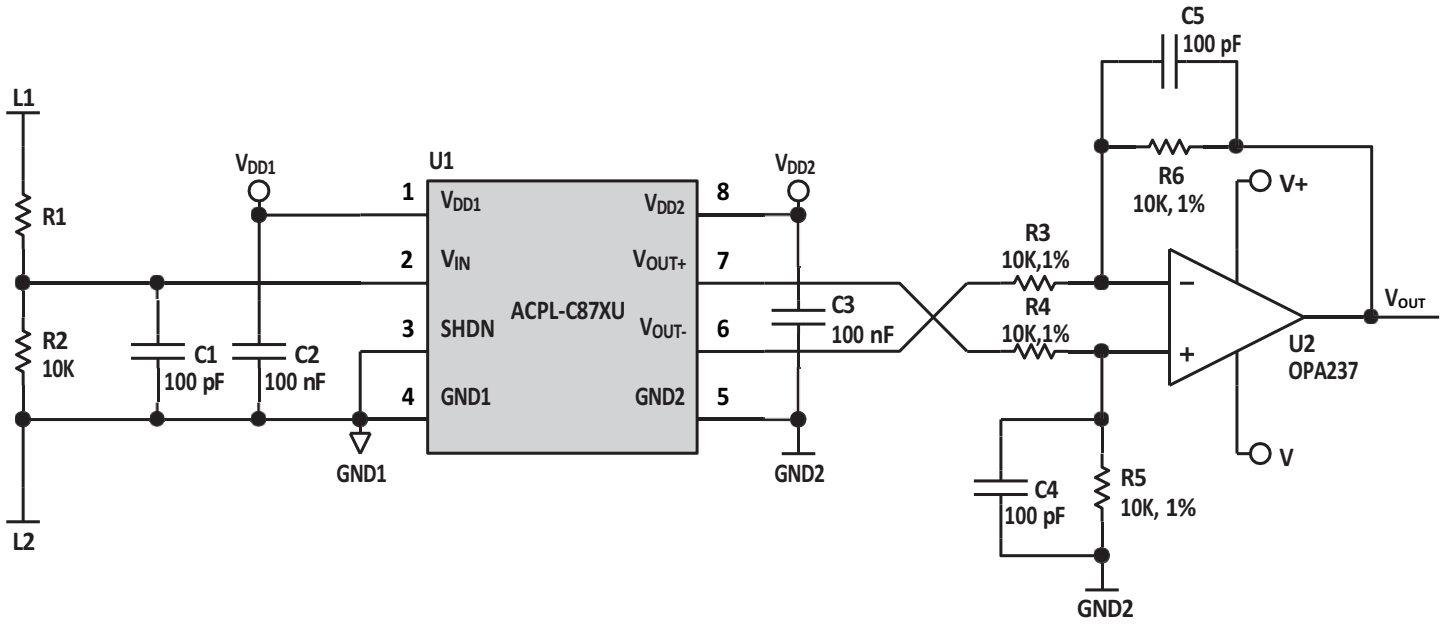
Figure 16 shows the typical application circuit. The ACPL-C87xU voltage sensor is often used in photovoltaic (PV) panel voltage measurement and tracking in PV inverters and in DC bus voltage monitoring in motor drivers. The high voltage across rails must be scaled down to fit the input range of the iso-amp by choosing R1 and R2 values according to the appropriate ratio.

The ACPL-C87xU senses the single-ended input signal and produces differential outputs across the galvanic isolation barrier. The differential outputs (V_{OUT+}, V_{OUT-}) can be connected to an op-amp to convert to a single-ended signal or directly to two ADCs. The op-amp used in the external post-amplifier circuit should be of sufficiently high precision so that it does not contribute a significant amount of offset or offset drift relative to the contribution from the isolation amplifier. Generally, op-amps with bipolar input stages exhibit better offset performance than op-amps with JFET or MOSFET input stages.

In addition, the op-amp should also have enough bandwidth and slew rate so that it does not adversely affect the response speed of the overall circuit. The post-amplifier circuit includes a pair of capacitors (C4 and C5) that form a single-pole low-pass filter; these capacitors allow the bandwidth of the post-amp to be adjusted independently of the gain and are useful for reducing the output noise from the isolation amplifier.

The gain-setting resistors in the post-amp should have a tolerance of 1% or better to ensure adequate common mode rejection ratio (CMRR) and adequate gain tolerance for the overall circuit. Resistor networks can be used that have much better ratio tolerances than can be achieved using discrete resistors. A resistor network also reduces the total number of components for the circuit as well as the required board space.

Figure 16: Typical Application Circuit

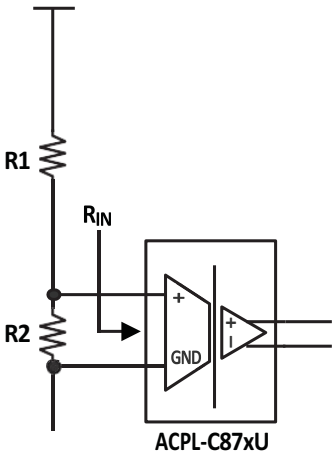


Measurement Accuracy and Power Dissipation of the Resistive Divider

The input stage of the typical application circuit in Figure 16 can be simplified as shown in Figure 17. R2 and R_{IN}, the input resistance of the ACPL-C87xU, create a current divider that results in an additional measurement error component that will be added to the device gain error. Assuming that R1 and R_{IN} have a much higher value than R2, the resulting error can be estimated to be $R2/R_{IN}$.

With an R_{IN} of 1 GΩ for the ACPL-C87xU, this additional measurement error is negligible with an R2 up to 1 MΩ, where the error is approximately 0.1%. Though small, it can be further reduced by reducing the R2 to 100 kΩ (error of approximately 0.01%) or to 10 kΩ (error of approximately 0.001%). However, with a lower R2, the drawback of higher power dissipation in the resistive divider string must be considered, especially in higher voltage-sensing applications. For example, with 600 V DC across L1 and L2 and an R2 of 100 kΩ for a 0.01% measurement error, the resistive divider string consumes about 12 mW, assuming that V_{IN} is set to 2V. If the R2 is reduced to 10 kΩ to reduce the error to 0.001%, the power consumption will increase to about 120 mW. In energy-efficiency critical applications, such as PV inverters and battery-powered applications, this trade-off between measurement accuracy and power dissipation in the resistive string provides flexibility in design priority.

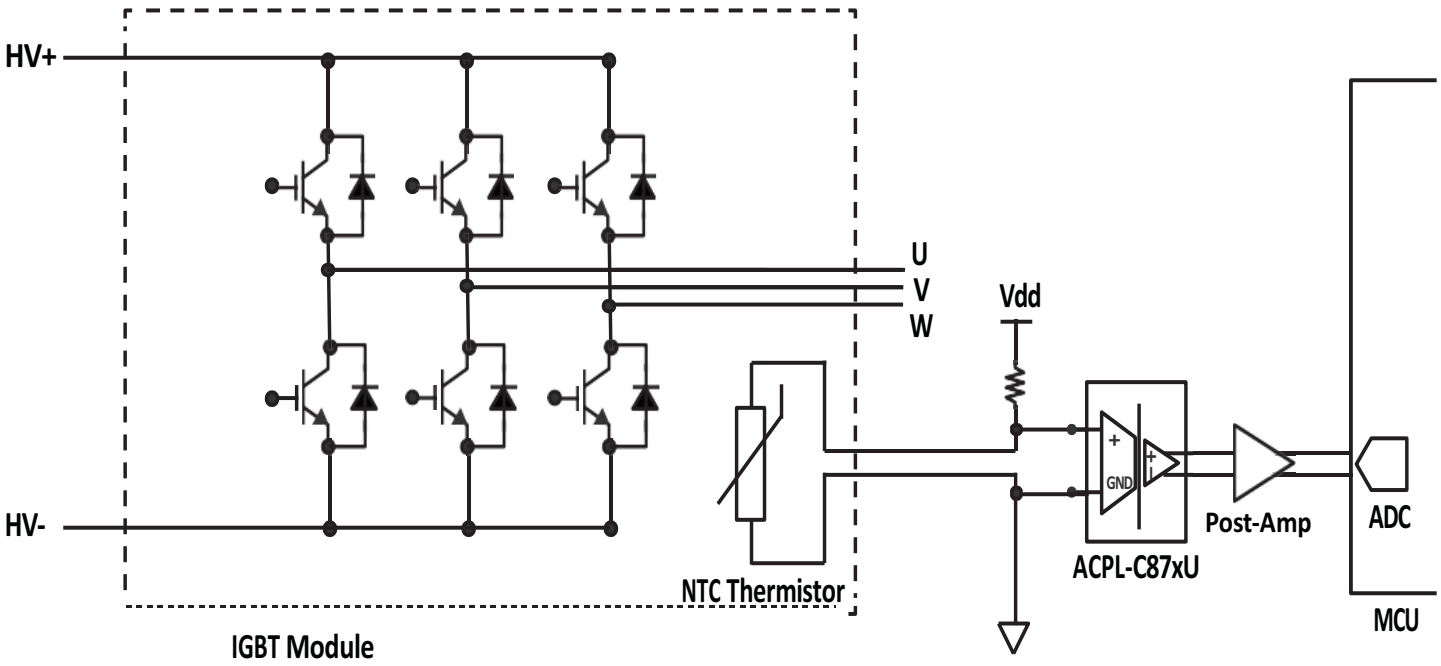
Figure 17: Simplified Input Stage



Isolated Temperature Sensing Using a Thermistor

Insulated-gate bipolar transistors (IGBTs) are an integral part of a motor or servo drive system. Because of the high power that IGBTs usually handle, it is essential that they have proper thermal management and are sufficiently cooled. Long-term overload conditions could raise the IGBT module temperature permanently, or failure of the thermal management system could subject the module to package overstress and lead to catastrophic failures. One common way to monitor the temperature of the module is by using an NTC type thermistor mounted onto the IGBT module. Some IGBT module manufacturers also have IGBTs with the thermistor integrated inside the module. In some cases, it is necessary to isolate this thermistor to provide added isolation and insulation due to the high-power nature of the IGBTs. The ACPL-C87xU voltage sensor can be used to easily meet such a requirement, while providing good accuracy and nonlinearity. Figure 18 shows an example of such an implementation. The ACPL-C87xU is used to isolate the thermistor voltage, which is later fed by the post-amp stage to an ADC onboard the microcontroller (MCU) to determine the module temperature. The thermistor must be biased such that its voltage output will optimize the 2V input range of the ACPL-C87xU across the intended temperature measurement range.

Figure 18: Thermistor Sensing in IGBT Module



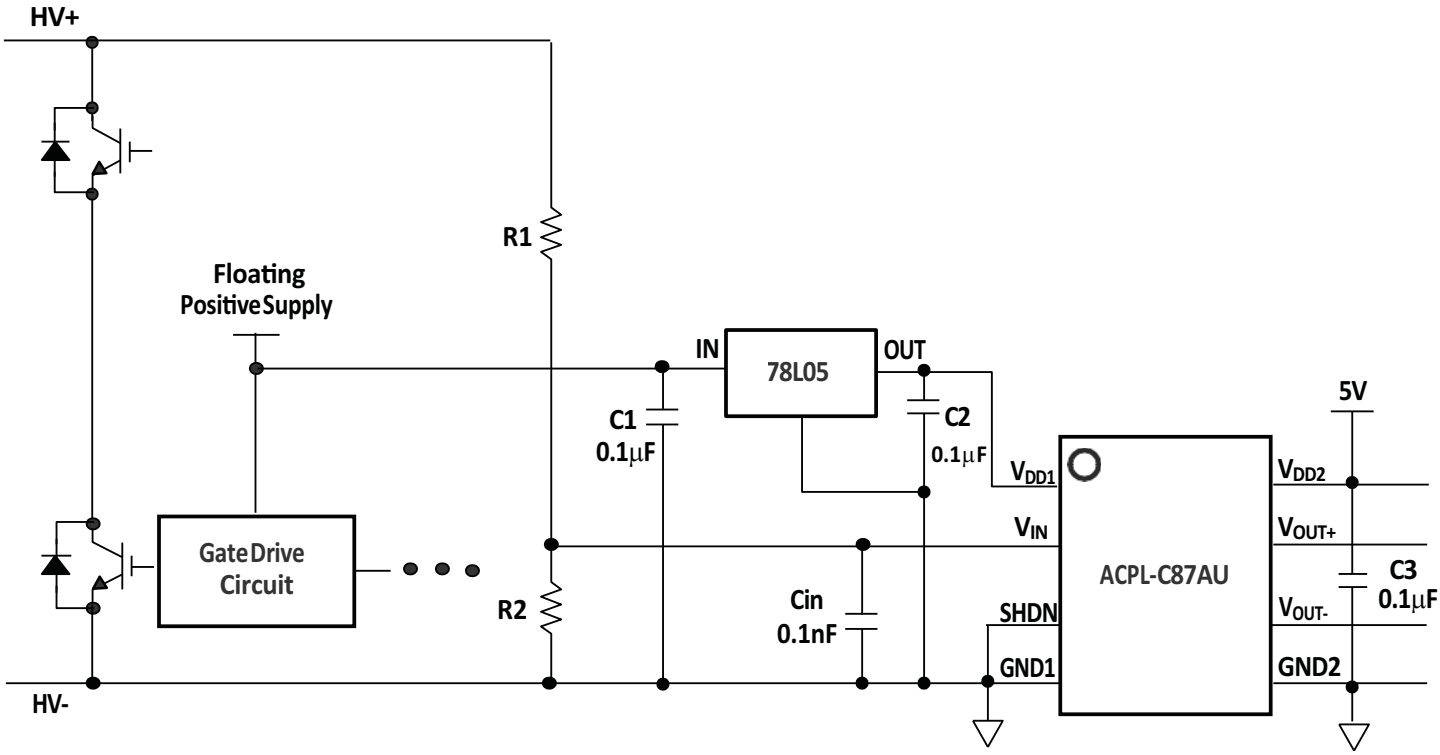
Power Supplies and Bypassing

A power supply of 5V is required to power the ACPL-C87xU input side VDD1. In many motor-drive DC-bus voltage-sensing applications, this 5V supply is most often obtained from the same supply used to power the power-transistor gate-drive circuit using an inexpensive 78L05 three-terminal regulator. To help attenuate high-frequency power-supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor.

In some other applications, a dedicated supply might be required to supply the VDD1. These applications include PV inverter voltage tracking and measurement and temperature sensor signal isolation. In these cases, it is possible to add an additional winding on an existing transformer. Otherwise, some sort of simple isolated supply can be used, such as a line powered transformer or a high-frequency DC-DC converter module.

As shown in Figure 19, 100-nF bypass capacitors (C2, C3) should be located as close as possible to the pins of the isolation amplifier. The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolation amplifier. A 100-pF bypass capacitor (Cin) is also recommended at the input pins due to the switched-capacitor nature of the input circuit. The input bypass capacitor Cin also forms part of the anti-aliasing filter, which is recommended to prevent high-frequency noise from aliasing down to lower frequencies and interfering with the input signal. When R1 is far greater than R2, the corner frequency of the low-pass anti-aliasing filter can be calculated by $1/(2\times\pi\times R2\times Cin)$. The input filter also performs an important reliability function—it reduces transient spikes from ESD events flowing through the high-voltage rails.

Figure 19: Recommended Power Supply and Bypassing



PC Board Layout

The design of the printed circuit board (PCB) should follow good layout practices, such as keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, and using ground and power planes. In addition, the layout of the PCB can also affect the isolation transient immunity (CMTI) of the ACPL-C87xU, primarily due to stray capacitive coupling between the input and the output circuits.

To obtain optimal CMTI performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the ACPL-C87AU. The input capacitor that forms part of the anti-aliasing filter, together with the resistor network, should be placed as close as possible to the V_{IN} pin.