Data Sheet

QFBR-5978AZ-2

Digital Diagnostic 650-nm Transceiver Supporting the SC-RJ Connector for PROFINET (100 Mb/s)

Description

The Broadcom® PROFINET transceiver provides the system designer with the ability to implement Fast Ethernet (100 Mb/s) over 50m POF (980 µm/1000 µm) and 100m HCS (200 µm/230 µm) fibers. The available transceiver connectivity supports the SC-RJ connector. This product is AEL Class 1, lead free, and compliant to RoHS 2011/65/EU and the complement (EU) 2015/863.

Transmitter

The transmitter consists of a 650-nm LED with an integrated driver IC. The LED driver operates at 3.3V. It receives differential LVPECL electrical inputs and converts them into a modulated current driving the LED.

The optimized lens system of the optical subassembly couples emitted optical power into POF and HCS fibers very efficiently.

Receiver

The receiver uses a fully integrated single chip solution that provides excellent immunity to EMI and fast transient dV/dt rejection. The receiver directly converts an optical signal to a digital LVPECL signal. The receiver operates at 3.3V.

The receiver has a signal detect (SD) feature, and the output voltage of SD is LVPECL.

Package

The transceiver package consists of four basic elements: two optical subassemblies, an electrical subassembly, and the housing as illustrated in the block diagram in Figure 1. The package outline drawing and pinout diagram are shown in Figure 2 and Figure 3.

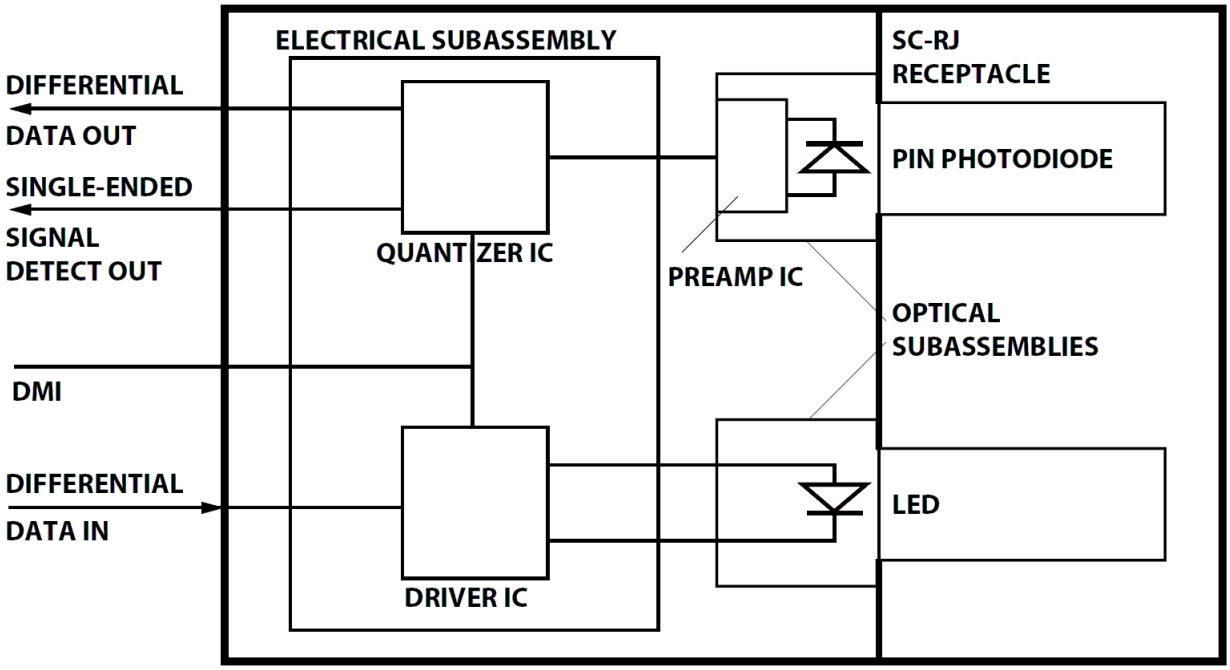
Features

- Compatible with the electrical and optical performance of POFAC recommendations for Fast Ethernet over polymer optical fiber (POF)
- Compatible with the electrical and optical performance of PROFINET recommendations for Fast Ethernet over POF and HCS fibers
- Manufactured in an ISO 9001 certified facility
- Compatible with QFBR-5978AZ
- Link distance up to 50m POF or 100m HCS
- Link distance up to 250m with gradient index HCS fiber
- Low power dissipation
- Operating case temperature: –40°C to +90°C
- Excellent EMI and EMC behavior
- Digital Diagnostics Monitoring Interface (DMI) is based on SFF-8472 Rev 9.3 and provides real-time monitoring of the following:
  - Received optical power
  - Temperature
  - Receiver supply voltage
  - Receiver OMA margin
- LVPECL input and output interfaces
- LVPECL signal detect output

Applications

- PROFINET application
- Factory automation at Fast Ethernet data rate
- Fast Ethernet networking over POF and HCS fibers

Figure 1: Block Diagram



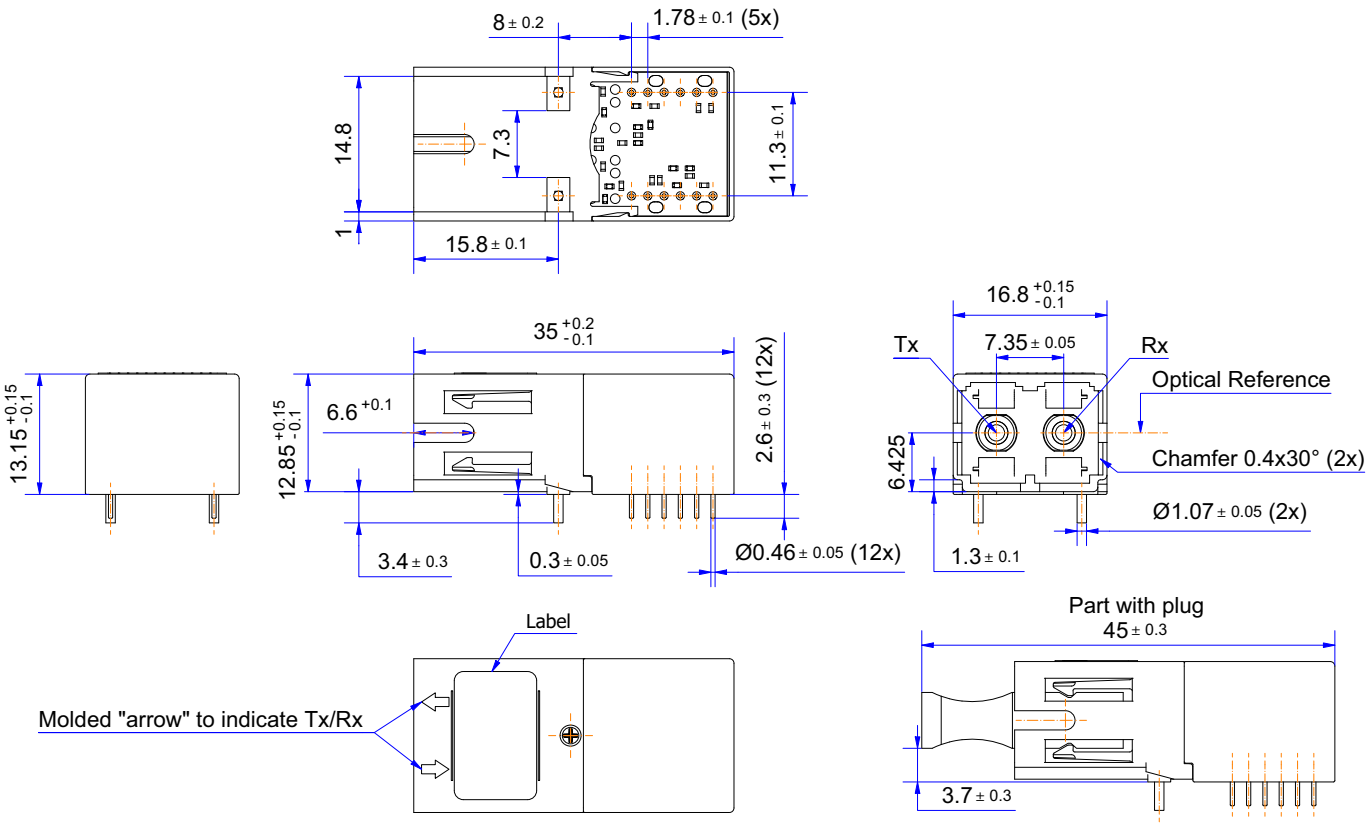
The optical subassembly for the receiver contains a PIN photodiode with a preamplifier IC. The optical subassembly for the transmitter includes the LED. Furthermore, both subassemblies contain lens elements to provide an efficient light coupling.

The electrical subassembly consists of a multilayer printed circuit board on which the ICs and various surface-mounted passive circuit elements are attached.

The subassemblies are shielded with a metal cover to provide immunity to ESD and EMI. The connector ferrule and the solder posts have a mechanical contact, and both are isolated from the internal circuit of the transceiver. To use a metal ferrule, the solder posts should be connected to chassis ground. Altogether, these three design features provide excellent immunity to ESD and EMI.

The transceiver is attached to the PCB with 12 signal pins and two solder posts, which exit the bottom of the housing. The two solder posts provide mechanical strength to withstand mechanical stress.

Figure 2: Package Outline Drawing



NOTE:

1. All dimensions are in mm.
2. The weight of the transceiver is approximately 13.3g (without port plug).

Labeling

PN:	**QFBR-5978AZ-2**
PHILIPPINES:	**Refers to Country of Origin**
2109:	**(YYWW) Year and Workweek**
SN FORMAT:	**ATYYWWXXXX**

PROFINET Pin Descriptions

Pin 1 Sda
Data line for the two-wire serial interface. This data line should be pulled up with a 4.7-kΩ to 10-kΩ resistor value on the host board to a supply of 3.3V ± 10%.

Pin 2 RxGND
Receiver ground pin. RxGND is connected to TxGND inside of the transceiver. Connect this pin to the ground plane of the host board.

Pin 3 RxVcc
Receiver power supply pin. Provides+3.3V DC through a receiver power supply filter circuit (see Figure 4). Locate the power supply filter circuit as close as possible to the RxVcc pin. RxVcc and TxVcc shall be powered at same time.

Pin 4 Sd
Signal detect pin. If an optical signal is present at the input of the receiver, Sd output is at logic “1”. The absence of an optical signal to the receiver results in Sd output at a logic “0”. This signal detect output can be used to drive an LVPECL input on an upstream circuit. Proper LVPECL termination should be in place. (See Figure 4.)

Pin 5 Rdata-
Negative receiver data-out. This data line is a 3.3V LVPECL compatible differential line. This data line should be properly terminated with a 130Ω pull-up to Vcc and an 82Ω pull-down to ground (see Figure 4).

Pin 6 Rdata+
Positive receiver data-out. This data line is a 3.3V LVPECL compatible differential line. This data line should be properly terminated with a 130Ω pull-up to Vcc and an 82Ω pull-down to ground (see Figure 4).

Pin 7 TxVcc
Transmitter power supply pin. Provides +3.3V DC through a transmitter power supply filter circuit (see Figure 4). Locate the power supply filter circuit as close as possible to the TxVcc pin. TxVcc and RxVcc shall be powered at same time.

Pin 8 TxGND
Transmitter ground. TxGND is connected to RxGND inside of the transceiver. Connect this pin to the ground plane on the host board.

Pin 9 Txdis
Transmitter disable input. This input is used to shut down the transmitter light output. It is internally pulled up with an ~8-kΩ resistor.

- Low (0V–0.8V) – Transmitter on
- Between (0.8V–2.0V) – Undefined
- High (2.0V–3.63V) – Transmitter off
- Open – Transmitter off

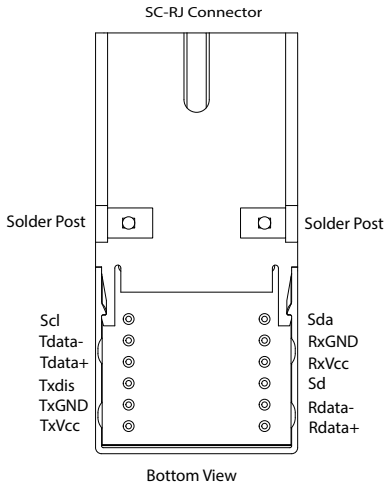
Pin 10 Tdata+
Positive transmitter data-in. This data line is internally AC-coupled. A 100Ω termination resistor is included between the Tdata+ and Tdata- data lines.

Pin 11 Tdata-
Negative transmitter data-in. This data line is internally AC-coupled. A 100Ω termination resistor is included between the Tdata+ and Tdata- data lines.

Pin 12 Scl
This is a clock line of the two-wire serial interface. This data line should be pulled up with a 4.7-kΩ to 10-kΩ resistor on the host board to a supply of 3.3V ± 10%.

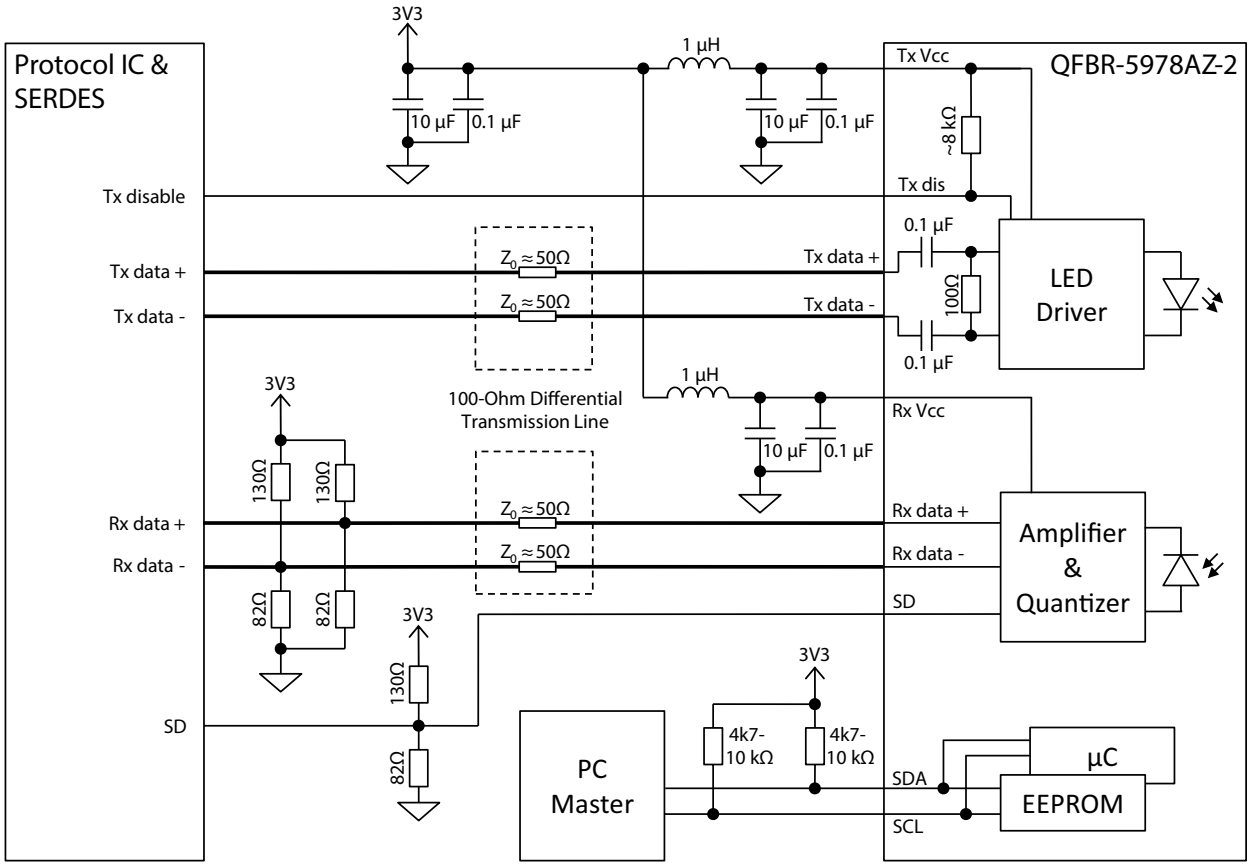
Solder Post
In case of using a connector with a metal ferrule, these posts are electrically contacted to the ferrule front. It is recommended to connect the solder posts to chassis ground to optimize immunity to ESD and EMI.

Figure 3: Pinout Diagram



NOTE: The metal back part of the transceiver housing is connected internally to GND level. Avoid any contact to the signal layers or any other electrical component.

Figure 4: Recommended Termination Circuit



Board Layout – Decoupling Circuit and Ground Planes

It is important to take care in the layout of your circuit board to achieve optimum performance from the transceiver. A power supply decoupling circuit is recommended to filter noise and to ensure optimal product performance. It is further recommended that a contiguous ground plane be provided in the circuit board directly under the transceiver to provide a low-inductance ground for the signal return current. This recommendation adheres to good high-frequency board layout practices.

Functional Data Input/Output

The LVPECL transmitter input is internally AC-coupled and terminated, so there is no need for any further external components. The LVPECL receiver output can be DC-coupled to the LVPECL-compliant network interface through a Thevenin's equivalent transformation. For a 3.3V power supply, the LVPECL outputs should be pulled up to Vcc with a 130Ω resistor and pulled down to ground with an 82Ω resistor. Both coupling resistors should be placed close to the network interface IC (see Figure 4).

AC coupling can be used for systems in which the transceiver and connected logic are at different supply voltages. For AC coupling, the coupling capacitor should be large enough (typically 100 nF) to avoid excessive low-frequency droop when the data signal contains long strings of consecutive identical symbols. The LVPECL outputs must be pulled down to ground first to DC-bias the output before AC coupling. Because the LVPECL output common-mode voltage is fixed at Vcc – 1.3V, the DC-biasing resistor can be selected by assuming a 14-mA DC current. This results in a bias-resistor value of typically 150Ω. After the AC-coupling capacitors, a Thevenin's equivalent transformation connects to the LVPECL-compatible network interface, equal to the one used in DC coupling.

Digital Diagnostic Monitoring Interface

The transceiver features an enhanced digital diagnostic interface, compatible with the “Digital Diagnostic Monitoring Interface for Optical Transceivers” SFF-8472 Multi-source Agreement (MSA). Refer to the MSA document to access information on the range of options, both hardware and software, available to the host system for using the available digital diagnostic features.

The enhanced digital interface allows real-time access to device operating parameters and includes optional digital features, such as soft control and monitoring of I/O signals. In addition, it fully incorporates the functionality needed to implement digital alarms and warnings, as defined by the SFF-8472 MSA. The digital diagnostic monitoring interface allows the user to perform component monitoring, fault isolation, and failure prediction in transceiver-based applications. The diagnostic monitoring interface (DMI) has two 256-byte memory maps in EEPROM that are accessible over a two-wire interface: the serial ID memory map at address 1010000X (0xA0) and the digital diagnostic memory map at address 1010001X (0xA2).

The serial ID memory map contains a serial identification and vendor-specific information. This information is read only.

The digital diagnostic memory map contains device operating parameters as well as alarm and warning flags. The operating parameters are retrieved through a sequential read command, ensuring that the MSB and LSB of each parameter are “coherent”. Furthermore, it contains 120 bytes that can be written by the user as well as a writable soft control byte.

For applications that require continuously updated alarm and warning limits, it is recommended to use the available real-time monitor in combination with software algorithms. Avoid continuous writing to alarm or warning registers. Write alarm and warning registers only once after transceiver power-up.

Table 1 to Table 6 show details of memory contents, timing characteristics, soft commands, and alarm and warning flags.

Figure 5: Digital Diagnostic Memory Map – Specific Data Field Description (from SFF-8472 MSA)

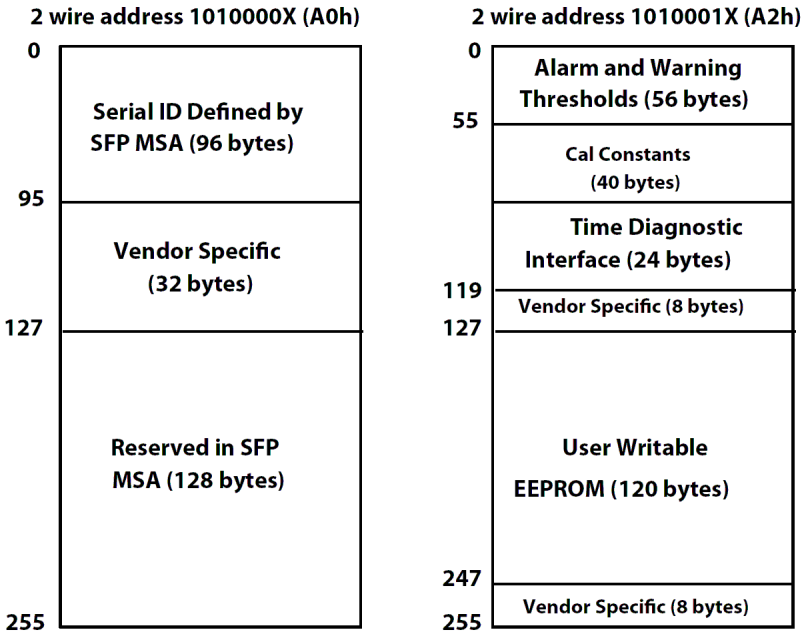


Table 1: Transceiver Soft Diagnostics Timing Characteristics

Parameter	Symbol	Min.	Max.	Units	Notes
Hardware TX_DISABLE assert time	$t_{\_off}$	—	10	µs	Note [a], Figure 6
Hardware TX_DISABLE de-assert time	$t_{\_on}$	—	1	ms	Note [b], Figure 6
Time to initialize	$t_{\_init}$	—	100	ms	Note [c], Figure 6
Hardware RX_SD assert time	$t_{\_SD\_on}$	—	100	µs	d
Hardware RX_SD de-assert time	$t_{\_SD\_off}$	—	100	µs	e
Software TX_DISABLE assert time	t_{off_soft}	—	100	ms	f
Software TX_DISABLE de-assert time	t_{on_soft}	—	100	ms	g
Software RX_SD assert time	$t_{SD\_ON\_soft}$	—	100	ms	h
Software RX_SD de-assert time	$t_{SD\_OFF\_soft}$	—	100	ms	i
Analog parameter data ready	t_{data}	—	1000	ms	j
Serial bus hardware ready	t_{serial}	—	300	ms	k
Write cycle time	t_{write}	—	10	ms	l
Serial ID clock rate	f_{serial_clk}	—	400	kHz	

a. Time from the rising edge of TX_DISABLE to when the optical output falls below 10% of nominal.

b. Time from the falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal.

c. Time from power-on or the falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal.

d. Time from a valid optical signal to RX_SD assertion.

e. Time from the loss of an optical signal to RX_SD de-assertion.

f. Time from two-wire interface assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the optical output falls below 10% of nominal. Measured from the falling clock edge after the stop bit of the write transaction.

g. Time from two-wire interface de-assertion of TX_DISABLE (A2h, byte110, bit 6) to when the modulated optical output rises above 90% of nominal.

h. Time for two-wire interface assertion of RX_SD (A2h, byte 110, bit 1) from the presence of a valid optical signal.

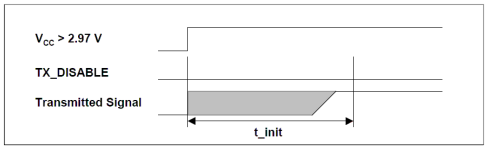
i. Time for two-wire interface de-assertion of RX_SD (A2h, byte 110, bit 1) from the loss of an optical signal.

j. From power-on to data ready bit asserted (A2h, byte 110, bit 0). Data ready indicates that analog monitoring circuitry is operational.

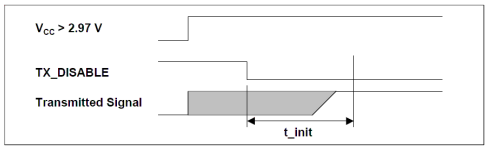
k. Time from power-on until the module is ready for data transmission over the serial bus (reads or writes over A0h and A2h).

l. Time from the stop bit to completion of a 1-byte to 8-byte write command.

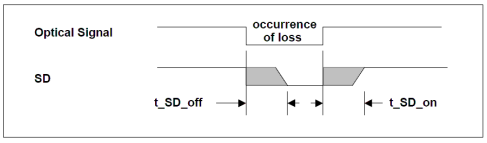
Figure 6: Transceiver Timing Diagrams



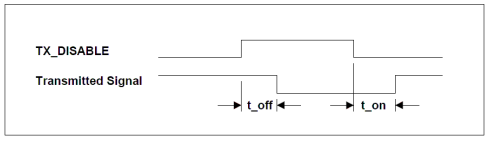
t_init: TX_DISABLE Deasserted



t_init: TX_DISABLE Asserted



tx_SD_off and tx_SD_on



t_off and t_on: TX Disable Asserted Then Deasserted

Table 2: Transceiver Digital Diagnostic Monitor Characteristics

Parameter	Symbol	Min.	Units	Notes
Transceiver internal temperature accuracy	T_{INT}	± 5.0	°C	Registers indicate case temperature that is derived from the internally measured temperature. Valid from –40°C to +90°C case temperature with Tx enabled.
Transceiver internal supply voltage accuracy	V_{INT}	± 0.1	V	Rx supply voltage is measured internal to the transceiver voltage and can, with less accuracy, be correlated to the voltage at the Vcc pin. Valid over 3.3V ± 10%.
Transmitter LED bias current	I_{Bias}	—	—	Typical value of 20 mA. Only for information.
Transmitted average optical output power – POF	$P_{T, POF}$	—	—	Coupled into 1-mm POF. Typical value of –4.25 dBm. Only for information.
Received average optical input power accuracy – POF	$P_{R, POF}$	± 1.5	dB	Coupled from 1-mm POF.
Received average optical input power accuracy – HCS	$P_{R, HCS}$	± 1.5	dB	Coupled into 200-µm HCS fiber. Note [a].
Received optical modulation amplitude (OMA) margin accuracy – POF	$P_{ROMA, POF}$	± 1.5	dB	Coupled from 1-mm POF. Valid over Rx. OMA margin range: 0 dB to +6 dB. Notes [b, c, d].
		± 2.5	dB	Coupled from 1-mm POF. Valid over Rx. OMA margin range: above +6 dB. Notes [b, c, d].
Received optical modulation amplitude (OMA) margin accuracy – HCS	$P_{ROMA, HCS}$	± 1.5	dB	Coupled from 200-µm HCS fiber. Valid over Rx. OMA margin range: 0 dB to +6 dB. Notes [b, c, d].
		± 2.5	dB	Coupled from 200-µm HCS fiber. Valid over Rx. OMA margin range: above +6 dB. Notes [b, c, d].

a. When HCS fiber is used, the register read-back value must be offset by –1.6 dB to obtain the actual HCS Rx power.

b. Received optical modulation amplitude margin or Rx OMA margin is a measure for the reserve in OMA to sensitivity. The accuracy is defined as the difference between reported Rx OMA margin and the actual margin relative to the 0-dB point.

c. The register read-back value must be offset by –1.6 dB for a stressed link to obtain the actual Rx OMA margin.

d. The OMA margin is calibrated using a PRBS7 pattern.

Table 3: EEPROM Serial ID Memory Contents – Address A0h

Address	Hex	ASCII	Description	Address	Hex	ASCII	Description
0	00			40	51	Q	
1	00			41	46	F	
2	00			42	42	B	
3	00			43	52	R	
4	00			44	2D	-	
5	00			45	35	5	
6	00			46	39	9	
7	00			47	37	7	
8	00			48	38	8	
9	00			49	41	A	
10	00			50	5A	Z	
11	00			51	2D	-	
12	00			52	32	2	
13	00			53	20		
14	00			54	20		
15	00			55	20		
16	00			56	20		
17	00			57	20		
18	00			58	20		
19	00			59	20		
20	41	A		60	02		Note [a]
21	56	V		61	8A		Note [a]
22	41	A		62	00		
23	47	G		63	8E		Note [b]
24	4F	O		64	00		
25	20			65	14		
26	54	T		66	00		
27	45	E		67	00		
28	43	C		68–83			Note [c]
29	48	H		84–91			Note [d]
30	20			92	68	h	
31	20			93	D0		
32	20			94	01		
33	20			95			Note [b]
34	20			96–127			Note [e]
35	20						
36	00						
37	00						
38	17						
39	6A						

a. The LED wavelength is represented in 16 unsigned bits. The hexadecimal representation of 650 (nm) is 0x28A.

b. Byte 95 contains the lower-order 8 bits of the sum of bytes 64–94, and Byte 63 contains the lower-order 8 bits of the sum of bytes 0–62. They are calculated (per SFF-8472) and stored prior to product shipment.

c. Address 68–83 specifies a unique module serial number.

d. Address 84–91 specifies the date code.

e. Address 96–127 is vendor specific.

Table 4: EEPROM DMI Memory Contents – Address A2h

Address	Hex	Dec	Description
0	5A	90	Temp H alarm MSB [a]
1	00	0	Temp H alarm LSB [a]
2	D8	216	Temp L alarm MSB [a]
3	00	0	Temp L alarm LSB [a]
4	55	85	Temp H warning MSB [a]
5	00	0	Temp H warning LSB [a]
6	E7	231	Temp L warning MSB [a]
7	00	0	Temp H warning LSB [a]
8	98	152	Rx Vcc H alarm MSB [g]
9	58	88	Rx Vcc H alarm LSB [g]
10	69	105	Rx Vcc L alarm MSB [g]
11	78	120	Rx Vcc L alarm LSB [g]
12	8D	141	Rx Vcc H warning MSB [g]
13	CC	204	Rx Vcc H warning LSB [g]
14	74	116	Rx Vcc L warning MSB [g]
15	04	4	Rx Vcc L warning LSB [g]
16	75	117	Tx Bias H alarm MSB [i]
17	30	48	Tx Bias H alarm LSB [i]
18	03	3	Tx Bias L alarm MSB [i]
19	E8	232	Tx Bias L alarm LSB [i]
20	75	117	Tx Bias H warming MSB [i]
21	30	48	Tx Bias H warming LSB [i]
22	03	3	Tx Bias L warming MSB [i]
23	E8	232	Tx Bias L warming LSB [i]
24	1B	27	Tx Pwr H alarm MSB [j]
25	58	88	Tx Pwr H alarm LSB [j]
26	01	1	Tx Pwr L alarm MSB [j]
27	F4	244	Tx Pwr L alarm LSB [j]
28	17	23	Tx Pwr H warning MSB [j]
29	70	112	Tx Pwr H warning LSB [j]
30	03	3	Tx Pwr L warning MSB [j]
31	E8	232	Tx Pwr L warning LSB [j]
32	FF	255	Rx Pwr H alarm MSB [k]
33	DC	220	Rx Pwr H alarm LSB [k]
34	00	0	Rx Pwr L alarm MSB [k]
35	00	0	Rx Pwr L alarm LSB [k]

Address	Hex	Dec	Description
40	08	8	Rx OMA Margin L alarm [b, c]
41	12	18	Rx OMA Margin L warning [b, c]
42–55			Reserved [d]
56–94			Note [e]
95	DA	218	Checksum for bytes 0–94 [f]
96			Real-time temperature MSB [a]
97			Real-time temperature LSB [a]
98			Real-time Rx Vcc MSB [g]
99			Real-time Rx Vcc LSB [g]
100			Real-time Tx Bias MSB [i]
101			Real time Tx Bias LSB [i]
102			Calibrated Tx Pwr MSB [j, h]
103			Calibrated Tx Pwr LSB [j, h]
104			Real-time Rx Pwr MSB [k]
105			Real-time Rx Pwr LSB [k]
106			Real-time Rx OMA Margin [b, c]
107			Reserved [d]
108			Reserved [d]
109			Reserved [d]
110			Status control – see Table 5
111			Reserved [d]
112			Flag bit – see Table 6
113			Flag bit – see Table 6
114			Reserved [d]
115			Reserved [d]
116			Flag bit – see Table 6
117			Flag bit – see Table 6
118			Reserved [d]
119–127			Vendor specific
128–247			Customer writable
248–255			Vendor specific

Table 4: EEPROM DMI Memory Contents – Address A2h (Continued)

Address	Hex	Dec	Description
36	FF	255	Rx Pwr H warming MSB [k]
37	DC	220	Rx Pwr H warming LSB [k]
38	00	0	Rx Pwr L warming MSB [k]
39	00	0	Rx Pwr L warming LSB [k]

Address	Hex	Dec	Description

a. Temperature (Temp) is decoded as a 16-bit signed two's complement integer in increments of 1/256°C.
b. Received optical modulation amplitude margin or Rx OMA margin is a measure for the reserve in OMA to sensitivity.
c. Received OMA margin is decoded as an 8-bit signed two's compliment integer in increments of 0.2 dB.
d. Reserved registers return "00" when read. A write to a reserved register is acknowledged but not stored.
e. Bytes 56–94 are not intended for use with QFBR-5978AZ-2 but have been set to default values per SFF-8472.
f. Byte 95 is a checksum calculated (per SFF-8472) and stored prior to product shipment.
g. Rx supply voltage (RxVcc) is decoded as a 16-bit unsigned integer in increments of 100 µV.
h. Transmitted average optical power is factory calibrated at room temperature and is for information only.
i. LED bias current (Tx Bias) is decoded as a 16-bit unsigned integer in increments of 2 µA. Typical value and for information only.
j. Transmitted average optical power (Tx Pwr) is decoded as a 16-bit unsigned integer in increments of 0.1 µW.
k. Received average optical power (Rx Pwr) is decoded as a 16-bit unsigned integer in increments of 0.1 µW.

Table 5: EEPROM Serial ID Memory Contents – Soft Commands (Address A2h, Byte 110)

Bit	Status/Control Name	Description	Notes
7	TX_DISABLE State	Digital state of the TX_DISABLE input pin (logic 1 = TX_DISABLE asserted)	a
6	Soft TX_DISABLE	Read/write bit for changing the digital state of the TX_DISABLE function	a, b
5	Reserved	—	c
4	Not supported	—	d
3	Not supported	—	e
2	Not supported	—	f
1	RX_SD State	Digital state of the RX_SD output pin (logic 0 = RX_SD asserted)	a
0	Data Ready (Negated)	Indicates that the transceiver is powered and real-time sense data is ready (0 = ready)	g

a. The response time for soft commands of the QFBR-5978AZ-2 is 100 ms as specified by the MSA SFF-8472.
b. Bit 6 is logic ORed with the TX_DISABLED input pin. Either asserted will disable the transmitter.
c. Reserved bits return "0" when read. A write to a reserved bit is acknowledged but not stored.
d. A read from bit 4 returns "1". A write is acknowledged but not stored.
e. A read from or a write to bit 3 is acknowledged and stored but is ignored by the transceiver.
f. A read from bit 2 returns "0". A write is acknowledged but not stored.
g. Meets the MSA SFF-8472 data ready timing of 1000 ms.

Table 6: EEPROM Serial ID Memory Contents – Alarm and Warnings (Address A2h, Bytes 112, 113, 116, and 117)

Byte	Bit	Flag Bit Name	Description
112	7	Temp high alarm	Set when the transceiver internal temperature exceeds the high alarm threshold
	6	Temp low alarm	Set when the transceiver internal temperature exceeds the low alarm threshold
	5	Rx Vcc high alarm	Set when the transceiver internal supply voltage exceeds the high alarm threshold
	4	Rx Vcc low alarm	Set when the transceiver internal supply voltage exceeds the low alarm threshold
	3	Tx Bias high alarm	Set when the transceiver LED bias current exceeds the high alarm threshold [a]
	2	Tx Bias low alarm	Set when the transceiver LED bias current exceeds the low alarm threshold [a]
	1	Tx Power high alarm	Set when the transmitted average optical power exceeds the high alarm threshold [a]
	0	Tx Power low alarm	Set when the transmitted average optical power exceeds the low alarm threshold [a]
113	7	Rx Power high alarm	Set when the received average optical power exceeds the high alarm threshold
	6	Rx Power low alarm	Set when the received average optical power exceeds the low alarm threshold
	5	Rx OMA Margin alarm	Set when the received Rx OMA margin is less than or equal to the low alarm threshold
	4–0	Reserved	Note [b]
116	7	Temp high warning	Set when the transceiver internal temperature exceeds the high warning threshold
	6	Temp low warming	Set when the transceiver internal temperature exceeds the low warning threshold
	5	Rx Vcc high warning	Set when the transceiver internal supply voltage exceeds the high warning threshold
	4	Rx Vcc low warning	Set when the transceiver internal supply voltage exceeds the low warning threshold
	3	Tx Bias high warning	Set when the transceiver LED bias current exceeds the high warning threshold [c]
	2	Tx Bias low warning	Set when the transceiver LED bias current exceeds the low warning threshold [c]
	1	Tx Power high warning	Set when the transmitted average optical power exceeds the high warning threshold [c]
	0	Tx Power low warning	Set when the transmitted average optical power exceeds the low warning threshold [c]
117	7	Rx Power high warning	Set when the received average optical power exceeds the high warning threshold
	6	Rx Power low warning	Set when the received average optical power exceeds the low warning threshold
	5	Rx OMA Margin warning	Set when the received Rx OMA margin is less than or equal to the low warning threshold
	4–0	Reserved	Note [b]

a. Bit returns “0” when read. The alarm flag is not functional.

b. Reserved bits return “0” when read. A write to a reserved bit is acknowledged but not stored.

c. Bit returns “0” when read. The warning flag is not functional.

Regulatory Compliance Table

Feature	Test Method	Performance [a]
Electrostatic Discharge (ESD) HBM	JEDEC JS-001-2017	Withstands 1-kV, 1.5-kV, and 2-kV HBM applied between the electrical pins.
Electrostatic Discharge (ESD) Air and Contact Discharge	IEC 61000-4-2	Level 3 Air discharge ESD resistance ± 8 kV. Contact discharge ESD resistance ± 6 kV. Withstands an electrostatic discharge without damage when the SC-RJ connector receptacle is contacted. Single-bit errors may occur, but no synchronization loss was observed.
Immunity (EMI)	IEC 61000-4-3	20-V/m electric field immunity Shows no measurable effect from an electric field applied to the transceiver when mounted to a circuit board without a chassis enclosure.
Emission (EMI)	IEC 61000-6-4 + A1	System margins are dependent on customer board and chassis design.
Eye Safety	EN60950-1: 2006+A11+A1+A12+A2 EN60825-1: 2014 EN60825-2: 2004+A1+A2	AEL Class 1, TÜV Certificate number R50217706
Component Recognition	Underwriter Laboratories	File E173874

a. To reach the performance stated in this table, the solder posts were connected to ground.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device or cause a malfunction. Limits apply to each parameter in isolation; all other parameters have values within the recommended operating conditions. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	–40	+100	°C	
Case Operating Temperature	T_C	–40	+90	°C	a
Lead Soldering Temperature	T_{Sold}	—	+260	°C	b
Lead Soldering Time	t_{Sold}	—	10	s	b
Supply Voltage	V_{CC}	–0.5	4.0	V	
Receiver Average Input Power	P_{RX}	—	–2	dBm	
Data Input Voltage	V_I	–0.5	V_{CC}	V	
Transmitter Disable Voltage	V_{TxDis}	—	RxV_{CC}	V	
Differential Input Voltage (peak to peak)	V_{Diff}	—	2	V	
Output Current PECL	ID_{Out}	–40	40	mA	
ESD-Resistance – HBM	V_{ESD}	–2	+2	kV	c
ESD-Resistance – Air Discharge	V_{ESD}	–8	+8	kV	d
ESD-Resistance – Contact Discharge	V_{ESD}	–6	+6	kV	e
Electric Field Immunity	V_{EMI}	—	20	V/m	f
EEPROM Write/Erase Cycles	WE_{Cyc}	—	10,000	Cycles	

a. Operating the product outside the maximum rated case operating temperature range will compromise its reliability and may damage the product. Case temperature is defined as the temperature measured with the thermocouple placed in the center of the top surface of the metal cover.

b. The transceiver is Pb-free wave solderable. The moisture sensitivity level is 3.

c. Human Body Model (HBM): JEDEC JS-001-2012.

d. Air discharge IEC 61000-4-2 level 3 ESD resistance for the transceiver.

e. Contact discharge IEC 61000-4-2 level 3 ESD resistance for the transceiver.

f. According to IEC 61000-4-3.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Case Operating Temperature	T_C	–40	—	+90	°C	a
Supply Voltage	V_{CC}	2.97	3.3	3.63	V	
Data and Signal Detect Output Load	R_L	—	50	—	Ω	
Signaling Rate (Fast Ethernet)	B	—	125	—	MBd	b
Humidity	—	5	—	95	%	

a. Electrical and optical specifications of the product are guaranteed across the recommended case operating temperature range only.

b. 4B/5B coding.

Transceiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Transceiver Supply Current	I_{CC}	—	80	120	mA	a
Power Dissipation	P_{Diss}	—	265	440	mW	
Power Supply Noise Rejection (peak-to-peak)	P_{SNR}	50	—	—	mV	
Transmitter Propagation Delay	T_{PD}	5.5	7	8.5	ns	
Receiver Propagation Delay	R_{PD}	3.5	6	10	ns	b

a. The current consumption of the external termination circuit on the receiver side is not considered.
b. The receiver propagation delay strongly depends on the light input power. Typical value was measured at –20 dBm.

Transmitter Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Differential Input Voltage (peak-to-peak)	V_{Diff}	400	800	1600	mV	
Differential Input Impedance	R_{Diff}	80	100	120	Ω	a

a. Internally AC-coupled (see Figure 4). Impedance measured on IC level.

Transmitter Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Average Launched Power (1-mm POF, NA = 0.5)	$P_{O,\ POF}$	–8.0	–5.2	–2.0	dBm	a
Optical Modulation Amplitude (POF) (peak to peak)	OMA_{POF}	–6.0	–2.3	–0.5	dBm	a
Average Launched Power (200-µm HCS, NA = 0.37)	$P_{O,\ HCS}$	–19.0	–15.9	–11.0	dBm	b
Optical Modulation Amplitude (HCS) (peak-to-peak)	OMA_{HCS}	–17.0	–12.9	–8.0	dB	b
Central Wavelength	λ_C	635	650	660	nm	a, c
Spectral RMS	$\Delta\lambda$	—	—	17	nm	a, d
Optical Rise Time (10%–90%)	t_R	—	3.4	6.5	ns	a
Optical Fall Time (90%–10%)	t_F	—	2.7	6.5	ns	a
Duty Cycle Distortion (peak-to-peak)	DCD	–1.0	—	+1.0	ns	a
Random Jitter (peak-to-peak)	RJ	—	—	0.7	ns	a, e
Overshoot	Ov	—	—	40	%	a

a. Measured at the end of 1m POF cable.
b. Measured at the end of 1m HCS cable.
c. Central wavelength is defined as:

$$\lambda_c = \frac{\sum_{i=1}^{N} P_i \lambda_i}{\sum_{i=1}^{N} P_i}$$

where P_i is the optical power at λ_i.

Reference: EIA/TIA Standard FOTP-127/6.1, 1991

d. Spectrum RMS is defined as:

$$\lambda_w = \left[\left(\frac{\sum_{i=1}^{N} P_i \lambda_i^2}{\sum_{i=1}^{N} P_i} \right) - \lambda_c^2 \right]^{\frac{1}{2}}$$

Reference: EIA/TIA Standard FOTP-127/6.3, 1991

e. According to Technical Specification for PROFINET, version 1.0 (Jan 2008).

Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Data Output Voltage – Low	$V_{OL} – V_{CC}$	–2.2	–1.75	–1.5	V	a
Data Output Voltage – High	$V_{OH} – V_{CC}$	–1.2	–1.05	–0.7	V	a
Data Output Voltage Swing	$\|V_{OH} – V_{OL}\|$	400	—	800	mV	a, b
Data Output Rise Time (10%–90%)	t_R	0.35	0.8	2.2	ns	a
Data Output Fall Time (90%–10%)	t_F	0.35	0.8	2.2	ns	a
Duty Cycle Distortion (peak-to-peak)	DCD	–1.0	—	+1.0	ns	a
Data Dependent Jitter (peak-to-peak)	DDJ	—	—	1.5	ns	a
Random Jitter (peak-to-peak)	RJ	—	—	0.7	ns	a, c, d
Signal Detect Output Voltage – Low	$V_{OL} – V_{CC}$	–2.2	–1.75	–1.5	V	a
Signal Detect Output Voltage – High	$V_{OH} – V_{CC}$	–1.2	–1.05	–0.7	V	a

a. LVPECL termination (130Ω to Vcc and 82Ω to ground).

b. Single ended.

c. Maximum random jitter for receiver input power of –5 dBm, according to Technical Specification for PROFINET, version 1.0 (Jan. 2008).

d. Maximum random jitter is 3 ns for input power at the end of 1m POF fiber at –23 dBm (OMA).

Receiver Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Unstressed Receiver Sensitivity, OMA (POF) (peak-to-peak)	OMA_{POF}	–25.5	—	—	dBm	a
Unstressed Receiver Sensitivity, OMA (HCS) (peak-to-peak)	OMA_{HCS}	–27	—	—	dBm	b
Optical Power Maximum, OMA (POF) (peak-to-peak)	$P_{In,\ POF}$	—	—	+1	dBm	c
Optical Power Maximum, OMA (HCS) (peak-to-peak)	$P_{In,\ HCS}$	—	—	–4	dBm	c
Operating Wavelength	λ_O	635	650	660	nm	
Signal Detect Asserted	P_A	—	7	—	dB	d
Signal Detect De-asserted	P_D	—	11	—	dB	d
Signal Detect Hysteresis	$P_A – P_D$	1.5	4	—	dB	e

a. Measured at the end of 1m POF cable with PRBS7 pattern signal, BER < 2.5×10^{-10}.

b. Measured at the end of 1m HCS cable with PRBS7 pattern signal, BER < 2.5×10^{-10}.

c. Maximum input optical power is defined as the maximum optical modulation amplitude where the receiver duty cycle reaches ±1 ns.

d. Signal detect assert and de-assert levels are indicated as dB below the unstressed receiver sensitivity level for either POF or HCS.

e. Measured with a PRBS7 pattern.

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