Data Sheet

ACPL-M75N

High-Speed 15-Mbaud Digital CMOS Optocoupler

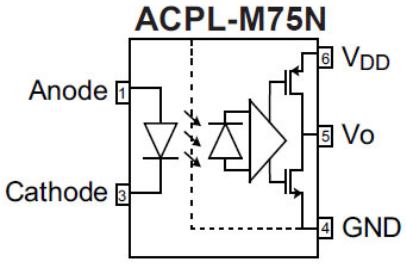
Description

The Broadcom® ACPL-M75N optocoupler uses LED, packaging, and CMOS IC technologies to achieve excellent optical galvanic isolation at data rate of up to 15 Mbaud.

An internal Faraday shield provides a guaranteed common-mode transient immunity specification of 30 kV/µs minimum.

The basic building blocks of the optocoupler are a high-speed LED and a CMOS detector IC. The detector IC incorporates an integrated photodiode, a high-speed transimpedance amplifier, and a voltage comparator with an output driver.

Functional Diagram



NOTE: The connection of a 0.1-µF bypass capacitor between pins V_{DD} and GND is recommended.

Truth Table

LED	Output V_O
ON	LOW
OFF	HIGH

Features

- Superior optical isolation and insulation
- 3.3V and 5V CMOS compatibility
- Low power I_{DD}: 1.5 mA max.
- Low LED driving current I_F: 4 mA min.
- Data rate: 15 Mbaud min.
- 30 kV/µs min common-mode rejection (CMR)
- –40°C to +125°C operating temperature range
- SO-5 package
- Safety and regulatory approvals:
  - IEC/EN 60747-5-5 Insulation Working Voltage: 567 V_{PK}
  - UL 1577 Isolation Voltage: 3750 V_{RMS}/1 min.
  - CAN/CSA-C22.2 No. 62368-1

Applications

- Communication interfaces: RS485, CANBus, and I^2C
- Microprocessor system interfaces
- Digital isolation for A/D and D/A converters

CAUTION! Take normal static precautions in handling and assembly of this component to prevent damage, degradation, or both that may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments. The components are not AEC-Q100 qualified and not recommended for automotive applications.

Recommended Reflow Soldering Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

NOTE: Non-Halide Flux should be used.

Ordering Information

The ACPL-M75N is UL recognized with an isolation voltage of 3750 V_{rms} for 1 minute per UL1577. All devices are RoHS-compliant.

Part Number	Option RoHS-Compliant	Package	Surface Mount	Tape and Reel	IEC/EN 60747-5-5	Quantity
ACPL-M75N	-000E	SO-5	X			100 per tube
	-060E		X		X	100 per tube
	-500E		X	X		1500 per reel
	-560E		X	X	X	1500 per reel

To form an ordering part number, choose a part number from the part number column and combine it with the desired option from the RoHS option column.

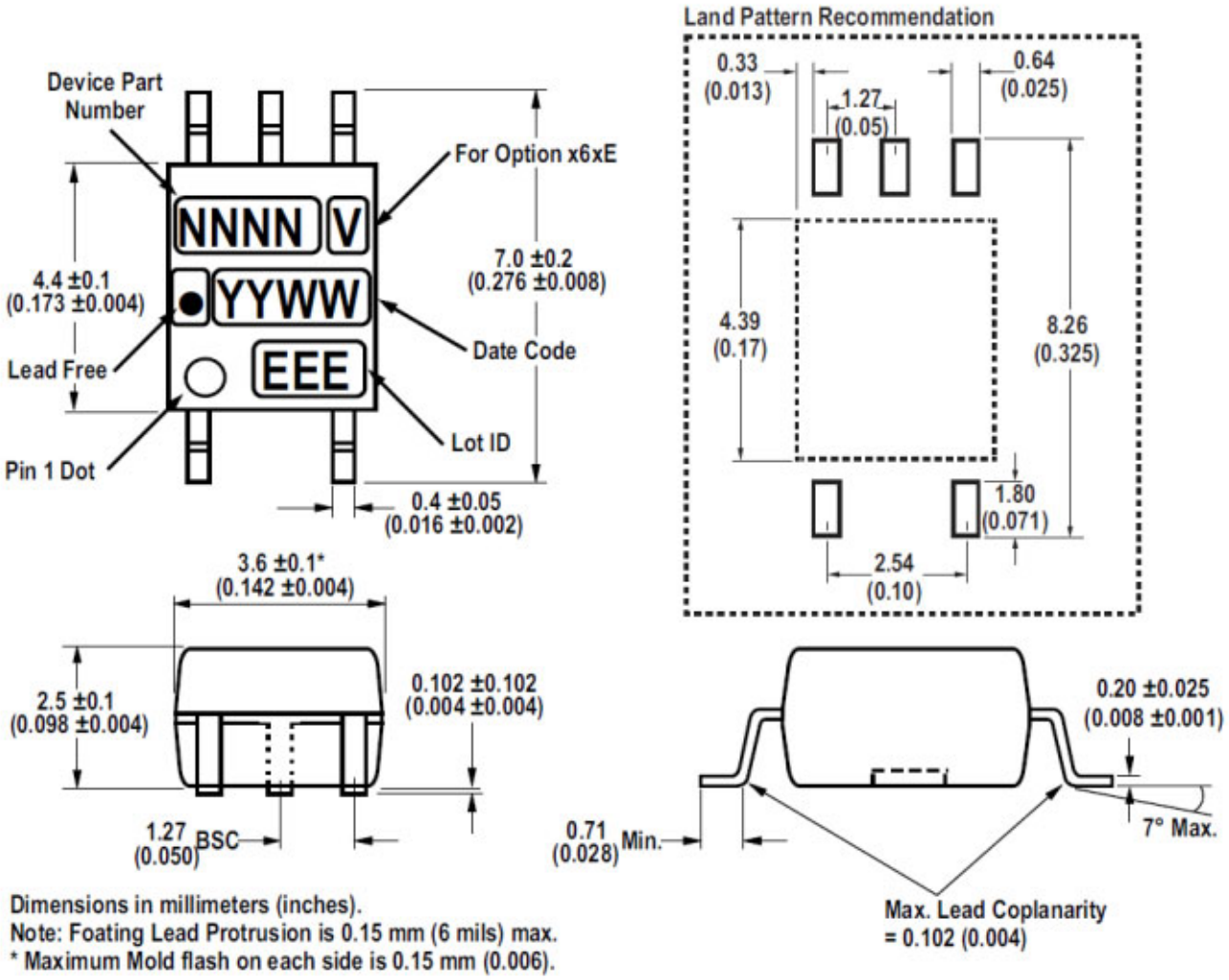
Example:

Part number ACPL-M75N-560E describes an optocoupler with a surface-mount SO-5 package; delivered in Tape and Reel with 1500 parts-per-reel; with IEC/EN 60747-5-5 Safety Approval; and full RoHS compliance.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawings

Figure 1: ACPL-M75N SO-5 Package



Regulatory Information

IEC/EN 60747-5-5	Options 060, 560 only
UL	Approved under UL 1577, component recognition program, File E55361
CSA	Approved under CAN/CSA-C22.2 No. 62368-1

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	5.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	5.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photo-emitter and photo-detector inside the optocoupler cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	≥ 175	V	VDE 0303-11/DIN EN 60112
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1).

IEC/EN 60747-5-5 Insulation Related Characteristics (Option 060/560)

Parameter	Symbol	Characteristics	Units
Installation Classification per DIN VDE 0110/1.89, Table 1			
For Rated Mains Voltage ≤ 150 V_{RMS}		I-IV	
For Rated Mains Voltage ≤ 300 V_{RMS}		I-IV	
For Rated Mains Voltage ≤ 600 V_{RMS}		I-III	
For Rated Mains Voltage ≤ 1000 V_{RMS}		I-II	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	567	V_{PEAK}
Input to Output Test Voltage, Method b[a] V_{IORM} × 1.875 = V_{PR}, 100% Production, Test with t_m = 1s, Partial Discharge < 5 pC	V_{PR}	1063	V_{PEAK}
Input to Output Test Voltage, Method a[a] V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, Test with t_m = 10s, Partial Discharge < 5 pC	V_{PR}	907	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage, t_{ini} = 60s)	V_{IOTM}	6000	V_{PEAK}
Safety Limiting Values (Maximum values allowed in the event of a failure			
Case Temperature	T_S	150	°C
Input Current	$I_{S, INPUT}$	150	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	≥ 10^9	Ω

a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, IEC/EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

NOTE: These optocouplers are suitable for safe electrical isolation only within the safety limit data. Maintain the safety data by means of protective circuits.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Condition
Storage Temperature	T_S	–55	+125	°C	
Ambient Operating Temperature	T_A	–40	+125	°C	
IC Junction Temperature	T_J	—	+150	°C	
Supply Voltage	V_{DD}	0	6.5	V	
Output Voltage	V_O	–0.5	V_{DD} + 0.5	V	
Average Forward Input Current	I_F	—	20	mA	
Average Output Current	I_O	—	10	mA	
Peak Transient Input Current (I_F at 1-µs pulse width, <10% duty cycle)	$I_{F(tran)}$	—	1	A	< 1-µs pulse width, < 300 pulses/second
			80	mA	< 1-µs pulse width, < 10% duty cycle
Input Power Dissipation	P_I	—	35	mW	
Output Power Dissipation	P_O	—	30	mW	
Lead Solder Temperature	260°C for 10 seconds, 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Recommended Reflow Soldering Profile				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	–40	+125	°C
Supply Voltage	V_{DD}	4.5	5.5	V
		3.0	3.6	V
Forward Input Current	$I_{F(ON)}$	4	10	mA
Forward Off State Voltage	$V_{F(OFF)}$	—	0.8	V

Electrical Specifications (DC)

Over recommended ambient operating temperature (T_A = –40°C to +125°C), 3.0V ≤ V_{DD} ≤ 3.6V and 4.5V ≤ V_{DD} ≤ 5.5V. All typical specifications are at V_{DD} = +5V, T_A = +25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Forward Voltage	V_F	1.20	1.50	1.85	V	I_F = 6 mA (Figure 2)
Input Reverse Breakdown Voltage	BV_R	5	—	—	V	I_R = 10 µA
Logic High Output Voltage	V_{OH}	VDD – 0.6	VDD – 0.2	—	V	I_{OH} = –3.2 mA, I_F = 0 (Figure 5)
Logic Low Output Voltage	V_{OL}	—	0.25	0.60	V	I_{OL} = 4 mA, I_F = 6 mA (Figure 4)
Input Threshold Current	I_{TH}	—	0.7	3.5	mA	
Logic High Output Supply Current	I_{DDH}	—	0.9	1.5	mA	I_F = 0
Logic Low Output Supply Current	I_{DDL}	—	1.0	1.5	mA	I_F = 6 mA
Input Capacitance	C_{IN}	—	60	—	pF	f = 1 MHz, V_F = 0V
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	—	–1.5	—	mV/°C	

Switching Specifications (AC)

Over recommended ambient operating temperature (T_A = –40°C to +125°C), 3.0V ≤ V_{DD} ≤ 3.6V and 4.5V ≤ V_{DD} ≤ 5.5V. All typical specifications are at V_{DD} = +5V, T_A = +25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Propagation Delay Time to Logic Low Output[a]	t_{PHL}	—	36	55	ns	I_F = 6 mA, CMOS Signal Level (Figures 6, 7, 8, 9, 10)
Propagation Delay Time to Logic High Output[a]	t_{PLH}	—	30	55	ns	
Pulse Width Distortion[b]	| PWD |	—	6	25	ns	
Propagation Delay Skew[c]	t_{PSK}	—	—	25	ns	
Output Rise Time (10% to 90%)	t_R	—	6	—	ns	
Output Fall Time (90% to 10%)	t_F	—	5	—	ns	
Static Common-Mode Transient Immunity at Logic High Output[d]	CM_H	30	—	—	kV/µs	V_{CM} = 1000V, I_F = 6 mA, CMOS Signal Level, T_A = 25°C (Figure 11)
Static Common-Mode Transient Immunity at Logic Low Output[e]	CM_L	30	—	—	kV/µs	V_{CM} = 1000V, I_F = 6 mA, CMOS Signal Level, T_A = 25°C (Figure 12)

a. t_{PHL} propagation delay is measured from the 50% (V_{in} or I_F) on the rising edge of the input pulse to the 0.8V of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (V_{in} or I_F) on the falling edge of the input pulse to the 80% level of the rising edge of the V_O signal.

b. PWD is defined as $|t_{PHL} - t_{PLH}|$.

c. t_{PSK} is equal to the magnitude of the worst-case difference in t_{PHL}, t_{PLH}, or both that is seen between units at any given temperature within the recommended operating conditions.

d. CM_H is the maximum tolerable rate of rise of the common-mode voltage to assure that the output remains in a high logic state.

e. CM_L is the maximum tolerable rate of fall of the common-mode voltage to assure that the output remains in a low logic state.

Package Characteristics

All typical specifications are at T_A = +25°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary Withstand Voltage[a]	V_{ISO}	3750	—	—	V_{RMS}	RH ≤ 50%, t = 1 min, T_A = 25°C
Input-Output Resistance	R_{I-O}	—	10^{14}	—	Ω	V_{I-O} = 500 V dc
Input-Output Capacitance	C_{I-O}	—	0.6	—	pF	f = 1 MHz, T_A = 25°C

a. In accordance with UL 1577, ACPL-M75N are proof tested by applying an insulation test voltage ≥ 4500 V_{rms} for 1 second, (Leakage detection current limit, I_{I-O} ≤ 5 µA). 3750 V_{RMS} for 1-minute duration is equivalent to 4500 V_{RMS} for 1-second duration.

Performance Plots

Figure 2: Typical Diode Input Forward Current Characteristic

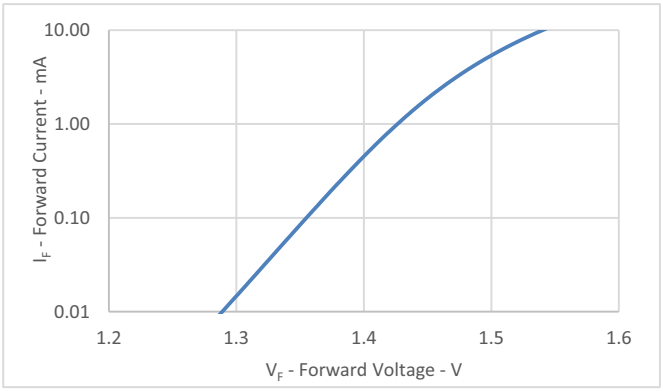


Figure 3: Typical Output Voltage vs. Input Forward Current

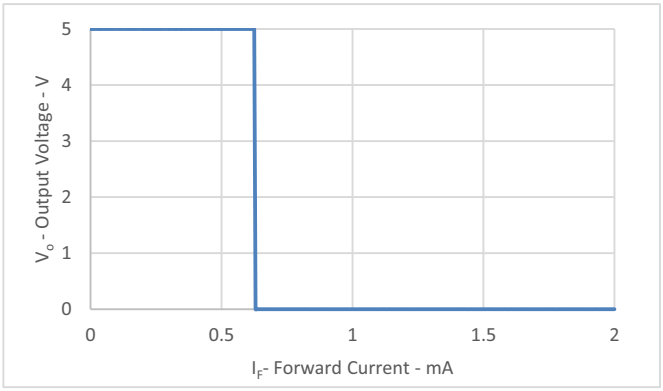


Figure 4: Typical Logic Low Output Voltage vs. Logic Low Output Current

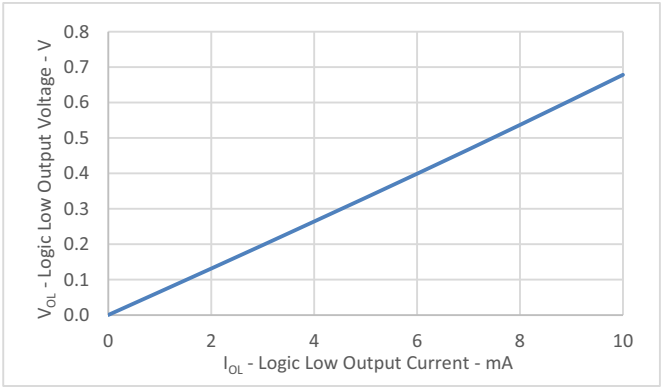


Figure 5: Typical Logic High Output Voltage vs. Logic High Output Current

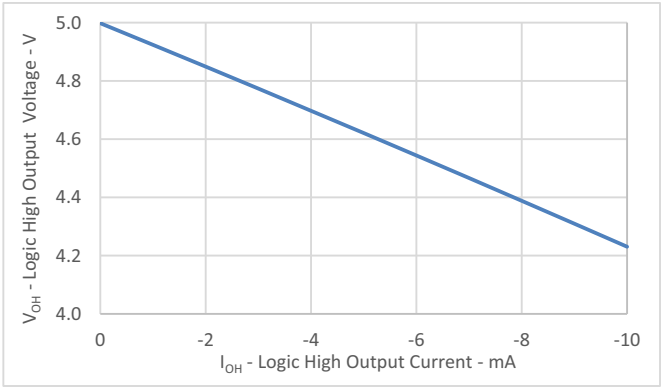


Figure 6: Typical Switching Speed vs. Temperature at 5V

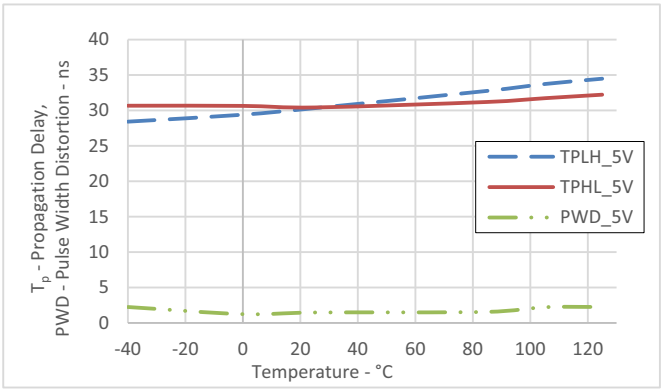


Figure 7: Typical Switching Speed vs. Temperature at 3V

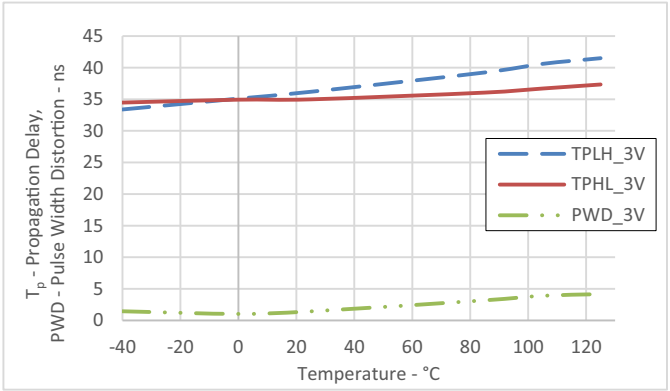


Figure 8: Typical Switching Speed vs. Forward Current at 5V

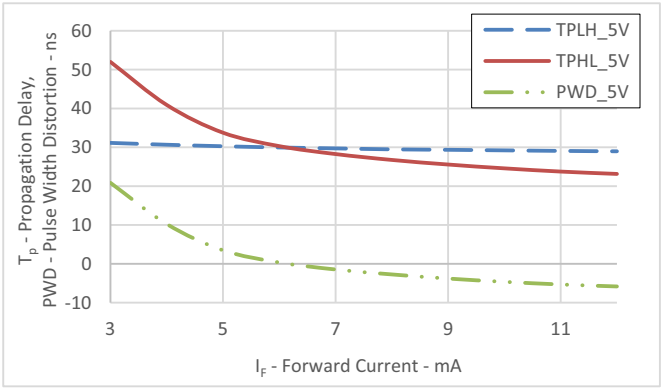
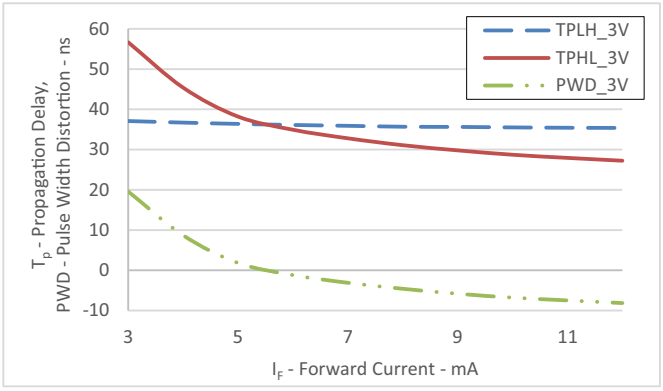
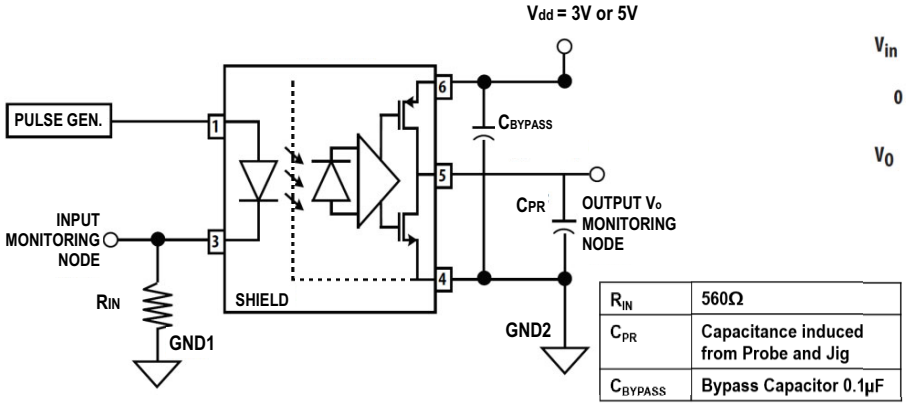


Figure 9: Typical Switching Speed vs. Forward Current at 3V



Test Circuit Diagrams

Figure 10: Switching Speed Test Circuit and Typical Waveform



R_{IN}	560Ω
C_{PR}	Capacitance induced from Probe and Jig
C_{BYPASS}	Bypass Capacitor 0.1µF

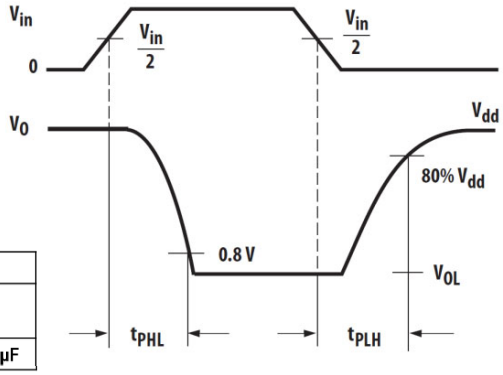
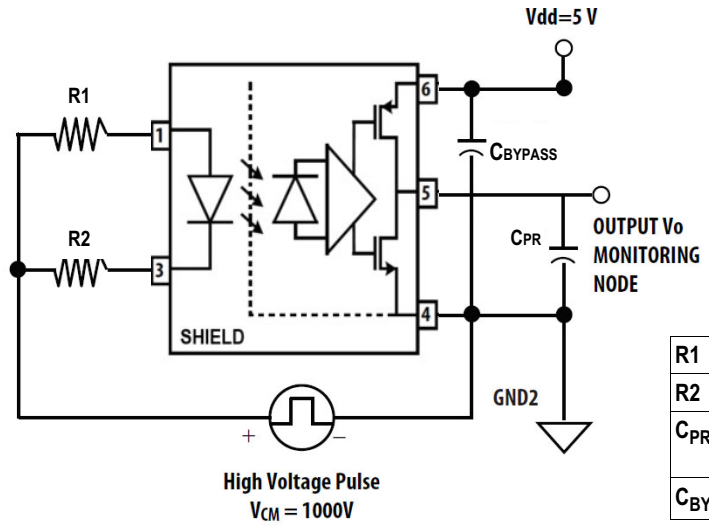
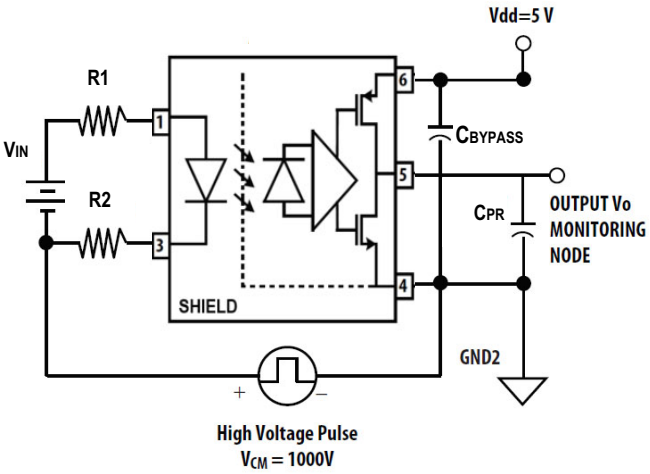


Figure 11: CMR Test Circuit (for CM_H)



R1	390Ω
R2	180Ω
C_{PR}	Capacitance induced from Probe and Jig
C_{BYPASS}	Bypass Capacitor 0.1 µF

Figure 12: CMR Test Circuit (for CM_L)



Vin	5.0V
R1	390Ω
R2	180Ω
C_{PR}	Capacitance induced from Probe and Jig
C_{BYPASS}	Bypass Capacitor 0.1 µF