CSU800 Series

800 Watts
Distributed Power System

Total Power: 800 Watts
Input Voltage: 90-264 Vac
164-320 Vdc
# of Outputs: Main and Standby

Special Features

- 800W output power
- High power and short form factor
- 1U power supply
- High density design: 25 W/in^3
- Active Power Factor Correction
- EN61000-3-2 Harmonic compliance
- Inrush current control
- 80 Plus® Platinum efficiency
- N+M redundant N+M ≤ 4
- Hot-pluggable
- Active current sharing
- Full digital control
- PMBus™ compliant
- Accurate input power reporting
- EN61000-4-5 surge level 2kV/4kV DM/CM
- Compatible with Artesyn's Universal PMBus GUI
- Reverse airflow option
- Conducted/Radiated EMI Class A
- EN61000-4-11

Safety

- UL/cUL
- UL +CB report
- CE Mark
- CCC
- BSMI
- KC
- TUV

Product Descriptions

The CSU800 series power supply features a very wide 90 to 264 Vac and 164 to 320 Vdc input voltage range and employs active power factor correction to minimize input harmonic current distortion and to ensure compliance with the international EN61000-3-2 standard – they have a power factor of 0.99 at full load.

The power supply employs a ultra high efficiency conversion topology, together with an innovative power transformer and rectifier construction that further improves power density and reduces interconnect power losses. Users have a choice of standard I^{2}C or advanced PMBus™ communications. The control software runs under Windows on any standard PC, and uses a highly intuitive graphical user interface to simplify power supply set-up.

The CSU800 series can deliver up to 66.7 A from its main 12 Vdc payload output, and up to 3 A from its 12 Vdc auxiliary output. The form factor is 1U and may be used in single or in redundant configurations.

CSU800 series has a power density of more than 25 Watts per cubic inch, and compliant with 80plus Platinum Efficiency, its efficiency is 94% at nominal high AC line with 50% full load.

ARTESYN™
An Advanced Energy Company

Model Numbers

Standard	Output Voltage	Minimum Load	Maximum Load	Stand-By Supply	Air Flow Direction
CSU800AP-3	12Vdc	1A	66.7A	12Vdc@3A	Normal (DC Connector to Handle)
CSU800AP-3-001	12Vdc	1A	66.7A	12Vdc@3A	Reversed (Handle to DC Connector)

Options

None

Electrical Specifications

Absolute Maximum Ratings

Stress in excess of those listed in the "Absolute Maximum Ratings" may cause permanent damage to the power supply. These are stress ratings only and functional operation of the unit is not implied at these or any other conditions above those given in the operational sections of this TRN. Exposure to any absolute maximum rated condition for extended periods may adversely affect the power supply's reliability.

Table 1. Absolute Maximum Ratings:

Parameter	Model	Symbol	Min	Typ	Max	Unit
Input Voltage						
AC continuous operation	All models	$V_{IN,AC}$	90	-	264	Vac
DC continuous operation	All models	$V_{IN,DC}$	164	-	320	Vdc
Maximum Output Power	All models	$P_{O,max}$	-	-	800	W
Isolation Voltage						
Input to outputs	All models		-	-	4242	Vdc
Ambient Operating Temperature[1]	All models	T_A	0	-	+55	^{O}C
Storage Temperature	All models	T_{STG}	-40	-	+70	^{O}C
Humidity (non-condensing)						
Operating	All models		5	-	85	%
Non-operating	All models		5	-	95	%
Altitude						
Operating	All models		-	-	5,000	m
Non-operating	All models		-	-	15,200	m

Note 1 - The maximum operating temperature (55 ^{O}C) is to be derated by 1 ^{O}C per 300m above 2000m .

Input Specifications

Table 2. Input Specifications:

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage, AC		$V_{IN,AC}$	90	115/230	264	Vac
Operating Input Voltage, DC		$V_{IN,DC}$	164	-	320	Vdc
Input AC Frequency		$f_{IN,AC}$	47	50/60	63	Hz
Maximum Input Current ($I_O = I_{O,max}$, $I_{SB} = I_{SB,max}$)	$V_{IN,AC}$ = 90Vac	$I_{IN,max}$	-	-	11.7	A
No Load Input Power (V_O =On, I_O = 0A, I_{SB} = 0A)	All	$P_{IN,no-load}$	-	-	5	W
Harmonic Line Currents	All	THD	Per EN 61000-3-2			
Power Factor	$I_O > 10\%I_{O,max}$	PF	0.90	-	-	
Startup Surge Current (Inrush) @ 25°C	$V_{IN,AC}$ = 264Vac	$I_{IN,surge}$	-	-	35	Apk
Input Fuse	Internal, L 5x20mm, Quick Acting 12.5A, 400Vdc		-	-	12.5	A
Leakage Current to earth ground	$V_{IN,AC}$ = 264Vac $f_{IN,AC}$ = 50Hz		-	-	1.75	mA
Operating Efficiency @ 25°C	$V_{IN,AC}$ = 230Vac $f_{IN,AC}$ = 50Hz $I_O = 10\%I_{O,max}$ $I_O = 20\%I_{O,max}$ $I_O = 50\%I_{O,max}$ $I_O = 100\%I_{O,max}$	η	 88 91 94 91	 - - - -	 - - - -	 % % % %
System Stability Phase Margin Gain Margin			 45 -10	 - -	 - -	 Ø dB

Output Specifications

Table 3. Output Specifications:

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Factory Set Voltage	All	V_O	11.9	12.0	12.1	Vdc
		V_{SB}	11.9	12.0	12.1	
Output Regulation	Inclusive of set-point, temperature change, warm-up drift and dynamic load	V_O	11.4	12.0	12.6	Vdc
		V_{SB}	11.4	12.0	12.6	
Output Ripple, pk-pk	Measure with a 0.1µF ceramic capacitor in parallel with a 10µF tantalum capacitor, 0 to 20MHz bandwidth	V_O	-	-	120	mV_{PK-PK}
		V_{SB}	-	-	120	
Output Current	All	I_O	1	-	66.7	A
	All	I_{SB}	1	-	3	
V_O Current Share Accuracy	50% to 100% I_O 20% to 50% I_O		- -	- -	5 10	$\%I_O$
Number of Parallel Units[1]	Main Output “12V load share” connected		-	-	4	
Load Capacitance	Start up	V_O	500	-	25000	uF
		V_{SB}	100		3100	uF
V_O Dynamic Response[2] Peak Deviation	60% load change, slew rate = 0.5A/µs	V_O	11.4	-	12.6	V
	1A load change slew rate = 0.5A/µs	V_{SB}	11.4	-	12.6	V

Note 1 - V_{SB} output do not use active current sharing. On paralleled units, maximum current on V_{SB} output rail should not exceed the current of one unit.

Note 2 - Recommend to test with 2000uF capacitive load at the Vo output and 20uF at V_{SB} output. For the dynamic the Min load should be 1A for +12V Main output.

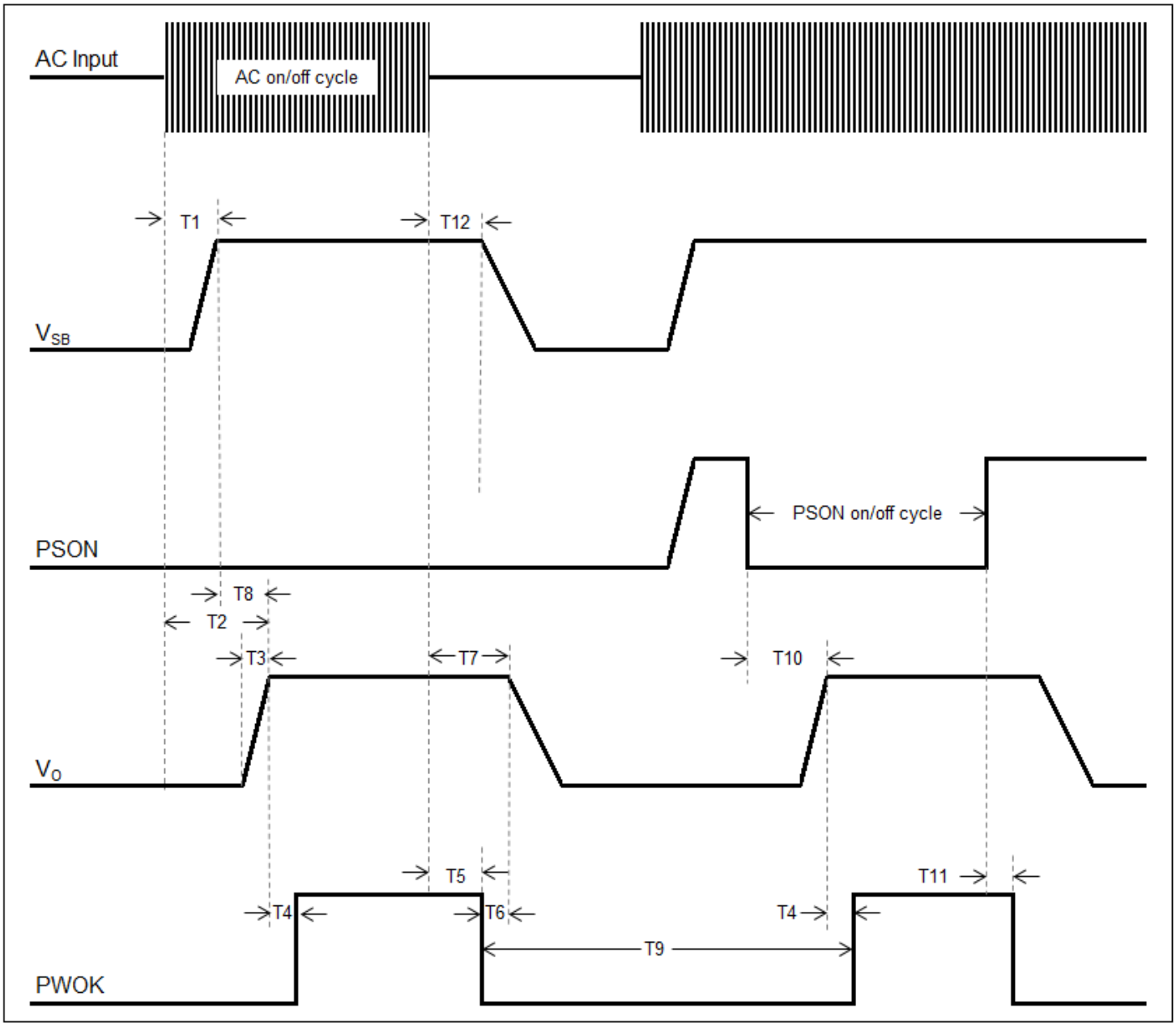
System Timing Specifications

Table 4. System Timing Specifications:

Label	Parameter	Min	Typ	Max	Unit
T1	Delay from AC being applied to V_{SB} being within regulation	-	-	1500	mSec
T2	Delay from AC being applied to all output voltages being within regulation with PSON asserted low.	-	-	3000	mSec
T3	V_O rise time, 0V to V_O in regulation.	5	-	70	mSec
T4	Delay from output voltages within regulation limits to PWOK asserted high at turn on.	100	-	500	mSec
T5	Delay from loss of AC to de-assertion of PWOK.	12	-	-	mSec
T6	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1	-	-	mSec
T7	Hold up time - time output voltages stay within regulation after loss of AC.	13	-	-	mSec
T8	Delay from standby voltage in regulation to output voltage in regulation at AC turn on.	50	-	1000	mSec
T9	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal	100	-	-	mSec
T10	Delay from PSON active to output voltages within regulation limits.	5	-	400	mSec
T11	Delay from PSON deactive to PWOK de-asserted low.	-	-	5	mSec
T12	Hold up time - time standby voltages stay within regulation after loss of AC.	70	-	-	mSec

System Timing Specifications

System Timing Diagram:



CSU800AP-3 Performance Curves

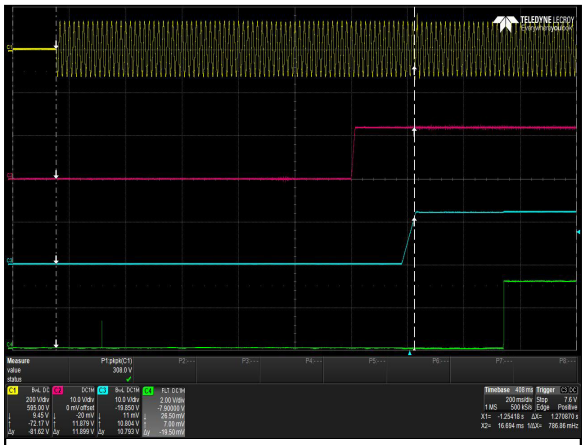


Figure 1: CSU800AP-3 Turn-on delay via AC Mains – Vin = 90Vac
Full Load: Io = 66.7A, I_{SB} = 3A
Ch 1: AC Mains Ch 2: V_{SB} Ch 3: Vo Ch 4: PWOK

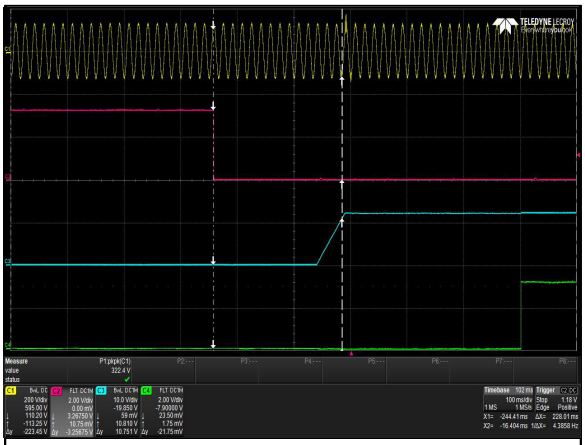


Figure 2: CSU800AP-3 Turn-on delay via PSON – Vin = 90Vac
Full Load: Io = 66.7A, I_{SB} = 3A
Ch 1: AC Mains Ch 2: PSON Ch 3: Vo Ch 4: PWOK

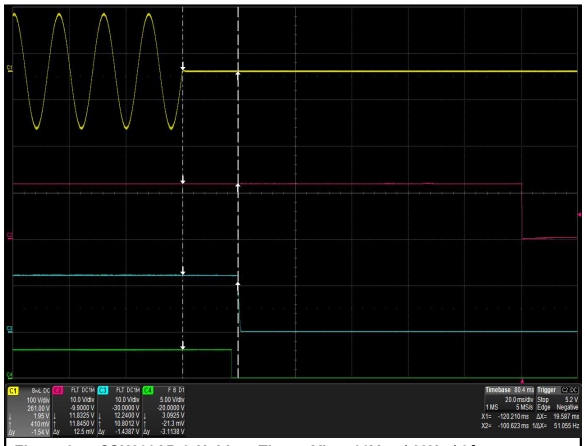


Figure 3: CSU800AP-3 Hold-up Time – Vin = 90Vac / 63Hz / 0°
Full Load: Io = 66.7A, I_{SB} = 3A
Ch 1: AC Mains Ch 2: V_{SB} Ch 3: Vo Ch 4: PWOK

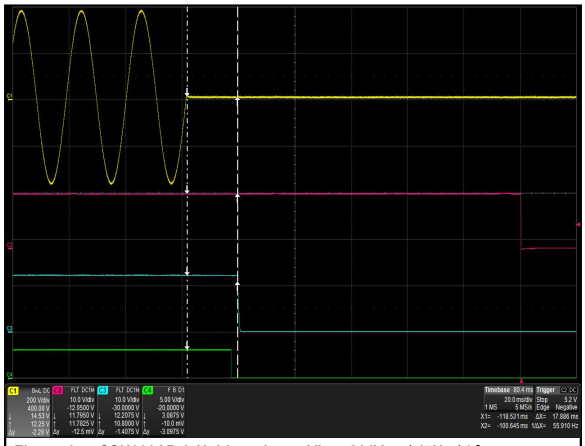


Figure 4: CSU800AP-3 Hold-up time – Vin = 264Vac / 47Hz / 0°
Full Load: Io = 66.7A, I_{SB} = 3A
Ch 1: AC Mains Ch 2: V_{SB} Ch 3: Vo Ch 4: PWOK

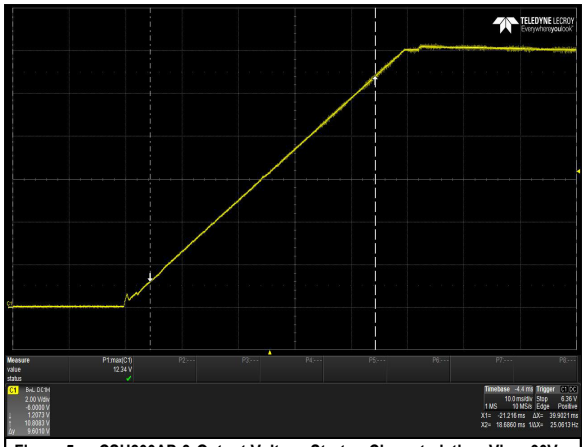


Figure 5: CSU800AP-3 Output Voltage Startup Characteristic – Vin = 90Vac
Full Load: Io = 66.7A, I_{SB} = 3A
Ch 1: Vo

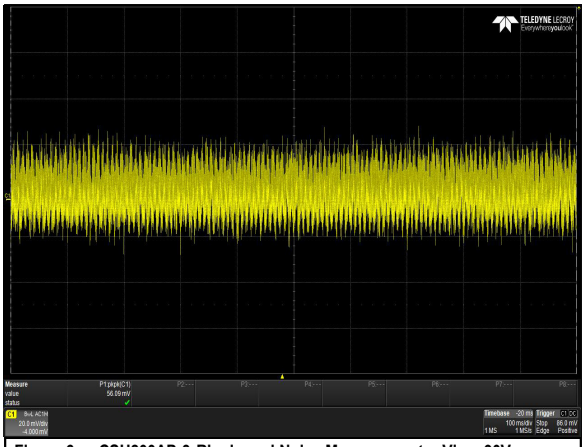


Figure 6: CSU800AP-3 Ripple and Noise Measurement – Vin = 90Vac
Full Load: Io = 66.7A, I_{SB} = 3A
Ch 1: Vo

CSU800AP-3 Performance Curves

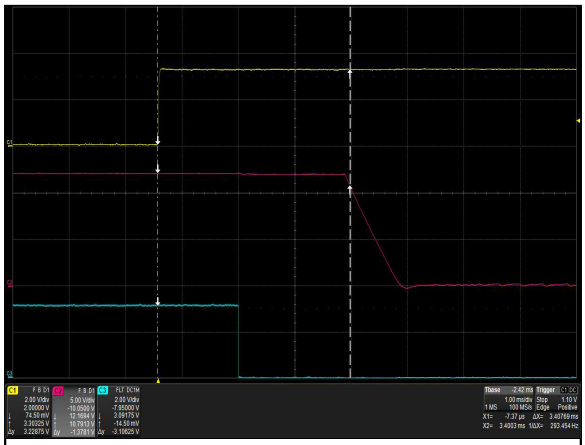


Figure 7: CSU800AP-3 Turn Off Characteristic via PSON
Full Load: Io = 66.7A, I_{SB} = 3A
Ch 1: PSON Ch 2: Vo Ch 3: PWOK

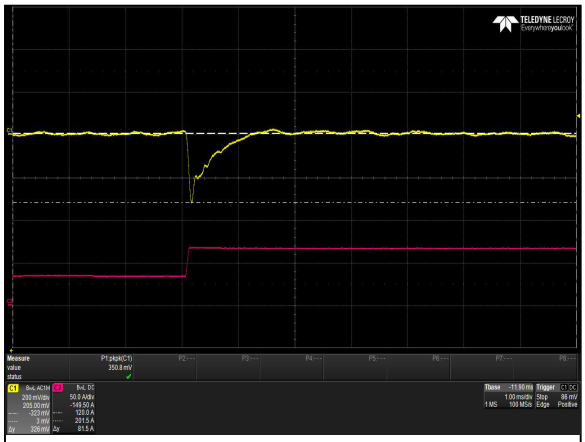


Figure 8: CSU800AP-3 Transient Response – Vo Deviation (low to high)
50% to 100% load change, 0.5A/µS slew rate, Vin = 230Vac
Ch 1: Vo Ch 2: Io

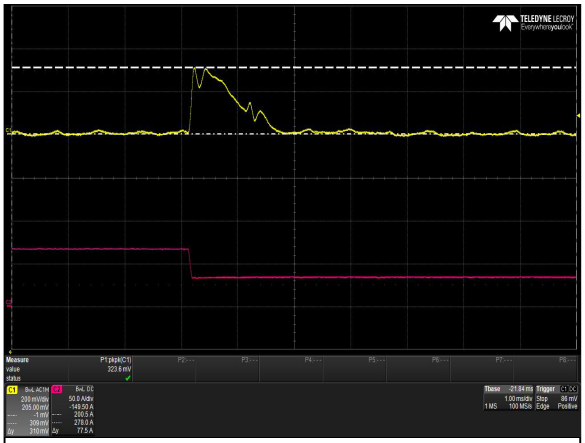


Figure 9: CSU800AP-3 Transient Response – Vo Deviation (high to low)
100% to 50% load change, 0.5A/µS slew rate, Vin = 230Vac
Ch 1: Vo Ch 2: Io

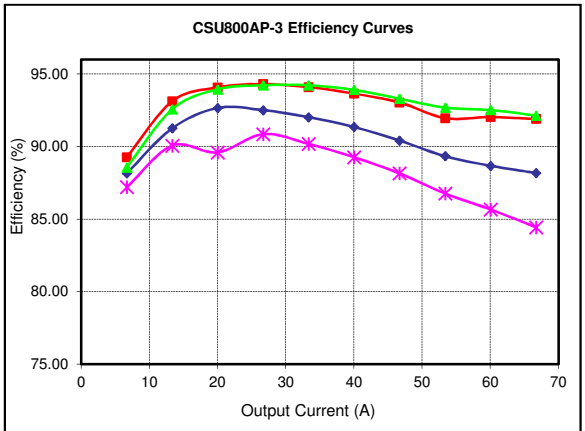


Figure 10: CSU800AP-3 Efficiency Curves @ 25 °C
90 Vac 115 Vac 230 Vac 264 Vac
Loading: Io_main = 10%$I_{o,max}$ increment to 66.7A, I_{SB} = 3A (12V)

Protection Function Specification

Input Fusing

CSU800 series is equipped with an internal non user serviceable 12.5A High Rupturing Capacity (HRC) 400Vdc fuse to IEC 127 for fault protection on L lines input.

Over Voltage Protection (OVP)

The power supply over voltage protection will be locally sensed. The power supply will shutdown and latch off after an over voltage condition occurs. This latch will be cleared by toggling the PSON signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage will never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage will never trip any lower than the minimum levels when measured at the power connector. +12V V_{SB} will be auto-recovered after removing OVP limit.

Parameter	Min	Nom	Max	Unit
V_O Output Overvoltage	13.3	/	14.5	V
V_{SB} Output Overvoltage	13.3	/	14.5	V

Over Temperature Protection (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shutdown. When the power supply temperature drops to within specified limits, the power supply will restore power automatically, while the +12V V_{SB} remains always on. The OTP circuit have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip level have a minimum of $4^{O}C$ of ambient temperature margin.

Over Current Protection (OCP)

The power supply have current limit to prevent the outputs from exceeding the values shown in table below. If the current limits are exceeded, the power supply will shutdown and latch off. The latch will be cleared by toggling the PSON signal or by an AC power interruption. The power supply will not be damaged from repeated power cycling in this condition. +12V V_{SB} will be auto recovered after removing OCP limit.

Parameter	Min	Nom	Max	Unit
V_O Output Over current	73.37	/	93.38	A
V_{SB} Output Over current	4.0	/	5.0	A

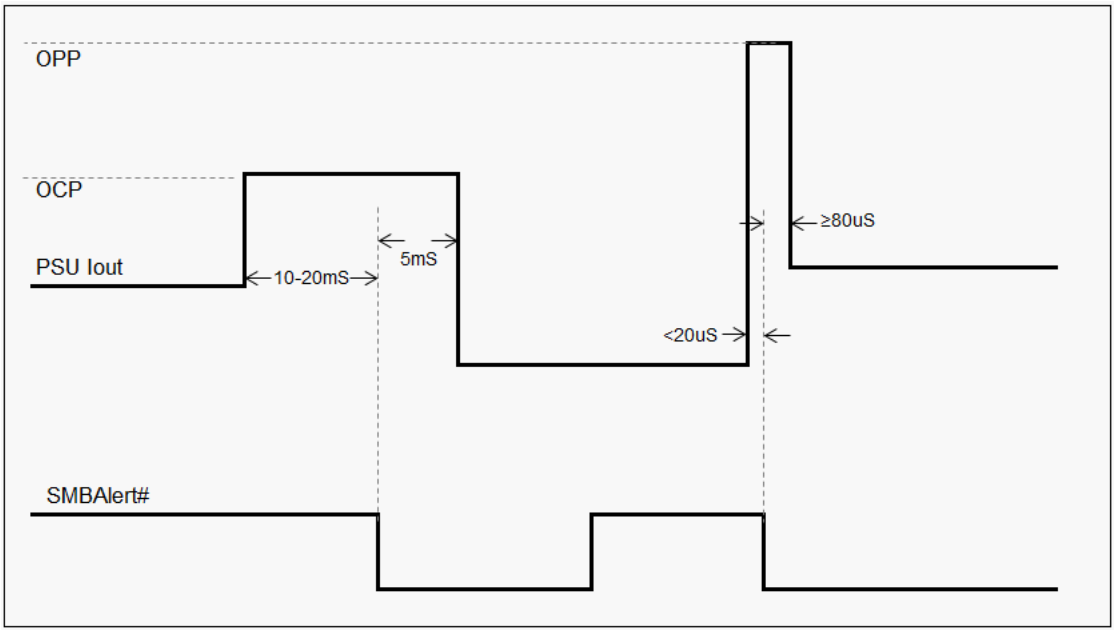
The over current protection for the main output is divided to three stages.

The first stage is Over Current Warning (OCW). When the output current is within this range and lasts for longer than 20Sec, the SMB Alert will assert within the 20 to 20.1Sec and the power supply will shutdown after the assertion of SMB_ALERT for longer than 1Sec.

The second stage is Over Current Protection (OCP). When the output current is within this range, the SMB Alert will assert within the 10 to 20mSec and the power supply will shutdown after the assertion of SMB_ALERT for longer than 5mSec.

The third stage is Over Power Protection (OPP). When the output current is within this range, the SMB Alert will assert in 20µSec and the power supply will shutdown after the assertion of SMB_ALERT for longer than 80µSec.

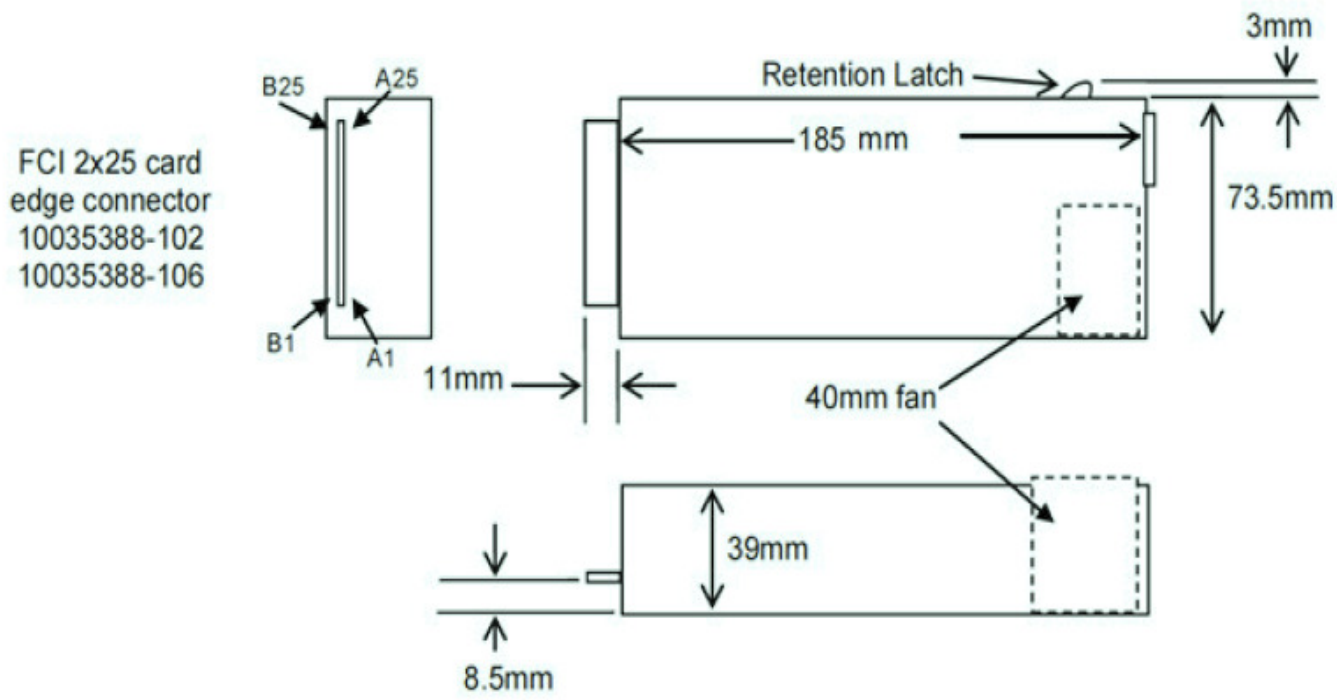
+12V Protection	Min	Nom	Max	SMB Alert	Fault Delay Time
OCW	110%$I_{O,max}$	115%$I_{O,max}$	120%$I_{O,max}$	20.0 - 20.1Sec	≥1Sec
OCP	120%$I_{O,max}$	130%$I_{O,max}$	140%$I_{O,max}$	10 - 20mSec	≥5mSec
OPP	140%$I_{O,max}$	150%$I_{O,max}$	160%$I_{O,max}$	<20µSec	≥80µSec



Mechanical Specifications

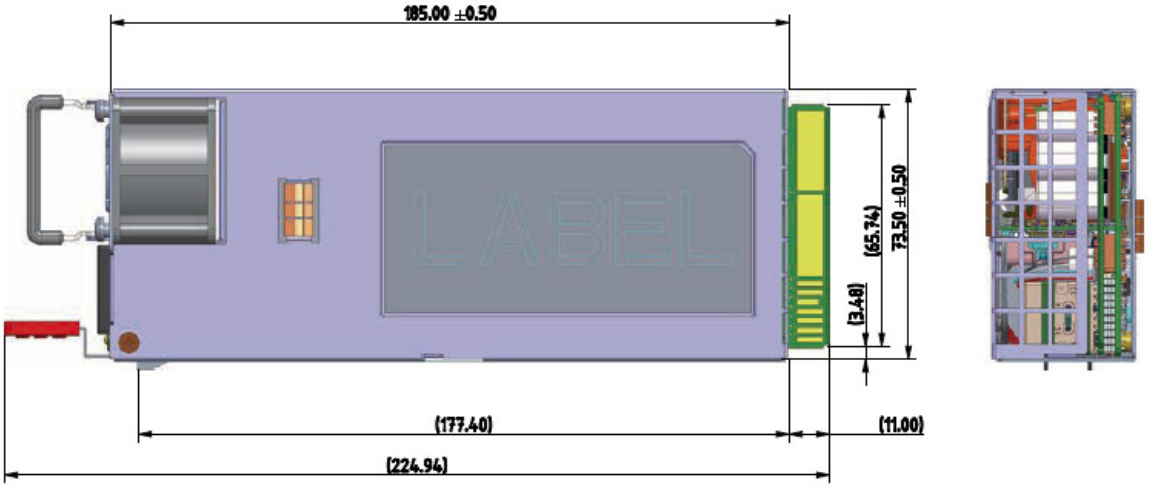
Mechanical Outlines (Unit:mm)

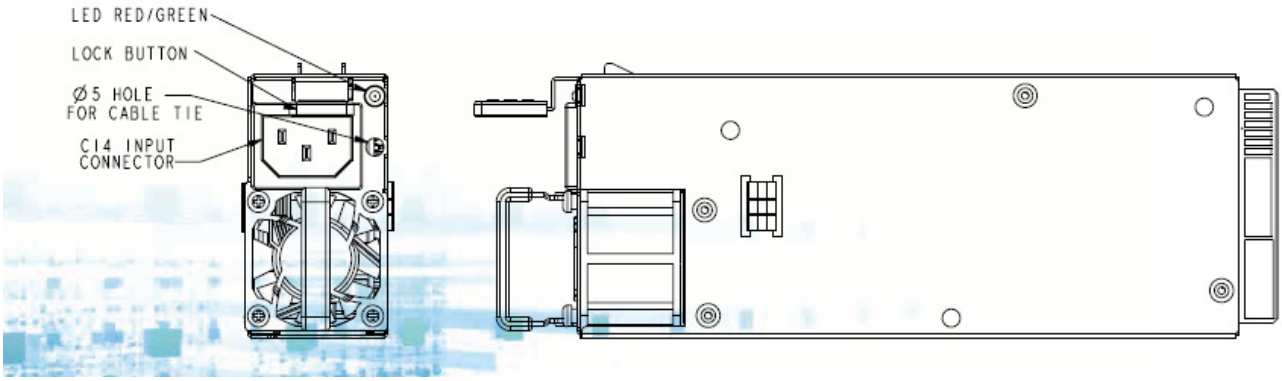
The physical size of the power supply enclosure is 39/40mm x 73.5mm x 185mm.
The power supply contains a single 40mm fan with normal airflow direction or reversed airflow direction.
The power supply has an identical card edge output that interfaces with a 2x25 card edge connector in the system.
The AC plugs directly into the external face of the power supply.
Refer to the following figure. All dimensions are nominal.



Mechanical Specifications

Detailed Mechanical (Unit: mm)





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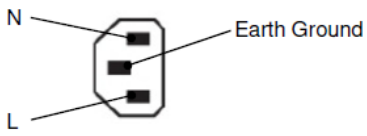
Connector Definitions

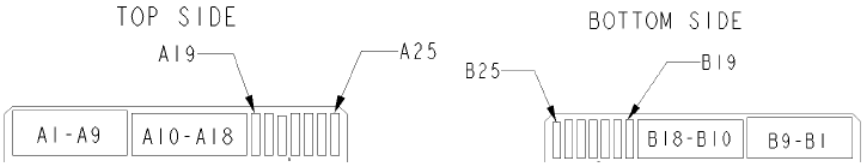
AC Input Connector

Pin 1 – L
Pin 2 – N
Pin 3 – Earth Ground



Output Connector – Power Blades

A1-A9 – Main Output Return
A10-A18 – + Main Output (V_O)
B1-B9 – Main Output Return
B10-B18 – + Main Output (V_O)



View from power supply output connector end

Output Connector – Control Signals

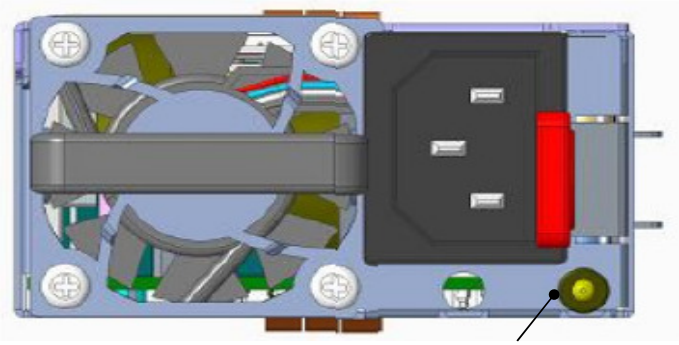
A19 – SDA
A20 – SCL
A21 – PSON
A22 – SMBAlert#
A23 – -VSENSE
A24 – +VSENSE
A25 – PWOK
B19 – A0 (SMBus address)
B20 – A1 (SMBus address)
B21 – $12V_{SB}$
B22 – CR_BUS#
B23 – 12V load share
B24 – Present
B25 – Reserved

Power / Signal Mating Connectors and Pin Types

Table 5. Mating Connectors for CSU800 series:

Reference	On Power Supply	Mating Connector or Equivalent
AC Input Connector	IEC320-C14	IEC320-C13
Output Connector	Card-edge	2x25 pin configuration of the FCI power card connector 10035388-102LF

LED indicator Definition



One bi-color (green/amber) LED at the power supply front provides status signal. The status LED conditions is shown on the below table.

Condition	LED Status
Normal work	GREEN
No AC power to all power supplies	OFF
AC present / Only 12 VSB on (PS off) or PS in CR state	1Hz Blinking Green
AC cord unplugged; with a second power supply in parallel still with AC input power	RED
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan, input voltage lower than 90Vac (not warning above 90Vac condition, must be warning state below 85Vac condition)	1 Hz Blinking RED
Power supply critical event causing a shutdown; failure, OCP, OVP, fan fail	RED

Weight

The CSU800 series weight is 864.5g/1.91lbs.

Environmental Specifications

EMC Immunity

CSU800 series power supply is designed to meet the following EMC immunity specifications

Table 6. Environmental Specifications:

Document	Description
Class A of CISPR32 (EN55032) and FCC Part 15	Conducted and Radiated EMI Limits
IEC/EN 61000-3-2 Class A	Harmonics
IEC/EN 61000-3-3	Voltage Fluctuations
IEC/EN 61000-4-2	Electromagnetic Compatibility (EMC) - Testing and measurement techniques – Electrostatic discharge immunity test. +/-15KV air, +/-8KV contact discharge, performance Criteria A
IEC/EN 61000-4-3: 2010	Electromagnetic Compatibility (EMC) - Testing and measurement techniques, Radiated, radio-frequency, electromagnetic field immunity test performance criterion: A
IEC/EN 61000-4-4: 2010	Electromagnetic Compatibility (EMC) - Testing and measurement techniques, Electrical Fast Transient/Burst Immunity Test. 2KV for AC power port, performance Criteria A
IEC/EN 61000-4-5: 2010	Electromagnetic Compatibility (EMC) - Testing and measurement techniques – Surge Test. 4KV common mode and 2KV differential mode for AC ports, performance criteria A.
EN55024	Electromagnetic Compatibility (EMC) - Testing and measurement techniques : Voltage Dips and Interruptions: Criteria B: >95% reduction for 10ms; Criteria C: 30% reduction for 500mS, or >95% reduction for 5000mS, Criteria C
EN55032: 2011	Information Technology Equipment-Immunity Characteristics, Limits and Method of Measurements

Safety Certifications

The CSU800 series power supply is intended for inclusion in other equipment and the installer must ensure that it is in compliance with all the requirements of the end application. This product is only for inclusion by professional installers within other equipment and must not be operated as a stand alone product.

Table 7. Safety Certifications for CSU800 series power supply system:

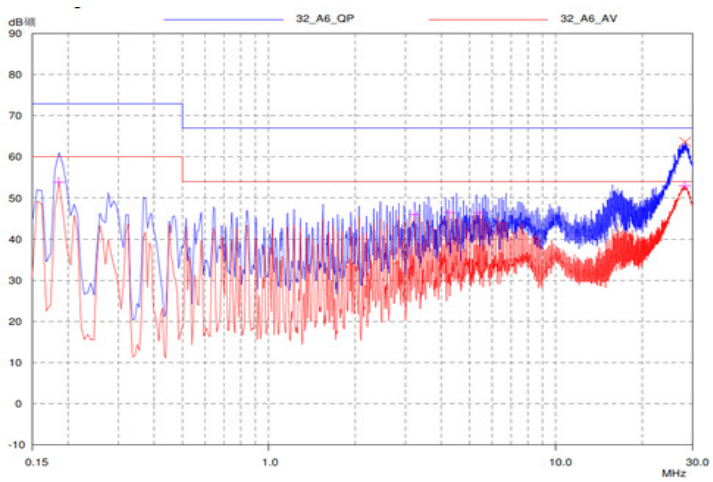
Document	File #	Description
UL 62368-1, CAN/CSA C22.2 No. 62368-1		US and Canada Requirements
EN 62368-1	B 013890 3158 Rev. 00	European Requirements
CB Certificate and Report	SG PSB-IV-01139	(All CENELEC Countries)
CHINA CCC Approval	2017010907942615	China Requirements

EMI Emissions

The CSU800 series has been designed to comply with the Class A limits of EMI requirements of FCC Part 15 and CISPR 32 (EN55032) for emissions and relevant sections of EN55032: 2011 for immunity. The unit is enclosed inside a metal box, tested at 800W using resistive load with cooling fan.

Conducted Emissions

The applicable standard for conducted emissions is EN55032 (FCC Part 15). Conducted noise can appear as both differential mode and common mode noise currents. Differential mode noise is measured between the two input lines, with the major components occurring at the supply fundamental switching frequency and its harmonics. Common mode noise, a contributor to both radiated emissions and input conducted emissions, is measured between the input lines and system ground and can be broadband in nature.



The CSU800 series power supplies have internal EMI filters to ensure the convertors' conducted EMI levels comply with EN55032 (FCC Part 15) Class A limits. The EMI measurements are performed with resistive loads at maximum rated loading.

Sample of EN55032 Conducted EMI Measurement at 110Vac input

Note: Blue Line refers to Artesyn Quasi Peak margin, which is 6dB below the CISPR international limit. Red Line refers to the Artesyn Average margin, which is 6dB below the CISPR international limit.

Conducted EMI emission specifications of the CSU800 series

Parameter	Model	Symbol	Min	Typ	Max	Unit
FCC Part 15, class A	All	Margin	-	-	6	dB
CISPR 32 (EN55032) class A	All	Margin	-	-	6	dB

Radiated Emissions

Unlike conducted EMI, radiated EMI performance in a system environment may differ drastically from that in a stand-alone power supply. The shielding effect provided by the system enclosure may bring the EMI level from Class A to Class B. It is thus recommended that radiated EMI be evaluated in a system environment. The applicable standard is EN55032 Class A (FCC Part 15). Testing ac-dc convertors as a stand-alone component to the exact requirements of EN55032 can be difficult, because the standard calls for 1m leads to be attached to the input and outputs and aligned such as to maximize the disturbance. In such a set-up, it is possible to form a perfect dipole antenna that very few ac-dc convertors could pass. However, the standard also states that an attempt should be made to maximize the disturbance consistent with the typical application by varying the configuration of the test sample.

Operating Temperature

The CSU800 series power supplies will start and operate within stated specifications at an ambient temperature from 0 ^{O}C to 55 ^{O}C. The maximum operating temperature (55 ^{O}C) is to be de-rated by 1 ^{O}C per 300m above 2000m.

Forced Air Cooling

The CSU800 series power supplies included internal cooling fans as part of the power supply assembly to provide forced air-cooling to maintain and control temperature of devices and ambient temperature in the power supply to appropriate levels. The standard direction of airflow is from the DC connector end to the AC connector end of the power supply.

Storage and Shipping Temperature / Humidity

The CSU800 series power supplies can be stored or shipped at temperatures between –40 ^{O}C to +70 ^{O}C and relative humidity from 5% to 95% non-condensing.

Altitude

The CSU800 series will operate within specifications at altitudes up to 5,000 meters above sea level. The power supply will not be damaged when stored at altitudes of up to 15,200 meters above sea level.

Humidity

The CSU800 series will operate within specifications when subjected to a relative humidity from 5% to 85% non-condensing. The CSU800 series can be stored in a relative humidity from 5% to 95% non-condensing.

Vibration

The CSU800 power supply will pass the following vibration specifications:

Non-Operating Random Vibration

Acceleration	1.87		gRMS
Frequency Range	10-500		Hz
Duration	30		mins
Direction	3 mutually perpendicular axis		
PSD Profile	**FREQ**	**SLOPE dB/oct**	**PSD g^2/Hz**
	10-200 Hz	---	0.01 g^2/Hz
	500 Hz	---	0.003 g^2/Hz

Operating Random Vibration

Acceleration	0.15		gRMS
Frequency Range	5-100		Hz
Duration	30		mins
Direction	3 mutually perpendicular axis		
PSD Profile	**FREQ**	**SLOPE dB/oct**	**PSD g^2/Hz**
	5 Hz	---	0.000025 g^2/Hz
	10-50 Hz	---	0.0004 g^2/Hz
	100 Hz	---	0.000025 g^2/Hz

Shock

The CSU800 series power supply will pass the following vibration specifications:

Non-Operating Half-Sine Shock

Acceleration	30	G
Duration	11	msec
Pulse	Half-Sine	
No. of Shock	3 shock on each of 6 faces	

Operating Half-Sine Shock

Acceleration	4	G
Duration	22	msec
Pulse	Half-Sine	
No. of Shock	3 shock on each of 6 faces	

Power and Control Signal Descriptions

AC Input Connector

This connector supplies the AC Mains to the CSU800 series power supply.

Pin 1 - L
Pin 2 - N
Pin 3 - Earth Ground

Output Connector - Power Blades

These pins provide the main output for the CSU800 series. The + Main Output (V_O) and the Main Output Return pins are the positive and negative rails, respectively, of the V_O main output of the CSU800 series power supply. The Main Output (V_O) is electrically isolated from the power supply chassis.

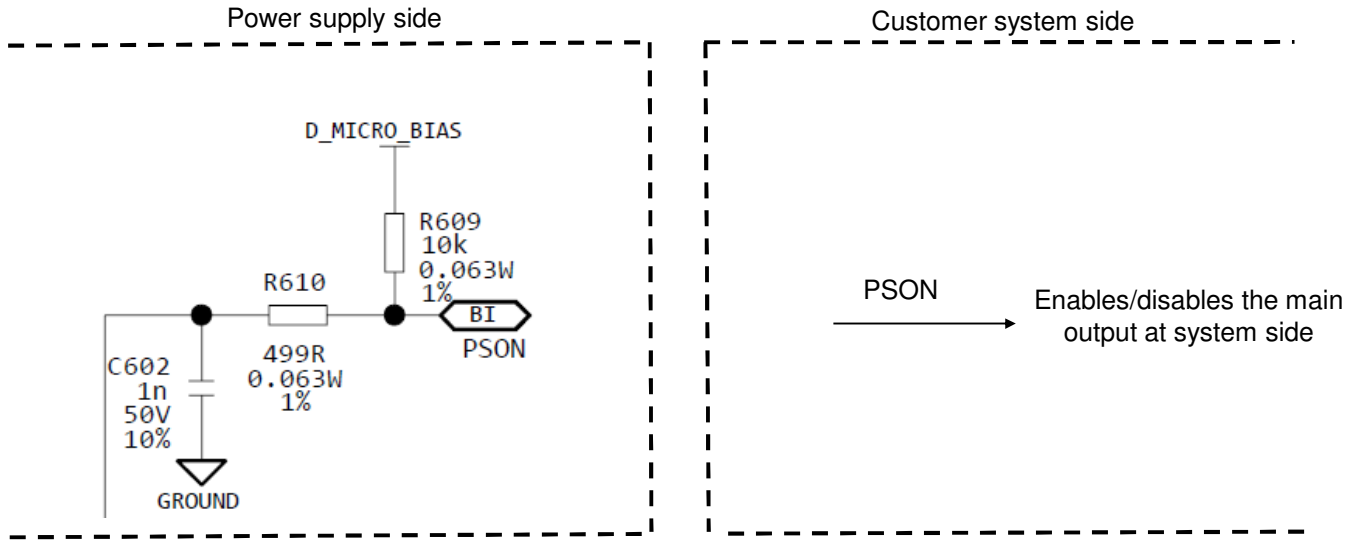
A1-A9	-	Main Output Return
A10-A18	-	+ Main Output (V_O)
B1-B9	-	Main Output Return
B10-B18	-	+ Main Output (V_O)

Output Connector - Control Signals

The CSU800 series contains a 14 pins control signal header providing an analogue control interface, standby power and I^2C interface signal connections.

PSON – (Pins A21)

This signal input pin controls the normal turn ON and Off of the Main Output of the CSU800 series power supply. The power supply main output (V_O) will be enabled when this signal is pulled low below 1.0V. The Power supply output (except V_{SB} output) will be disabled when this input is driven higher than 2.0V, or left open circuited. The source current is 4mA maximum when Vpson is low.



SMBALERT# – (Pin A22)

This signal indicates that the power supply is experiencing a problem that the user should investigate. The signal will activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits. The signal will be asserted low below 0.4V due to Critical events or Warning events, and will asserted high above 2.4V when the power supply is status is normal. The sink current is 4mA maximum when the signal is low and is 50uA maximum when the signal is high. The rise time and fall time of the signal is 100uS maximum. This signal is also to be asserted in parallel with LED turning solid Red or blink Red.

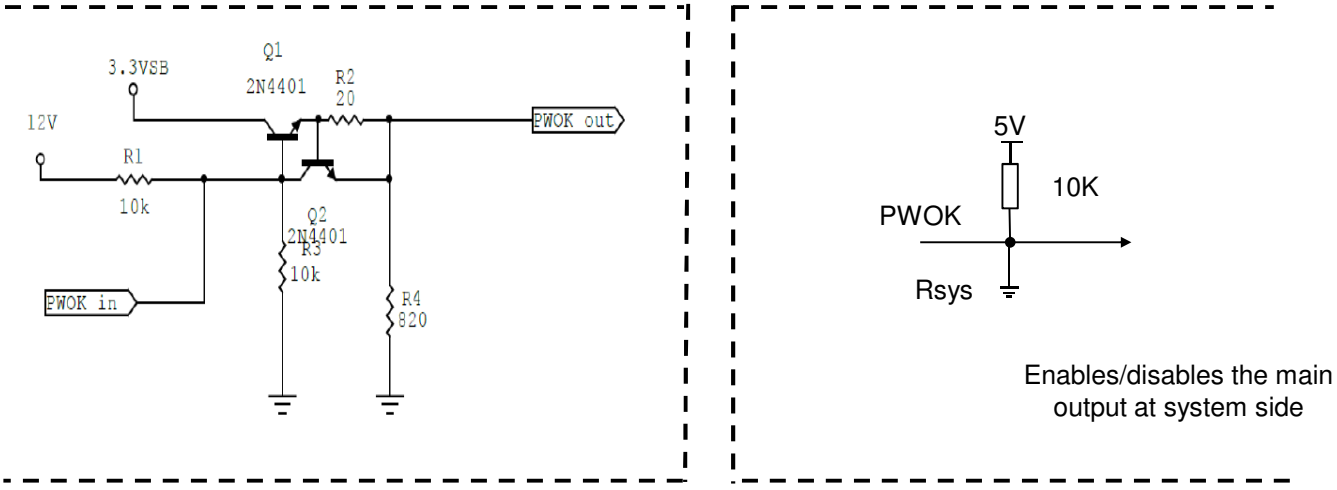
+ VSENSE & -VSENSE – (Pin A23, A24)

+ VSENSE and –VSENSE are the remote sense signals for 12V main output voltage.

PWOK – (Pin A25)

The PWOK is an output signal driven high above 2.4V by the power supply to indicate that all outputs are valid. If any of the power supply outputs fails below its regulation limits, this signal will be driven low below 0.4V. The sink current is 4mA maximum when the signal is low and is 2mA maximum when the signal is high. The rise time and fall time of the signal is 100uS maximum. The PWOK delay(Output in regulation to PWOK in regulation) is 100ms minimum, 500ms maximum. The power down delay(PWOK out of regulation to output out of regulation) is 1ms minimum, 200ms maximum.

A recommended implementation of the PWOK circuits is shown below.
Note: the PWOK circuits should be compatible with 5V pull up resistor (>10k) and 3.3V pull up resistor (>6.8k)



CR_BUS# – (Pin B22)

There is an additional signal defined supporting Cold Redundancy. This is connected to a bus shared between the power supplies: CR_BUS#. This is a tri-state output signal of the power supply used to communicate a fault or Vout under voltage level has occurred in one of the power supplies. This is used to power on all the power supplies in the system via the CR_BUS#. When the signal is pulled high it allows all power supplies in cold standby mode to go into cold standby state when the load share voltage is below the VCR_ON level. When the signal is left open on all power supplies it forces all cold standby power supplies into the ON. The Cold Redundancy section showing the logic state of the CR_BUS# signal depending upon the programmed configuration of the power supply in D0h, the operating state of the power supply, and the power supply fault status.

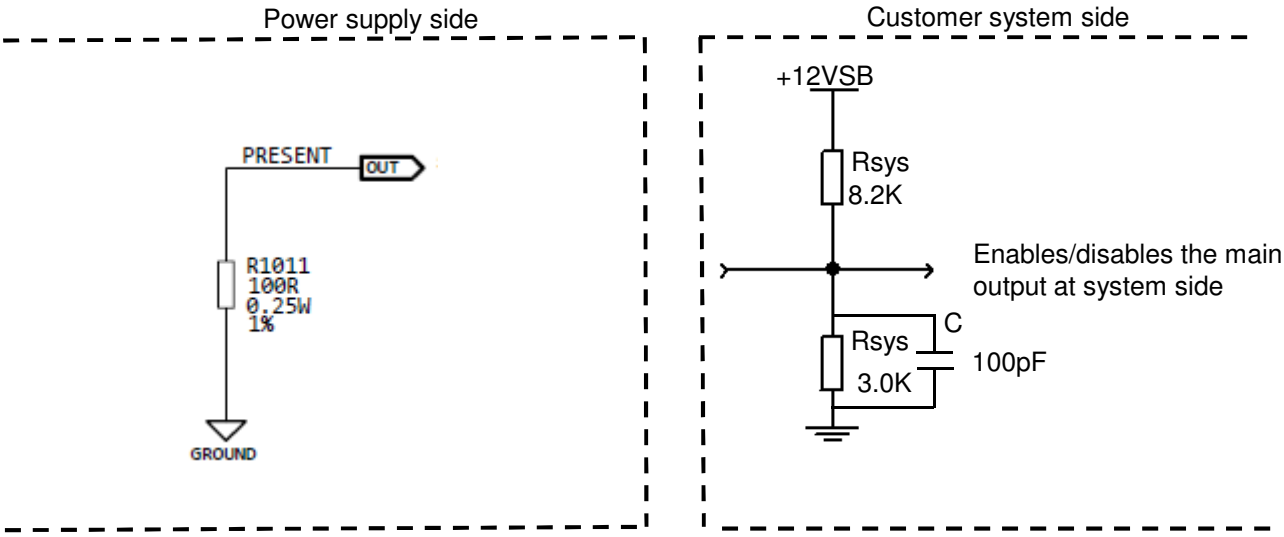
12V load share – (Pin B23)

12V load share is a single wire bus signal used to help equalize the output current from two or more power supplies connected to a common load. 12V load share should be taken that with two or more power supplies sharing current, the percentage is the combined current for all power supplies, not one. The voltage on the 12V load share line represents the percentage of rated output current each supply is providing. 0V is equivalent to 0% load, 4V is equivalent to 50% load, and 8V is equivalent to 100% load. 12V load share transients during hot insertion or removal will not cause the supply output to go out of regulation.

Present # – (Pin B24)

Signal used to indicate to the system that a power supply is inserted in the power bay. This pin is internally pulled down to the standby return in the power supply with a 100 ohms resistor. Recommended pull-up resistor to 12Vsb is 8.2k ohm with a 3.0k ohm pull-down to ground. A 100pF decoupling capacitor is also recommended.

- Low - PS is present
- High - PS is removed from system



Communication Bus Descriptions

I²C Bus Signals

CSU800 series power supply contains enhanced monitor and control functions implemented via the I²C bus. The CSU800 series I²C functionality (PMBus™ and FRU data) can be accessed via the output connector control signals. The communication bus is powered either by the internal 3.3V supply or from an external power source connected to the Standby Output (i.e. accessing an unpowered power supply as long as the Standby Output of another power supply connected in parallel is on).

If units are connected in parallel or in redundant mode, the Standby Outputs must be connected together in the system. Otherwise, the I²C bus will not work properly when a unit is inserted into the system without the DC source connected.

Note: PMBus™ functionality can be accessed only when the PSU is powered-up.
Guaranteed communication I²C speed is 100K Hz.

A0, A1(I²C Address Signals) - (Pins B19, B20)

These input pins are the address lines A0 and A1 to indicate the slot position the power supply occupies in the power bay and define the power supply addresses for FRU data and PMBus™ data communication. This allows the system to assign different addresses for each power supply. During I²C communication between system and power supplies, the system will be the master and power supplies will be slave.

They are internally pulled up to internal 3.3V supply with a 10K resistor.

SDA, SCL (I²C Data and Clock Signals) - (Pins A19, A20)

I²C serial data and clock bus - these pins are internally pulled up to internal 3.3V supply with a 10K ohm resistor. These pins must be pulled-up by a 2K-10K ohm resistor to 3.3V or 5V at the system side.

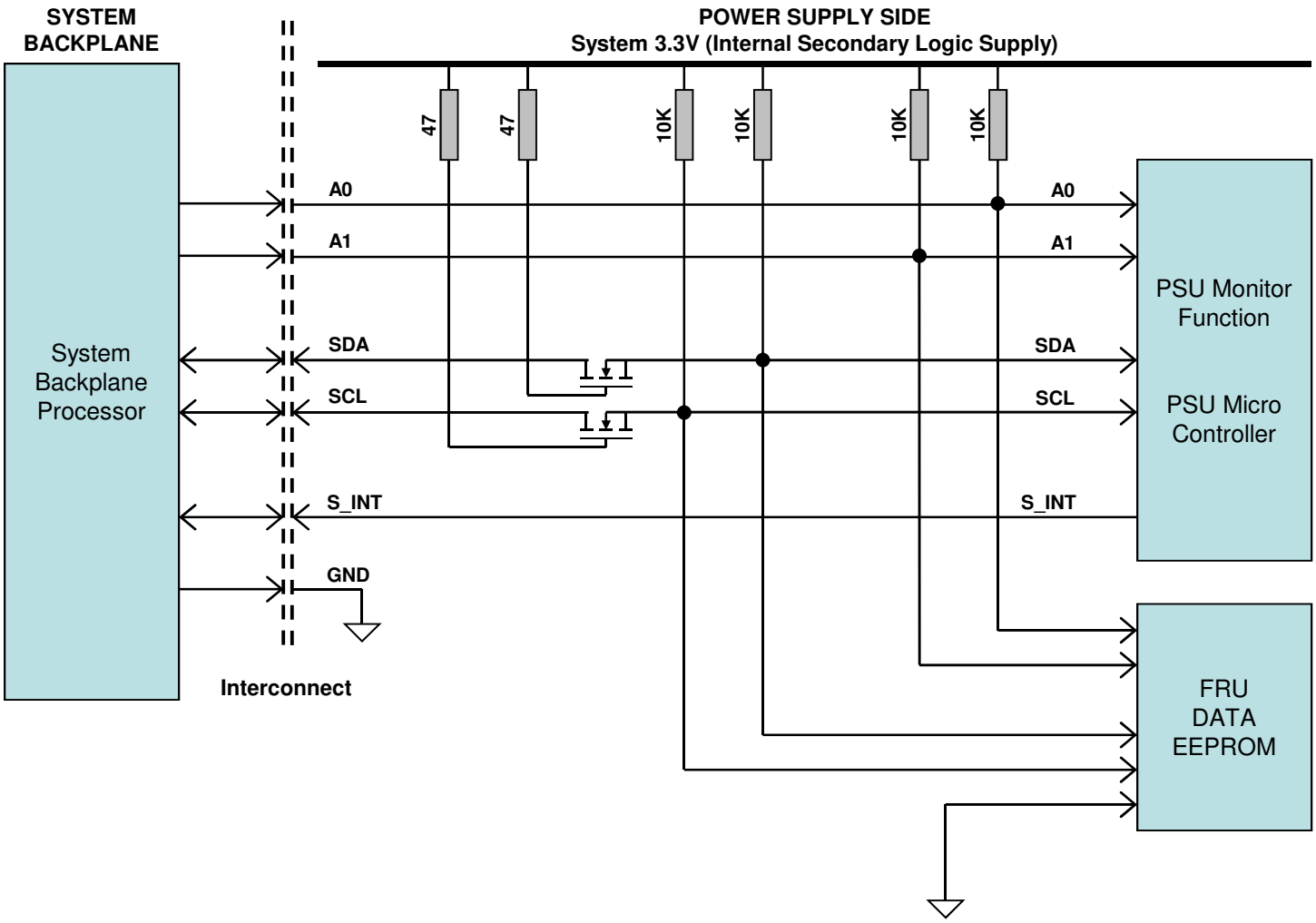
I²C Bus Communication Interval

The interval between two consecutive I²C communications to the power supply should be at least 15ms to ensure proper monitoring functionality.

I²C Bus Signal Integrity

The noise on the I²C bus (SDA, SCL lines) due to the power supply will be less than 300mV peak-to-peak. This noise measurement should be made with an oscilloscope bandwidth limited to 100MHz. Measurements should be make at the power supply output connector with 10K ohm resistors pulled up to Standby Output and 47pF ceramic capacitors to Standby Output Return.

I²C Bus Internal Implementation, Pull-ups and Bus Capacitances



I²C Bus - Recommended external pull-ups:

Electrical and Interface specifications of I²C signals (referenced to StandBy Output Return pin, unless otherwise indicated):

Parameter	Condition	Symbol	Min	Typ	Max	Unit
SDA, SCL internal pull-up resistor		R_{int}	-	10	-	Kohm
SDA, SCL internal bus capacitance		C_{int}	-	10	-	pF
Recommended external pull-up resistor	1 to 4 PSU	R_{ext}	-	2.2	-	Kohm

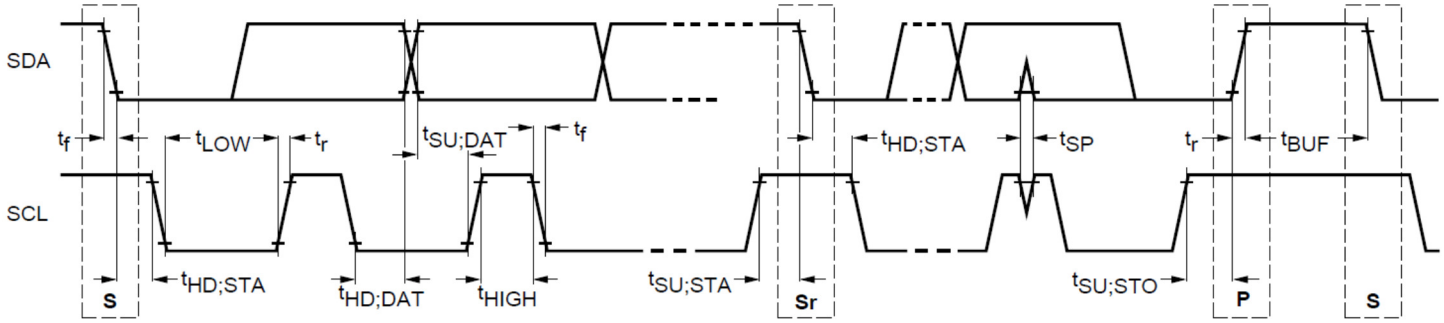
Logic Levels

CSU800 series power supply I²C Communication Bus will respond to logic levels as per below:

Logic High: 3.3V Nominal (Specs is 2.1V to 5.5V)**
Logic Low: 500mV nominal (Specs is 800mV max)**

**Note: Artesyn 73-769-001 I²C adapter was used.

Timings



Parameter	Symbol	Standard-Mode Specs		Actual Measured		Unit
		Min	Max			
SCL Clock Frequency	f_{SCL}	0	100	90.9		KHz
Hold time (repeated) START condition	$t_{HD;STA}$	4.0	-	4.74		µS
LOW period of SCL clock	t_{LOW}	4.7	-	4.86		µS
HIGH period of SCL clock	t_{HIGH}	4.0	-	4.84		µS
Setup time for repeated START condition	$t_{SU;STA}$	4.7	-	4.884		µS
Data hold time	$t_{HD;DAT}$	0	3.65	0.2416		µS
Data setup time	$t_{SU;DAT}$	250	-	4887		nS
Rise time	t_r	-	1000	SCL = 669.6	SDA = 710.4	nS
Fall time	t_f	-	300	SCL = 156.8	SDA = 146	nS
Setup time for STOP condition	$t_{SU;STO}$	4.0	-	5.02		µS
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	95***		µS

*** Note Artesyn 73-769-001 I²C adapter (USB-to-I²C) and Universal PMBus™ GUI software was used

Device Addressing

The CSU800 series will respond to supported commands on the I²C bus that are addressed according to pins A1 and A0 pins of output connector.

Address pins are held HIGH by default via pulled up to internal 3.3V supply with a 10K resistor. To set the address as “0”, the corresponding address line should be pulled down to logic ground level. Below tables show the address of the power supply with A0 and A1 pins set to either “0” or “1”.

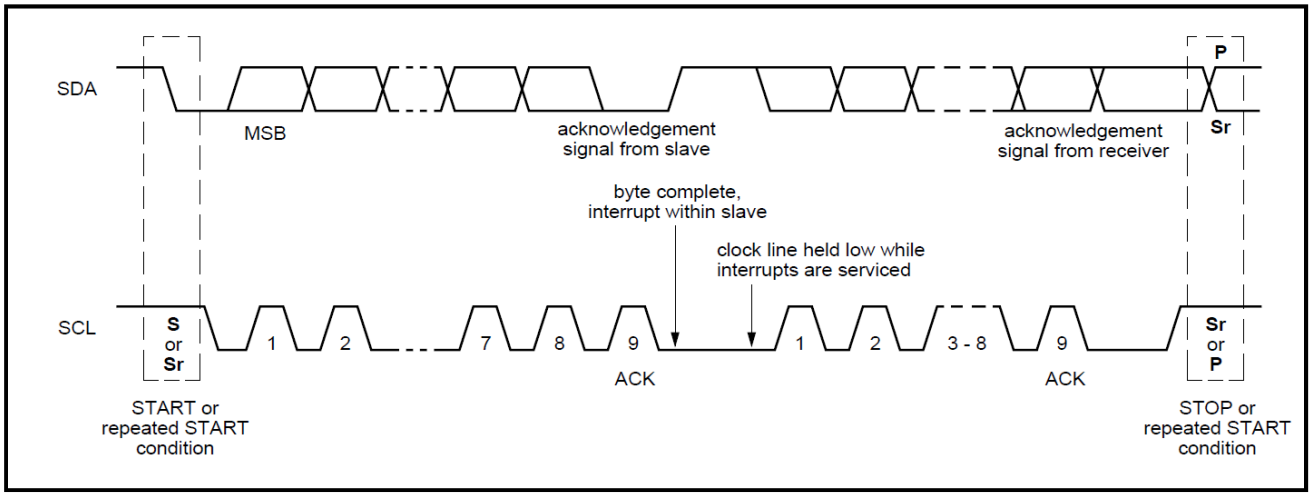
PSU Slot	Slot ID Bits		PMBus™ Address	EEPROM (FRU) Read Address
	A1	A0		
1	0	0	0xB0	0xA0
2	0	1	0xB2	0xA2
3	1	0	0xB4	0xA4
4	1	1	0xB6*	0xA6*

* Default PMBus™ address when A0 and A1 are left open

I²C Clock Synchronization

The CSU800 series power supply apply clock stretching. An addressed slave power supply hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The system master that is communicating with the power supply will attempt to raise the clock to transfer the next bit, but must verify that the clock line was actually raised. If the power supply is clock stretching, the clock line will still be low (because the connections are open-drain).

The maximum time out condition for clock stretching for CSU800 series is 100 microseconds.

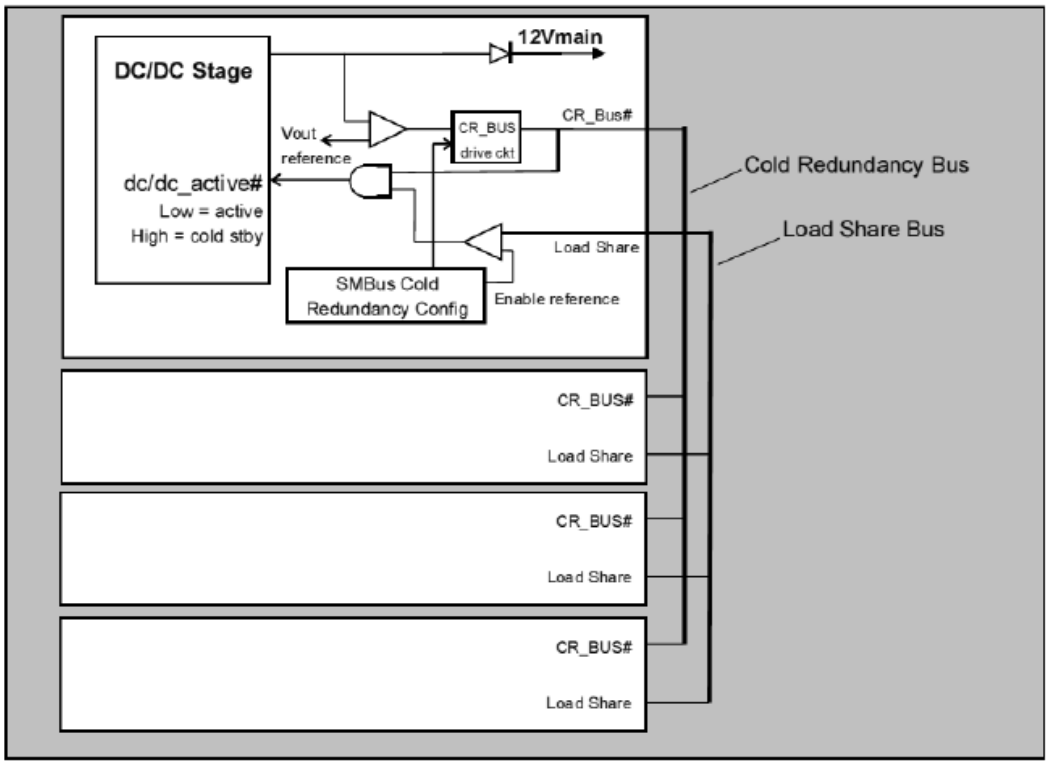


Cold Redundancy

The CSU800 series defines a signal pin for Cold Redundancy. This capability help improve the efficiency of the power subsystem when more than one power supply is used in a system; such as 1+1 or 2+1 or 3+1 or 2+2 redundantly powered systems. Cold Redundancy uses the PMBus™ manufacturer specific command area to define commands for the system to configure the power supplies for Cold Redundancy.

Overview

Below is a block diagram showing the Cold Redundancy architecture. When the power subsystem is in Cold Redundant mode the number of power supply in active mode is controlled by the load share bus voltage. As the load share bus voltage decreases the power supplies programmed for cold standby will power off into cold standby state. This maximizes the efficiency of the total power subsystem. As the load share voltage decreases to minimum loads only the power supply configured to be the Active power supply in the cold redundancy scheme remains ON. Each power supply has an additional signal that is dedicated to supporting Cold Redundancy; CR_BUS#, this signal is a common bus between all power supplies in the system. CR_BUS# is asserted (pulled low) when there is a fault in any power supply OR the power supplies output voltage falls below the voltage regulation. Asserting the CR_BUS# signal causes all power supplies in Cold Standby state to power ON. Whenever there is no Cold Redundant active power supply on the Cold Redundancy bus driving a HIGH level on the bus, all power supplies are ON no matter their defined Cold Redundant roll (Active or Cold Standby). This guarantees that incorrect programming of the Cold Redundancy states of the power supply will never cause the power subsystem to shutdown or become over loaded. The default state of the power subsystem is all power supplies ON. There needs to be at least one power supply in Cold Redundant Active state or Standard Redundant state to allow the Cold Standby state power supplies to go into Cold Standby state.



Cold Redundancy 3+1 (or 2+2) - Functional Block Diagram

The following table shows the state of the power supplies programmed for Cold Standby mode based on the condition of the CR_BUS# signal and the Load Share bus voltage.

Logic Matrix for Cold Standby Power Supplies

CR_BUS#	Load share	Cold Standby Power Supply State(s)
High	< VCR_ON	Cold Standby
Low	< VCR_ON	Active
High	> VCR_ON	Active
Low	> VCR_ON	Active

Note: VCR_ON is the voltage threshold set inside the power supplies configured for Cold Standby which tells them to power down into Cold Standby state when the load share voltage is less than VCR_ON.

Cold Standby Power Supply Operating State

When the power supply is in Cold Standby state the power supply must meet the following requirements.

1) Power ON in < 100µs when Cold_Red bus is driven LOW
2) Turn off its output OR-ing FET
3) Keep its internal output capacitor before the output OR-ing FET charged to not less than 12.6V
4) Keep PWOK asserted
5) Disconnect any output dummy loads to prevent discharging of the pre-charged output capacitor
6) Power off any internal fans
7) Pre-bias its voltage error amplifier to maximum duty cycle (preventing the loop compensation from slowing the turn on process when CR_BUS# asserts)
8) Disable its output slow start circuit
9) Keep the PFC stage ON at lowest possible operating frequency and its output bulk capacitor charged
10) No PMBus fault or warning conditions reported via STATUS commands
11) PMBus READ_EOUT command shall continue to increment its sample counter and update its power accumulator
12) PMBus READ_PIN command should continue to report its input power

Powering on Cold Standby supplies to maintain best efficiency

Power supplies in Cold Standby state monitor the shared voltage level of the load share signal to sense when it needs to power on. Depending upon which position (1, 2, or 3) the system defines for the power supply in the cold standby configuration; the power supply will go into cold standby state or ON state at different level of the load share bus. Since as power supplies power ON they will share the load and cause the load share bus level to change; there needs to be two thresholds in each power supply depending upon if the power supply is in ON state or in cold standby state. The VCR_ON_EN level is used by the power supply when it is in Cold Standby state telling it when to power ON based on the load share voltage level. The VCR_ON_DIS level is used by the power supply when it is in ON state telling it when to go into Cold Standby state based on the load share voltage level. Below is an example calculation for a 4 power supply parallel configuration.

Example Load Share Threshold for Activating Supplies

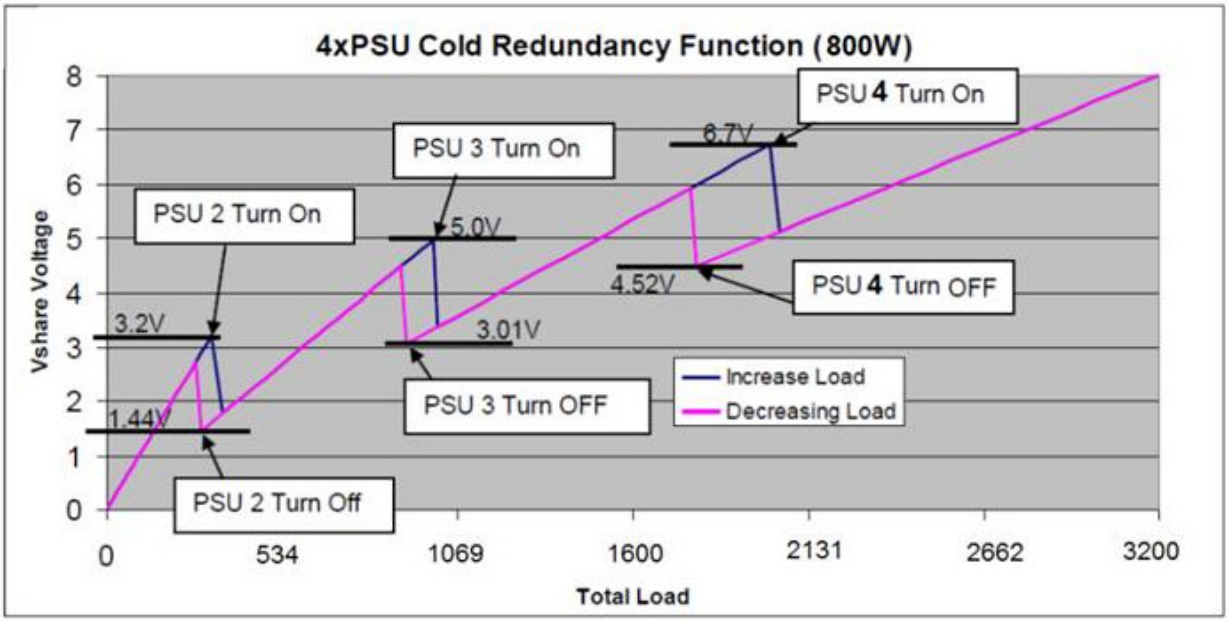
	Enable Threshold for VCR_ON_EN	Disable Threshold for VCR_ON_DIS
Standard Redundancy	NA; Ignore dc/dc_ active# signal; power supply is always ON	
Cold Redundant Active	NA; Ignore dc/dc_ active# signal; power supply is always ON	
Cold Standby 1 (02h)	3.2V (40% of max)	3.2V x 0.5 x 0.9 = 1.44V
Cold Standby 2 (03h)	5.0V (62% of max)	5.0V x 0.67 x 0.9 = 3.01V
Cold Standby 3 (04h)	6.7V (84% of max)	6.7V x 0.75 x 0.9 = 4.52V

Notes: Maximum load share voltage = 8.0V at 100% of rated output power
These are example load share bus threshold; for any power supply these shall be customized to maintain the best efficiency curve for that specific model.

Cold Standby Power Supply Turn On / Off

Powering on and off of the cold standby power supplies is controlled by each power supply sensing the load share bus voltage. Once a power supply turns on after crossing the enable threshold; it lowers its threshold to the disable threshold. The system defines the 'position' of each power supply in the Cold Redundant operation. Below are timing requirements and example plots of thresholds and load share voltage as load ramps on 4 parallel power supplies.

- When load ramps up and crosses the load share voltage threshold the module becoming active wake up time must be < 1ms to make sure at maximum load slew rate the power supply must be able to handle the system load.
- When load ramps down and crosses the load share voltage threshold module go-to-sleep (cold standby) time must be < 5ms



Example Power On/Off of power supplies in Cold Redundant Mode (4x800W PSUs)

Powering on Cold Standby supplies during a fault or over current condition

When an active power supply asserts its CR_BUS# signal (pulling it low), all parallel power supplies in cold standby mode shall power on within 100µs.

SMBus Commands for Cold Redundancy

Configuring Cold Redundancy with Cold_Redundancy_Config (D0h)

The PMBus™ manufacturer specific command MFR_SPECIFIC_00 is used to configure the operating state of the power supply related to cold redundancy. This command for Cold_Redundancy_Config is at D0h. Below is the definition of the values used with the Write Byte and Read Byte SMBus protocol with PEC. The below table shows the configuration of the power supply based on the value in the Cold_Redundancy_Config register.

The power supplies setup to be the cold standby power supplies; will change to standard redundancy mode (D0h = 00h) whenever the CR_BUS# is pulled low.

Cold Redundancy Configuration Table

Cold_Redundancy_Config (D0h)		
Value	**State**	**Description**
00h	Standard Redundancy (default power on state)	Turns the power supply ON into standard redundant load sharing more. The power supply's CR_BUS# signal shall be OPEN but still pull the bus low if a fault occurs to activate any power supplies still in Cold Standby state.
01h	Cold Redundant Active	Defines this power supply to be the one that is always ON in a cold redundancy configuration.
02h	Cold Standby 1	Defines the power supply that is first to turn on in a cold redundant configuration as the load increases.
03h	Cold Standby 2	Defines the power supply that is second to turn on in a cold redundant configuration as the load increases.
04h	Cold Standby 3	Defines the power supply that is third to turn on in a cold redundant configuration as the load increases.
05h	Always Cold Standby	Defines this power supply to be always in cold redundant configuration no matter what the load condition.
06h-FFh	Reserved	

When the CR_BUS# transitions from a high to a low state; each PSU programmed to be in Cold Standby state shall be put into Standard Redundancy mode (Cold_redundancy_Config = 00h). For the power supplies to enter Cold Redundancy mode the system must re-program the power supplies using the Cold_Redundancy_Config command.

Cold Redundant Signal (CR_BUS#)

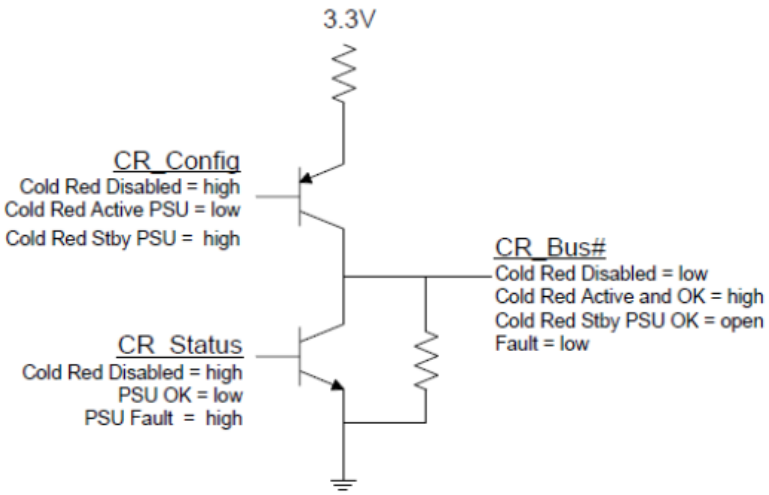
There is an additional signal defined supporting Cold Redundancy. This is connected to a bus shared between the power supplies: CR_BUS#. This is a tri-state output signal of the power supply used to communicate a fault or Vout under voltage level has occurred in one of the power supplies. This is used to power on all the power supplies in the system via the CR_BUS#. When the signal is pulled high it allows all power supplies in cold standby mode to go into cold standby state when the load share voltage is below the VCR_ON level. When the signal is left open on all power supplies it forces all cold standby power supplies into the ON. Below is a table showing the logic state of the CR_BUS# signal depending upon the programmed configuration of the power supply in D0h, the operating state of the power supply, and the power supply fault status.

Cold Redundancy State Table

Cold Redundant Config	Operating State	Power Supply Fault Status	CR_Bus#
Active	On	OK	High
Cold Standby 1,2,3	On	OK	Open
Cold Standby 1,2,3	Cold Standby	OK	Open
Active	Off	Fault	Low
Cold Standby 1,2,3	On	Fault	Low
Cold Standby 1,2,3	Cold Standby	Fault	Low

The below figure is a schematic representation of the logic for the CR_BUS# signal. The CR_Config input is programmed based on the value in the Cold_Redundancy_Config register.

The CR_Status input is based on both the Cold_Redundancy_Config register as well as the fault state of the power supply. The resulting output is a tri- state output. The output is Low when there is a Fault in any power supply or when Cold Redundancy is disabled. The output is High only when a power supply is programmed for the Cold Redundancy Active mode and it is functioning OK. The output is Open only when the power supply is programmed for Cold Redundant Standby mode and is functioning OK. This mean that there needs to be one good power supply programmed for Active Cold Redundant mode to allow power supply to function in cold standby mode; otherwise, all power supplies will power ON and come out of cold redundant mode.



CR_BUS# Functional Diagram

CR_BUS# Signal Characteristic

Signal Type	Active: Tri-state output Cold Standby: Input signal	
	Min	Max
Logic level low (power supply ON)	0 V	0.4 V
Logic level high (power supply OFF)	2.4 V	3.46 V
Source current, Cold Red = high	2 mA	
Sink current, Cold_Red = low	400 µA	
Cold_Red fault delay		10 µs
Cold_Red turn on delay		100 µs

BMC Requirements

The BMC uses the Cold_Redundancy_Config command to configure the power supply's roll in cold redundancy and to enabled / disable cold redundancy. It is recommended that the BMC schedule a rolling change for which PSU is the Active, Cold Stby1, Cold Stby 2, and Cold Stby 3 power supply. This allows for equal loading across power supply over their life.

Black Box

The power supply shall store PMBus and other data into non-volatile memory upon a critical failure that caused the power supply to shutdown. The data can be accessed via the PMBus interface by applying power to the $12V_{SB}$ pins. No AC power needs to be applied to the power supply.

Data is saved to the Black Box for the following fault events:

- General fault
- Over voltage on output
- Over current on output
- Loss of AC input
- Input voltage fault
- Fan failure
- Over temperature

Black Box Process:

1) System writes system tracking data to the power supply RAM at power ON
2) System writes the real time clock data to the PSU RAM once every ~5 minutes
3) Power supply tracks number of PSON and AC power cycles in FLASH
4) Power supply tracks ON time in FLASH
5) Power supply loads warning and fault event counter data from FLASH into RAM
6) Upon a warning event; the PSU shall increment the associated counter in RAM.
7) Upon and fault event the PSU shall increment the associated counter in RAM
8) Upon a fault event that causes the PSU to shutdown all event data in the PSU's RAM is saved to event data location N in the power supply's FLASH. This data includes the real time clock, number of AC & PSON power cycles, PSU ON time, warning event counters and fault event counters.

Commands:

Name: MFR_BLACKBOX
Format: Read Block with PEC (238 bytes)
Code: DCh

	Item	Number of Bytes	Description
System Tracking Data	System top assembly number	10	The system will write its Intel part number for the system top assembly to the power supply when it is powered ON. This is 9 ASCI characters.
	System serial number	10	The system shall write the system serial number to the power supply when it is powered ON. This include the serial number and date code.
	Motherboard assembly number	10	The system will write the motherboard Intel part number for the assembly to the power supply when it is powered ON. This is 9 ASCI characters.
	Motherboard serial number	10	The system shall write the motherboard's serial number to the power supply when it is powered ON. This includes the serial number and date code.
	Present total PSU ON time	3	Total on time of the power supply with PSON asserted in minutes. LSB = 1 minute.
	Present number of AC power cycles	2	Total number of times the power supply powered OFF then back ON due to loss of AC power. This is only counted when the power supply's PSON# signal is asserted. This counter shall stay at FFFFh once the max is reached.
	Present number of PSON power cycles	2	Total number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting. This is only counted when AC power is present to the power supply. This counter shall stay at FFFFh once the max is reached.
Power supply event data (N)		38	Most recent occurrence of saved black box data
Time Stamp			The power supply shall track these time and power cycle counters in RAM. When the a black box event occurs the data is saved into the Black Box.
	Power supply total power on time	3	Total on time of the power supply in minutes. LSB = 1 minute.
	Real Time Clock Data from System (reserved for future use)	4	This time stamp does not need to generated by the power supply. The system rights a real time clock value periodically to the power supply using the MFR_REAL_TIME command. Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C
	Number of AC power cycles	2	Number of times the power supply powered OFF then back ON due to loss of AC power at the time of the event. This is only counted when the power supply's PSON# signal is asserted.
	Number of PSON power cycles	2	Number of times the power supply is powered OFF then back ON due to the PSON# signal deasserting at the time of the event. This is only counted when AC power is present to the power supply.

	Item	Number of Bytes	Description
PMBus			The power supply shall save these PMBus values into the Black Box when a black box event occurs. Fast events may be missed due to the filtering effects of the PMBus sensors
	STATUS_WORD	2	
	STATUS_IOUT	1	
	STATUS_INPUT	1	
	STATUS_TEMPERTATURE	1	
	STATUS_FAN_1_2	1	
	READ_VIN	2	
	READ_IIN	2	
	READ_IOUT	2	
	READ_TEMPERATURE_1	2	
	READ_TEMPERATURE_2	2	
	READ_FAN_SPEED_1	2	
	READ_PIN	2	
	READ_VOUT	2	
Event Counters			The power supply shall track the total number for each of the following events. These value shall be saved to the black box when a black box event occurs. Once a value has reached 15, it shall stay at 15 and not reset.
	AC shutdown due to under voltage on input	Lower ½	The power supply shall save a count of these critical events to non-volatile memory each time they occur. The counters will increment each time the associated STATUS bit is asserted.
	Thermal shutdown	Upper ½	
	Over current or over power shutdown on output	Lower ½	
	General failure shutdown	Upper ½	
	Fan failure shutdown	Lower ½	
	Shutdown due to over voltage on output	Upper ½	
	Input voltage warning;no shutdown	Lower ½	The power supply shall save into RAM a count of these warning events. Events are count only at the initial assertion of the event/bit. If the event persists without clearing the bit the counter will not be incremented. When the power supply shuts down it shall save these warning event counters to non-volatile memory. The counters will increment each time the associated STATUS bit is asserted.
	Thermal warning; no shutdown	Upper ½	
	Output current power warning; no shutdown	Lower ½	
	Fan slow warning; no shutdown	Upper ½	
Power supply event data (N-1)		38	
Power supply event data (N-2)		38	
Power supply event data (N-3)		38	
Power supply event data (N-4)		38	

Name: MFR_REAL_TIME_BLACK_BOX

Format: Write/Read Block with PEC (4 bytes)

Code: DDh

The system shall use this command to periodically write the real time clock data to the power supply.

Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100.

This is based on a long standing UNIXbased standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C.

Name: MFR_SYSTEM_BLACK_BOX
Format: Write/Read Block with PEC (40 bytes). Low byte first.
Code: DEh

The system uses this command to write the following data to the PSU.

Item	Bytes	
System top assembly number	1-10	Low bytes
System serial number	11-20	
Motherboard assembly number	21-30	
Motherboard serial number	31-40	High bytes

Name: MFR_BLACKBOX_CONFIG
Format: Read/Write Byte with PEC
Code: DFh

Bit	Value	Description
0	0 = disable black box function 1 = enable black box function	Writing a 1 enables the power supply with black box function. Writing a 0 disables the power supply black box function. The state of MFR_BLACKBOX_CONFIG shall be saved in non-volatile memory so that it is not lost during power cycling. Intel shall receive the power supply with the black box function enabled; bit 0 = '1'.

Name: MFR_CLEAR_BLACKBOX
Format: Send Byte with PEC
Code: E0h

The MFR_CLEAR_BLACKBOX command is used to clear all black box records simultaneously.
This command is write only. There is no data byte for this command.

FRU (EEPROM) Data

The FRU (Field Replaceable Unit) data format is compliant with the Intel IPMI v1.0 specification.

The CSU800 series uses 1 page of EEPROM for FRU purpose. A page of EEPROM contains up to 256 byte-sized data locations.

Where: OFFSET - The OFFSET denotes the address in decimal format of a particular data byte within CSU800 series EEPROM.

VALUE - The VALUE details data written to a particular memory location of the EEPROM.

DEFINITION - The contents DEFINITION refers to the definition of a particular data byte.

CSU800 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
		COMMON HEADER, 8 BYTES		
0	00	**FORMAT VERSION NUMBER** (Common Header) 7:4 - Reserved, write as 0000b 3:0 - Format Version Number = 1h for this specification	1	01
1	01	**INTERNAL USE AREA OFFSET** (Not required, do not reserve)	0	00
2	02	**CHASSIS INFO AREA OFFSET** (Not required, do not reserve)	0	00
3	03	**BOARD INFO AREA OFFSET** (Not required, do not reserve)	0	00
4	04	**PRODUCT INFO AREA OFFSET**	1	01
5	05	**MULTI RECORD AREA OFFSET**	9	09
6	06	**PAD** (Not required, do not reserve)	0	00
7	07	**ZERO CHECK SUM** (256 – (Sum of bytes 0 to 6))	NA	NA
		PRODUCT INFORMATION AREA, 64 BYTES		
8	08	**FORMAT VERSION NUMBER** (Product Info Area) 7:4 - Reserved, write as 0000b 3:0 - Format Version Number = 1h for this specification	1	01
9	09	**PRODUCT INFO AREA LENGTH** (In multiples of 8 bytes)	8	08
10	0A	**Language (English)**	25	19
11	0B	**MANUFACTURER NAME TYPE / LENGTH (C7H)** 7:6 - (11)b, 8-Bit ASCII + Latin 1, 5:0 - (000111)b, 7-Byte Allocation	199	C7
		MANUFACTURER'S NAME 7 byte sequence		
12	0C	"A"= 41h	65	41
13	0D	"R"= 52h	82	52
14	0E	"T"= 54h	84	54
15	0F	"E"= 45h	69	45
16	10	"S"= 53h	83	53
17	11	"Y"= 59h	89	59
18	12	"N"= 4Eh	78	4E
19	13	**PRODUCT NAME** Type/Length (D0H) Type = "ASCII+LATIN1" = (11)b Length = 16 Bytes = (010000)b	208	D0

CSU800 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
		Product Name, 8 Byte sequence		
20	14	**"CRPS800W"**	67	43
21	15	In Decimal = 067d, 082d, 080d, 083d, 056d, 048d, 048d, 087d, 32d, 32d, 32d, 32d, 32d, 32d, 32d,	82	52
22	16	32d	80	50
23	17	In Hex = 43H, 52H, 50H, 53H, 38H, 30H, 30H, 57H, 20H, 20H, 20H, 20H, 20H, 20H, 20H, 20H	83	53
24	18		56	38
25	19		48	30
26	1A		48	30
27	1B		87	57
28	1C		32	20
29	1D		32	20
30	1E		32	20
31	1F		32	20
32	20		32	20
33	21		32	20
34	22		32	20
35	23		32	20
36	24	**PRODUCT PART/MODEL NUMBER** Type/Length (D0H) Type = "ASCII+LATIN1" = (11)b Length = 16 Bytes = (010000)b	208	D0
		Part / Model Number		
37	25	"CSU800AP-3"	67	43
38	26	In Decimal = 067d, 083d, 085d, 056d, 048d, 048d, 065d, 080d, 045d, 051d	83	53
39	27	In Hex = 43H, 53H, 55H, 38H, 30H, 30H, 41H, 50H, 2DH, 33H	85	55
40	28	Note: For Inspur version, the model is "CSU800AP-3-100".	56	38
41	29		48	30
42	2A		48	30
43	2B		65	41
44	2C		80	50
45	2D		45	2D
46	2E		51	33
47	2F		32	20
48	30		32	20
49	31		32	20
50	32		32	20
51	33		32	20
52	34	**PRODUCT VERSION NUMBER** Type/Length (C2h) Type = "ASCII+LATIN1" = (11)b Length = 2 bytes = (000010)b	194	C2
53	35	**Version,** 2 Byte sequence	XX	XX
54	36	"XX"	XX	XX
55	37	**PRODUCT SERIAL NUMBER** Type/Length Type = "ASCII+LATIN1" = (11)b Length = 13 bytes = (001101)b	205	CD
		Serial number, 13 Byte sequence		
56	38	"XXXXXXXXXXXXX"	XX	XX
57	39		XX	XX
58	3A		XX	XX
59	3B		XX	XX
60	3C		XX	XX
61	3D		XX	XX
62	3E		XX	XX
63	3F		XX	XX
64	40		XX	XX
65	41		XX	XX
66	42		XX	XX
67	43		XX	XX
68	44		XX	XX
		PAD (reserved)		
69	45	Default value is 0.	0	00
70	46	Default value is 0.	0	00

CSU800 series FRU (EEPROM) Data:

OFFSET (DEC)	OFFSET (HEX)	DEFINITION (REMARKS)	SPEC VALUE (DEC)	SPEC VALUE (HEX)
71	47	**ZERO CHECK SUM** (256-(sum of bytes 8 to 70)) Per Unit Zero Check Sum :Should follow check sum calculation as per IPMI v1.3 specs	NA	NA
		Multi Record Area, 56 Bytes		
		Power Supply Record Header		
72	48	Record Type = 00 for power supply info	0	00
73	49	End of List /Record Format Version Number for 12V Output Record	2	02
74	4A	Record Length of 12V Output Record	20	14
75	4B	Record checksum	NA	NA
76	4C	header checksum	NA	NA
		Power Supply Record		
		Combined Wattage,Byte 1 and Byte 2: 800W = 0320H byte 1 (LSB) = 20h = 32d byte 2 (MSB) =03h = 03d 2 Bytes Sequence		
77	4D	In Decimal = 32d, 03d	32	20
78	4E	In Hex = 20h,03h	03	03
		Peak VA, 1500W = 05DCH 2 Bytes Sequence		
79	4F	In Decimal = 220d, 5d	220	DC
80	50	In Hex = DCH, 05H	05	05
81	51	**Inrush Current**, 35A In Decimal = 35d In Hex = 23H	35	23
82	52	**Inrush Interval**, 5mS In Decimal = 5d In Hex = 05H	05	05
		Low End Input Voltage Range 1(10mV), (90V / 10mV) 9000 = 2328H 2 Bytes Sequence		
83	53	In Decimal = 40d, 35d	40	28
84	54	In Hex = 28H, 23H	35	23
		High End Input Voltage Range 1(10mV), (264V/10mV) 26400= 6720H 2 Bytes Sequence		
85	55	In Decimal = 032d, 103d	32	20
86	56	In Hex = 20H, 67H	103	67
87	57	**Low End Input Frequency** Range, 47Hz = 2FH	47	2F
88	58	**Low End Input Frequency Range,** 63Hz = 3FH	63	3F
89	59	**AC Dropout Tolerance in ms,** 12mS= 0CH	12	0C
90	5A	**Binary Flags: For each of the following binary flags No = 0, Yes = 1;.** Bits 7-5: RESERVED, WRITE AS 000B Bit4: Tachometer Pulses Per Rotation / Predictive Fail Polarity BIT = 0 Bit3: Hot Swap / Redundancy Support BIT = 1 Bit2: Auto switch Support BIT = 1 Bit1: Power Factor Correction Support BIT = 1 Bit0: Predictive Fail Support BIT = 0	14	0E
		Peak Wattage Capacity and Holdup Time ,(Set for 960Watts/3S)		
91	5B	In Decimal = 192 In Hex = C0H (LSB First)	192	C0
92	5C	In Decimal = 243 In Hex = F3H	243	F3
		Combined Wattage,		
93	5D		0	00
94	5E	No combined voltage for this power supply	0	00
95	5F		0	00
96	60	**Predictive Fail Tachometer Lower Threshold,** Not Applicable. Predictive Failure is not Supported.	00	00

CSU800 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
		12V OUTPUT RECORD HEADER		
97	61	Record Type = 09 for power supply info	09	09
98	62	End of List /Record Format Version Number for 12V Output Record	02	02
99	63	Record Length of 12V Output Record	13	0D
100	64	Record checksum (256-(sum of bytes 102 to 114))	NA	NA
101	65	header checksum (256-(sum of bytes 97 to 100))	NA	NA
		12V OUTPUT RECORD		
102	66	**Output Information,** 001 = 01H Bit 7: Standby Information = 0B Bits 6-5: Reserved, Write as 000B Bits 4: Current units, 0b = 10mA Bits 3-0: Output Number 1 = 001B	01	01
103 104	67 68	**Nominal Voltage (10mV), (12V / 10mV)** 1200 = 04B0H 2 Bytes Sequence In Decimal: 176d, 004d In Hex: B0H, 04H	176 04	B0 04
105 106	69 6A	**Maximum Negative Voltage Deviation (10mV),** 1140 = 0474H 2 Bytes Sequence In Decimal: 116d, 004d In Hex: 74H, 04H	116 04	74 04
107 108	6B 6C	**Maximum Positive Voltage Deviation (10mV),** 1260 =04ECH 2 Bytes Sequence In Decimal: 236d, 004d In Hex: ECH, 04H	236 4	EC 04
109 110	6D 6E	**Ripple and Noise pk-pk (mV),** 120 = 78H 2 Bytes Sequence In Decimal: 120d, 000d In Hex: 78H, 00H	120 0	78 00
111 112	6F 70	**Minimum Current Draw (mA),** 0000 = 0000H 2 Bytes Sequence In Decimal: 000d, 000d In Hex: 00H, 00H	0 0	00 00
113 114	71 72	**Maximum Current Draw (mA),** 6670 = 1A0EH 2 Bytes Sequence In Decimal: 14d, 26d In Hex: 0EH, 1AH	14 26	0E 1A
		12VSB OUTPUT RECORD HEADER		
115	73	Record type = 01 for DC Output Record	01	01
116	74	End of List /Record Format Version Number for 12VSB Output Record	130	82
117	75	Record Length of 12V DC Output Record	13	0D
118	76	Record CHECKSUM of 12VSB Output Record	NA	NA
119	77	Header CHECKSUM of 12VSB Output Record Header	NA	NA
		12VSB OUTPUT RECORD		
120	78	**Output Information,** 002 = 02H Bit 7: Standby Information = 1B Bits 6-4: Reserved, Write as 000B Bits 3-0: Output Number 2 = 0010B	130	82
121 122	79 7A	**Nominal Voltage (10mV), (12V / 10mV)** 1200 = 04B0H 2 Bytes Sequence In Decimal: 176d, 004d In Hex: B0H, 04H	176 4	B0 04
123 124	7B 7C	**Maximum Negative Voltage Deviation (10mV),** 1140 = 0474H 2 Bytes Sequence In Decimal: 116d, 004d In Hex: 74H, 04H	116 04	74 04

CSU800 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
		Maximum Positive Voltage Deviation (10mV), 1260 =04ECH		
		2 Bytes Sequence		
125	7D	In Decimal: 236d, 004d	236	EC
126	7E	In Hex: ECH, 04H	4	04
		Ripple and Noise pk-pk (mV), 120 = 78H		
		2 Bytes Sequence		
127	7F	In Decimal: 120d, 000d	120	78
128	80	In Hex: 78H, 00H	0	00
		Minimum Current Draw (10mA), 0000 = 0000H		
		2 Bytes Sequence		
129	81	In Decimal: 000d, 000d	0	00
130	82	In Hex: 00H, 00H	0	00
		Maximum Current Draw (10mA), 2500 = 09C4H		
		2 Bytes Sequence		
131	83	In Decimal: 184d, 11d	184	B8
132	84	In Hex: B8H, 0BH	11	0B
133	85	Reserved, Default value is 0.	0	00
134	86	Reserved, Default value is 0.	0	00
135	87	Reserved, Default value is 0.	0	00
136	88	(88h-FFh is Reserved, Default value is 0.)	0	0
137	89		0	0
138	8A		0	0
139	8B		0	0
140	8C		0	0
141	8D		0	0
142	8E		0	0
143	8F		0	0
144	90		0	0
145	91		0	0
146	92		0	0
147	93		0	0
148	94		0	0
149	95		0	0
150	96		0	0
151	97		0	0
152	98		0	0
153	99		0	0
154	9A		0	0
155	9B		0	0
156	9C		0	0
157	9D		0	0
158	9E		0	0
159	9F		0	0
160	A0		0	0
161	A1		0	0
162	A2		0	0
163	A3		0	0
164	A4		0	0
165	A5		0	0
166	A6		0	0
167	A7		0	0
168	A8		0	0
169	A9		0	0
170	AA		0	0
171	AB		0	0
172	AC		0	0
173	AD		0	0
174	AE		0	0
175	AF		0	0
176	B0		0	0

CSU800 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
177	B1	(88h-FFh is Reserved, Default value is 0.)	0	0
178	B2		0	0
179	B3		0	0
180	B4		0	0
181	B5		0	0
182	B6		0	0
183	B7		0	0
184	B8		0	0
185	B9		0	0
186	BA		0	0
187	BB		0	0
188	BC		0	0
189	BD		0	0
190	BE		0	0
191	BF		0	0
192	C0		0	0
193	C1		0	0
194	C2		0	0
195	C3		0	0
196	C4		0	0
197	C5		0	0
198	C6		0	0
199	C7		0	0
200	C8		0	0
201	C9		0	0
202	CA		0	0
203	CB		0	0
204	CC		0	0
205	CD		0	0
206	CE		0	0
207	CF		0	0
208	D0		0	0
209	D1		0	0
210	D2		0	0
211	D3		0	0
212	D4		0	0
213	D5		0	0
214	D6		0	0
215	D7		0	0
216	D8		0	0
217	D9		0	0
218	DA		0	0
219	DB		0	0
220	DC		0	0
221	DD		0	0
222	DE		0	0
223	DF		0	0
224	E0		0	0
225	E1		0	0
226	E2		0	0
227	E3		0	0
228	E4		0	0
229	E5		0	0
230	E6		0	0
231	E7		0	0
232	E8		0	0
233	E9		0	0
234	EA		0	0
235	EB		0	0
236	EC		0	0
237	ED		0	0

CSU800 series FRU (EEPROM) Data:

OFFSET		DEFINITION	SPEC VALUE	
(DEC)	(HEX)	(REMARKS)	(DEC)	(HEX)
238	EE	(88h-FFh is Reserved, Default value is 0.)	0	0
239	EF		0	0
240	F0		0	0
241	F1		0	0
242	F2		0	0
243	F3		0	0
244	F4		0	0
265	F5		0	0
246	F6		0	0
247	F7		0	0
248	F8		0	0
249	F9		0	0
250	FA		0	0
251	FB		0	0
252	FC		0	0
253	FD		0	0
254	FE		0	0
255	FF		0	0

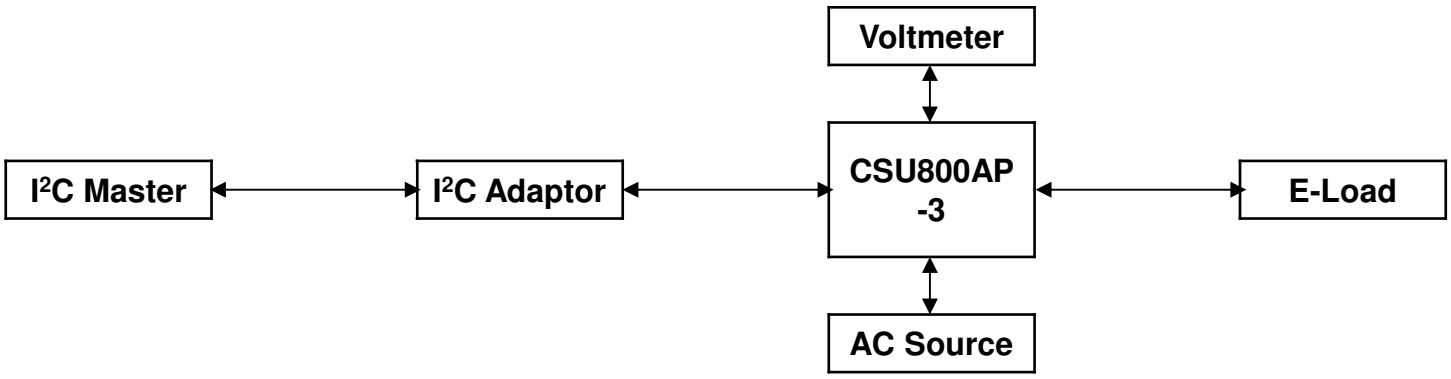
PMBus™ Interface Support

The CSU800 series is compliant with the industry standard PMBus™ protocol for monitoring and control of the power supply via the I²C interface port.

CSU800 Series PMBus™ General Instructions

Equipment Setup

The following is typical I²C communication setup:



CSU800 Series Support PMBus™ Command List

The CSU800 series is compliant with the industry standard PMBus™ protocol for monitoring and control of the power supply via the I²C interface port.

CSU800 Series Supported PMBus™ Command List:

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
00h	Page	0	R/W	1	Hex	Valid input: 00h
01h	OPERATION	80	R/W	1	Bitmapped	Used to turn the unit ON/OFF in conjunction with the input PSON pin.
	b7:6	10				00 - Immediate Turn OFF (No Sequencing) 01 - Soft Turn OFF (With Sequencing) 10 - PSU ON
	b5:4	00				Reserved
	b3:2	00				Reserved
	b1:0	00				Reserved
03h	CLEAR_FAULTS	0	S		N/A	
19h	CAPABILITY	90	R	1	Bitmapped	Provides a way for the hosts system to determine some key capabilities of a PMBus™ device.
	b7 - Packet Error Checking	1				0 - PEC not supported 1 - PEC supported
	b6:5 - Maximum Bus Speed	00				00 - Maximum supported bus speed, 100KHz 01 - Maximum supported bus speed, 400KHz
	b4 - SMBALERT#	1				0 - SMBus Alert Pin not supported 1 - SMBus Alert Pin supported
	b3 - Numeric Format	0				0 - Linear11, Ulinear16, Slinear16, or Direct 1 - IEEE Half Precision Floating Point Format
	b2 - AVSBus	0				0 - AVSBus not supported 1 - AVSBus supported
	b1:0	00				Reserved
1Ah	QUERY	-	BR/BW		N/A	Used to determine if the PSU supports a specific command; It should return the proper information about any commands listed
1Bh	SMBALERT_MASK	-	BR/BW		N/A	Used with STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT
20h	VOUT_MODE	17	R	1	Bitmapped	Specifies the mode and parameters of Output Voltage related Data Formats
30h	COEFFICIENTS		BW/BR	5	Hex	Use to retrieve the m, b and R coefficients, needed for DIRECT data format
	byte 5	00				R byte
	byte 4:3	0000				b low Byte, b high byte
	byte 2:1	0001				m low Byte, m high byte
3Ah	FAN_CONFIG_1_2	90	R	1	Bitmapped	
	b7	1				0 - No fan is installed in position 1 1 - Fan is installed in position 1
	b6	0				0 - Fan is commanded in Duty Cycle 1 - Fan is commanded in RPM
	b5:4	01				00 - 1 pulse per revolution 01 - 2 pulse per revolution 10 - 3 pulse per revolution 11 - 4 pulse per revolution
	b3:0	0000				Reserved

CSU800 Series Supported PMBus™ Command List:

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
3Bh	FAN_COMMAND_1	0000	R/W	2	Linear	Adjusts the operation of the Fans. The device may override the command, if it requires higher value, to maintain proper device temperature. Duty cycle Control - Commands Speeds from 0 to 100%
46h	IOUT_OC_FAULT_LIMIT	EAB0	R	2	Linear	Sets the Over Current Threshold in Amps. (86.00A)
4Ah	IOUT_OC_WARNING_LIMIT	EA58	R	2	Linear	Sets the Over Current Warning Threshold in Amps. (75.00A)
51h	OT_WARN_LIMIT(Hot Spot)	0055	R	2	Hex	Secondary ambient temperature warning threshold, in degree C. Operating limit (85degC)
5Dh	IIN_OC_WARN_LIMIT	CAC0	R	2	Linear	Sets the Over Current Threshold in Amps. (5.50A)
6Ah	POUT_OP_WARN_LIMIT	0398	R	2	Linear	Sets the output Over Power Threshold in Watt. (920W)
6Bh	PIN_OP_WARN_LIMIT	03E8	R	2	Linear	Sets the Over Power Threshold in Watt. (1000W)
78h	STATUS_BYTE	-	R	1	Bitmapped	Returns the summary of critical faults
	b6 – OFF					Unit is OFF
	b5 - VOUT_OV					Output over-voltage fault has occurred
	b4 - IOUT_OC					Output over-current fault has occurred
	b3 - VIN_UV					An input under-voltage fault has occurred
	b2 – TEMPERATURE					A temperature fault or warning has occurred
	b1 - CML					A communication, memory or logic fault has occurred.
79h	STATUS_WORD	-	R	2	Bitmapped	Summary of units Fault and warning status.
	b15 – VOUT					An output voltage fault or warning has occurred
	b14 – IOUT					An Output current or power fault or warning has occurred.
	b13 – INPUT					An input voltage, current or power fault or warning as occurred.
	b11 - POWER_GOOD#					The POWER_GOOD signal is de-asserted
	b10 – FANS					A fan or airflow fault or warning has occurred.
	b7 – BUSY					A fault was declared because the device was busy and unable to respond.
	b6 – OFF					Unit is OFF
	b5 - VOUT_OV					Output over-voltage fault has occurred
	b4 - IOUT_OC					Output over-current fault has occurred
	b3 - VIN_UV					An input under-voltage fault has occurred
	b2 – TEMPERATURE					A temperature fault or warning has occurred
	b1 – CML					A communication, memory or logic fault has occurred.
7Ah	STATUS_VOUT	-	R	1	Bitmapped	
	b7 - VOUT Over-Voltage Fault	-				VOUT Over-Voltage Fault
	b4 - VOUT Under-Voltage Fault	-				VOUT Under-Voltage Fault

CSU800 Series Supported PMBus™ Command List:

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
7Bh	STATUS_IOUT		R	1	Bitmapped	
	b7 - IOUT Overcurrent Fault					IOUT Overcurrent Fault
	b5 - IOUT Overcurrent Warning					IOUT Overcurrent Warning
	b1 - POUT_OP_FAULT					POUT_OP_FAULT
	b0 - POUT_OP_WARNING					POUT_OP_WARNING
7Ch	STATUS_INPUT		R	1	Bitmapped	Input related faults and warnings
	b7 - VIN_OV_FAULT					VIN Over voltage Fault
	b5 - VIN_UV_WARNING					VIN Under voltage Warning
	b4 - VIN_UV_FAULT					VIN Under voltage Fault
	b3 - Unit Off For Low Input Voltage					Unit is OFF for insufficient Input Voltage
	b1 - IIN_OC_WARNING					IIN Overcurrent Warning
	b0 - PIN_OP_WARNING					PIN Overpower Warning
7Dh	STATUS_TEMPERATURE		R	1	Bitmapped	Temperature related faults and warnings
	b7 - Over temperature Fault					Over temperature Fault
	b6 - Over temperature Warning					Over temperature Warning
7Eh	STATUS_CML		R	1	Bitmapped	Communications, Logic and Memory
	b7 - Invalid/Unsupported command					Invalid or unsupported Command Received
	b6 - Invalid/Unsupported Data					Invalid Data
	b5 - Packet Error Check Failed					Packet Error Check Failed
80h	INPUT_TYPE		R	1	Hex	00h - no input 01h - AC input 02h - DC input
81h	STATUS_FANS_1_2	00	R	1	Bitmapped	
	b7 - Fan1 Fault					Fan1 Fault
	b5 - Fan1 Warning					Fan1 Warning
	b3 - Fan1 Speed Overridden					Fan1 Speed Overridden
86h	Ein		BR	6	Direct	Returns the accumulated input power over time
87h	Eout		BR	6	Direct	Returns the accumulated output power over time
88h	READ_VIN		R	2	Linear	Returns input Voltage in Volts ac.
89h	READ_IIN		R	2	Linear	Returns input Current in Amperes
8Bh	READ_VOUT		R	2	Linear	Returns the actual, measured voltage in Volts.
8Ch	READ_IOUT		R	2	Linear	Returns the output current in amperes.
8Dh	READ_TEMPERATURE_1 (Ambient)		R	2	Linear	Returns the ambient temperature in degree Celsius.
8Eh	READ_TEMPERATURE_2 (Hot Spot)		R	2	Linear	Returns the hot pot temperature in degree Celsius.
90h	READ_FAN_SPEED_1		R	2	Linear	Speed of Fan 1
96h	READ_POUT		R	2	Linear	Returns the output power, in Watts.
97h	READ_PIN		R	2	Linear	Returns the input power, in Watts.

CSU800 Series Supported PMBus™ Command List:

Command Code	Command Name	Default Value	Access Type	Data Bytes	Data Format	Description
98h	PMBUS_REVISION	22	R	1	Bitmapped	Reads the PMBus revision number
	b7:5	0001				Part 1 Revision 0000 - Revision 1.0 0001 - Revision 1.1
	b4:0	0001				Part 2 Revision 0000 - Revision 1.0 0001 - Revision 1.1
99h	MFR_ID	ARTESYN### ##### (0x41 52 54 45 53 59 4E 23 23 23 23 23 23 23 23)	BR	15	ASCII	Abbrev or symbol of manufacturers name, ASCII format.
9Ah	MFR_MODEL	CSU800AP-3##### (0x43 53 55 38 30 30 41 50 2D 33 23 23 23 23 23)	BR	15	ASCII	Manufacturers Model number, ASCII format
9Bh	MFR_REVISION	NA	BR	6	ASCII	1st byte and 4th byte is 0x00. 2nd and 3rd byte: Secondary major and minor revision. 5th and 6th byre: Primary major and minor revision.
9Ch	MFR_LOCATION	LUODING (0x4C 55 4F 44 49 4E 47)	BR	7	ASCII	Manufacturers facility, ASCII format
9Dh	MFR_DATE	0816 (0x30 38 31 36)	BR	4	ASCII	Manufacture Date, ASCII format structure : MMYY
9Eh	MFR_SERIAL	"xxxxxxxxxxxxxxxxxx"	BR	15	ASCII	Unit serial number, ASCII format.
A0h	MFR_VIN_MIN	005A	R	2	Linear	Minimum Input Voltage (90Vac)
A1h	MFR_VIN_MAX	0108	R	2	Linear	Maximum Input Voltage (264Vac)
A4h	MFR_VOUT_MIN	16CD	R	2	Linear	Minimum Output Voltage Regulation Window. (11.4V)
A5h	MFR_VOUT_MAX	1933	R	2	Linear	Maximum Output Voltage. Regulation Window (12.6V)
A6h	MFR_IOUT_MAX	EA16	R	2	Linear	Maximum Output Current (66.7A)
A7h	MFR_POUT_MAX	0320	R	2	Linear	Maximum Output Power (800W)
C0h	MFR_MAX_TEMP_1 (Ambient)	0046	R	2	Linear	Maximum ambient temperature (65degC)
C1h	MFR_MAX_TEMP_2 (hot Spot)	0069	R	2	Linear	Maximum hot sopt temperature (87degC)
D0h	Cold_Redundancy_Config	00	R/W	1	Hex	00 - Normal 01 - Active 02 - Cold Standby 1 03 - Cold Standby 2 04 - Cold Standby 3 05 – Always Cold Standby
DCh	MFR_BLACKBOX		BR	238		
DDh	MFR_REAL_TIME_BLACK_BOX		BR/BW	4		
DEh	MFR_SYSTEM_BLACK_BOX		BR/BW	40		
DFh	MFR_BLACKBOX_CONFIG		R/W			
E0h	MFR_CLEAR_BLACKBOX		W			

CSU800 Series Firmware Upload Command List:
The power supply uses the following command during the boatload process.

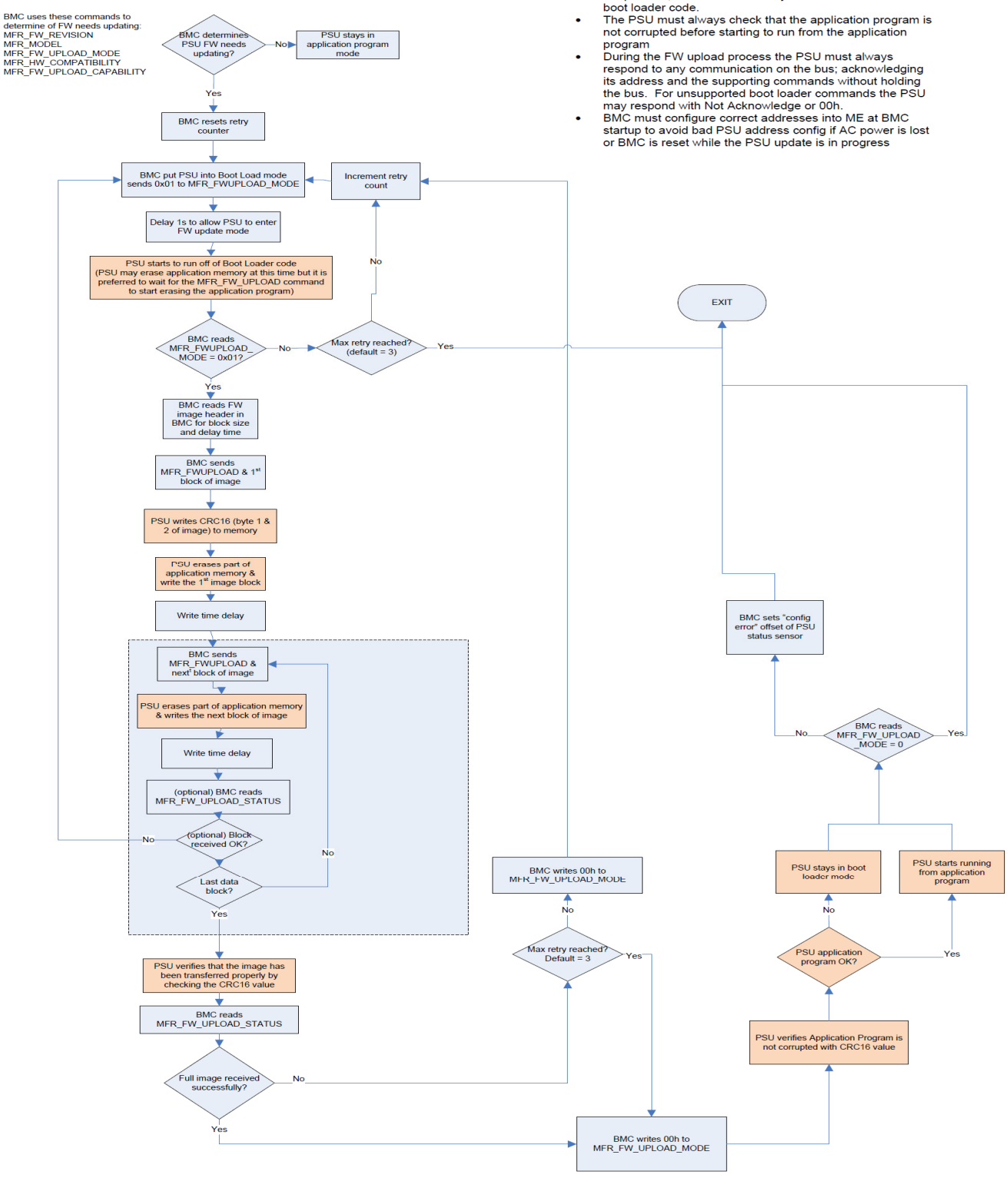
Command Code	Command Name	Default Value	Access Type	Data Bytes	Description
D4h	MFR_HW_COMPATIBILITY	-	R	-	This is a COMPATIBILITY value used to tell if there are any changes in the FW that create an incompatibility with the FW. This value only changes when the PSU HW is changed creating an incompatibility with older versions of FW
D5h	MFR_FWUPLOAD_CAPABILITY	-	R	-	The system can read the power supply's FW upload mode capability using this command. For any given power supply; more than one FW upload mode may be supported. The supported FW upload mode(s) must support updating all available FW in the power supply. This power supply supports FW uploading in standby mode only. Bit 0: "1" FW uploading in standby mode only All other bits configurations are not supported
D6h	MFR_FWUPLOAD_MODE	-	R/W	-	Writing a 1 puts the power supply into firmware upload mode and gets it ready to receive the first image block via the MFR_FW_UPLOAD command. The system can use this command at any time to restart sending the FW image. Writing a 0 puts the power supply back into normal operating mode. Writing a 1 restart This command will put the PSU into standby mode if the PSU supports FW update in standby mode only. If the power supply image passed to the PSU is corrupt the power supply shall stay in firmware upload mode even if the system requested the PSU to exit the FW upload mode. Value: 0 = exit firmware upload mode 1 = firmware upload mode
D7h	MFR_FWUPLOAD		BW		Command used to send each block of the FW image.
D8h	MFR_FWUPLOAD_STATUS		R	2	At any time during or after the firmware image upload the system can read this command to determine status of the firmware upload process. All bits get reset to 0 when the power supply enters FW upload mode. Bit 0: "1" full image received Bit 1: "1" full image not received. This remains asserted until the full image is received Bit 2: "1" bad or corrupt image received Bit 3: For future use Bit 4: "1" FW image is not supported and not received Bit 5-15: Reserved
D9h	MFR_FW_REVISION	NA	BR	3	Describes revisions of the FW Block Read with PEC (3 bytes) Byte 0: 0-255 Minor revision, secondary Byte 1: 0-255 Minor revision, primary Byte 3: 0-255 Bit 7: "1" Down grading of PSU FW has to be avoided; "0" no restriction in downgrading the PSU FW Bit 0-6: Major revision

Noted: While the PSU FW image is being updated the PSU will blink the green LED at a 2 Hz rate.

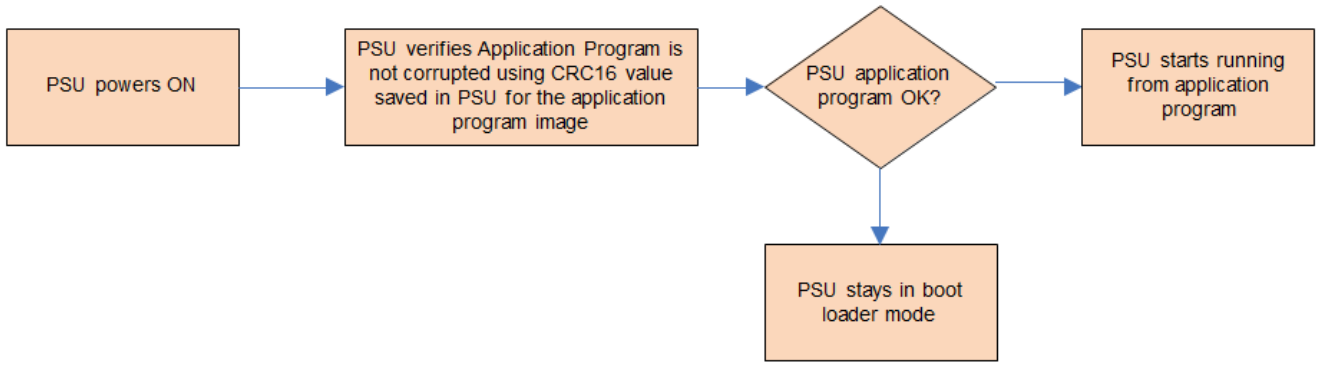
Firmware Update Process

IMPORTANT!

- PSU may be in standby mode or ON mode during FW update process
- If the FW update process is interrupted at any point during the process; the PSU must always be able to return to the boot loader code.
- The PSU must always check that the application program is not corrupted before starting to run from the application program
- During the FW upload process the PSU must always respond to any communication on the bus; acknowledging its address and the supporting commands without holding the bus. For unsupported boot loader commands the PSU may respond with Not Acknowledge or 00h.
- BMC must configure correct addresses into ME at BMC startup to avoid bad PSU address config if AC power is lost or BMC is reset while the PSU update is in progress



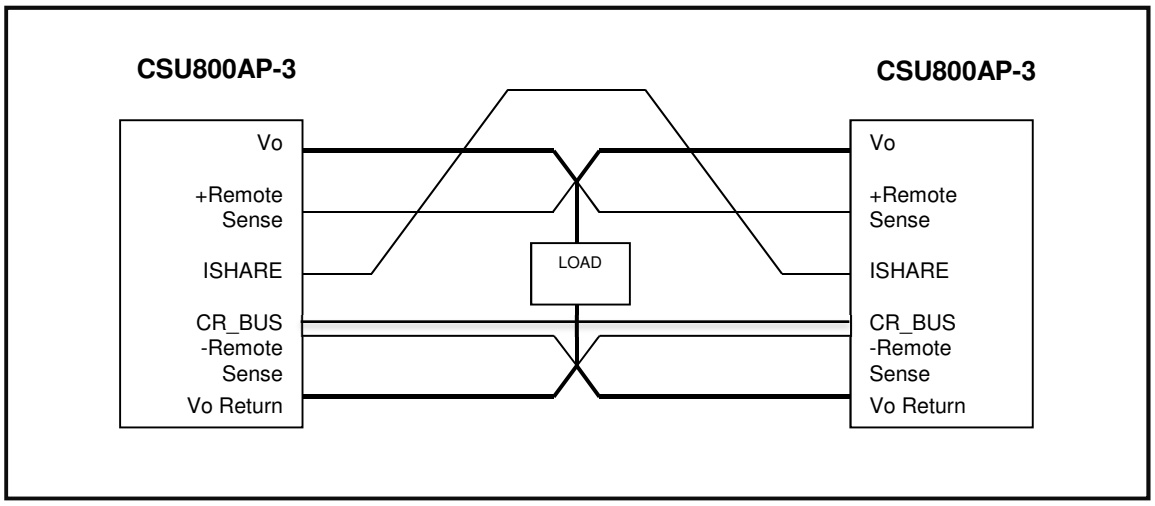
PSU Flow During Powering ON



Application Notes

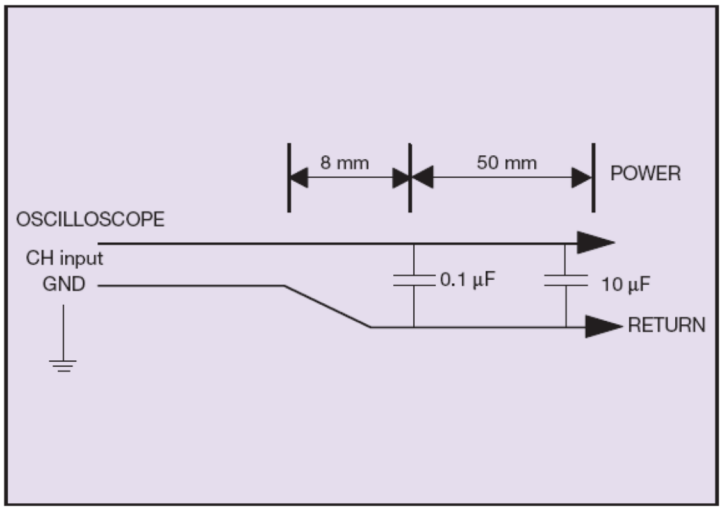
Current Sharing

The CSU800 series' main output V_O is equipped with current sharing capability. This will allow up to 4 power supplies to be connected in parallel for higher power application. Current share accuracy is typically 5% when the load is larger than 50%. When supplying light loads between 20% and 50% of its rated load, the power supplies will share within 10% accuracy. Below 20% total loading, there is no guarantee of output current sharing.



Output Ripple and Noise Measurement

The setup outlined in the diagram below has been used for output voltage ripple and noise measurements on the CSU800 Series. When measuring output ripple and noise, a scope jack in parallel with a 0.1µF ceramic chip capacitor, and a 10µF aluminum electrolytic capacitor should be used. Oscilloscope should be set to 20MHz bandwidth for this measurement



Record of Revision and Changes

Issue	Date	Description	Originators
1.0	11.23.2017	First Issue	A. Li
1.1	03.09.2018	1.Update the Cold redundancy 05h 3. Update Always Standby to Always Cold Standby 2.Update the PSON 4. Update Efficiency Curve 5. Add a diagram to current share section	K. Wang
1.2	08.22.2018	Update the mechanical drawing	K. Wang
1.3	10.29.2018	Update the error for FRU data	K. Wang
1.4	01.18.2019	Update type error form 238 to 230 bytes	K. Wang
1.5	07.02.2019	Update “9Dh” description	K. Wang
1.6	08.11.2019	Add the bootload process	K. Wang
1.7	10.16.2019	Update black box byte to 238	K. Wang
1.8	04.02.2020	Update “19h” description	C.Liu
1.9	04.23.2020	Update “3Ah” description	C.Liu
2.0	05.26.2020	Update safety cert from 60950 to 62368-1	C.Liu

WORLDWIDE OFFICES

Americas
2900 South Diablo Way
Suite B100
Tempe, AZ 85282
USA
+1 888 412 7832

Europe (UK)
Ground Floor Offices
Barberry House, 4 Harbour Buildings
Waterfront West, Brierley Hill
West Midlands, DY5 1LN, UK
+44 (0) 1384 842 211

Asia (HK)
14/F, Lu Plaza
2 Wing Yip Street
Kwun Tong, Kowloon
Hong Kong
+852 2176 3333

ARTESYN™
An Advanced Energy Company
www.artesyn.com

For more information: www.artesyn.com
For support: productsupport.ep@artesyn.com