*Click **here** to ask an associate for production status of specific part numbers.*

MAX20499

Automotive Single 8A/12A Step-Down Converter Family

General Description

The MAX20499 is a family of high-efficiency, synchronous step-down converters that operate with a 3.0V to 5.5V input voltage range and supply a 0.5V to 1.275V output voltage range. The wide input/output voltage range and the ability to provide up to 12A peak output current make this device family ideal for on-board point-of-load and post-regulation applications. The MAX20499 achieves ±1.5% output error over load, line, and temperature ranges.

The MAX20499 features a 2.2MHz fixed-frequency PWM mode for better noise immunity and load-transient response. The 2.2MHz frequency operation allows for the use of all ceramic capacitors and minimizes external components. The spread-spectrum frequency modulation option minimizes radiated electromagnetic emissions. Integrated low $R_{DS(ON)}$ switches improve efficiency at heavy loads and make layout simpler than discrete solutions.

The MAX20499 is offered with factory-preset output voltage. See the *Ordering Information* table for options. The I^2C interface supports dynamic voltage adjustment with programmable slew rates. Other features include programmable soft-start, along with overcurrent and overtemperature protections.

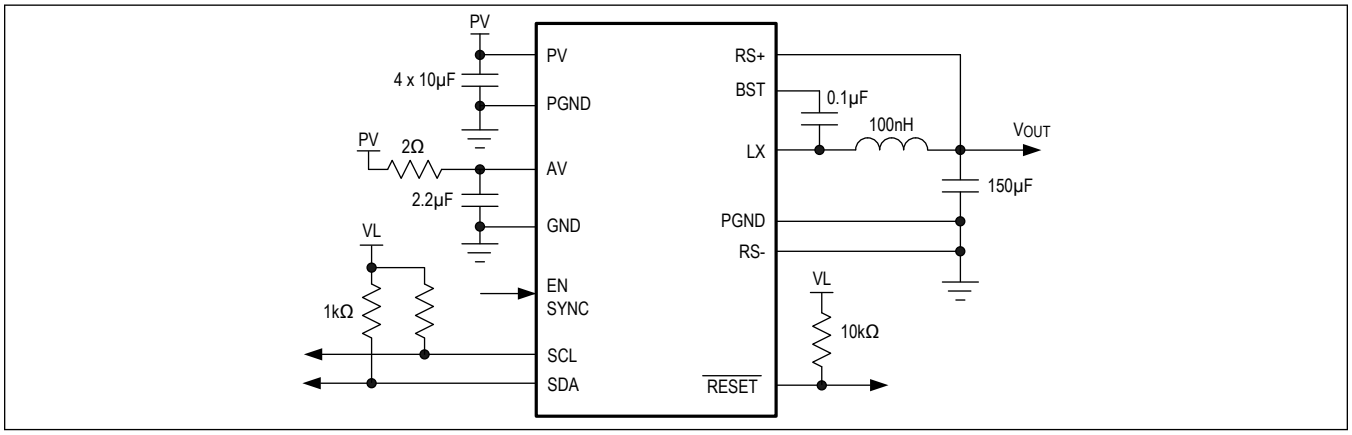
Benefits and Features

- High-Efficiency DC-DC Converter
- Up to 12A Peak Output Current
  - MAX20499A: 8A
  - MAX20499B: 12A
- Differential Remote Voltage Sensing
- 3.0V to 5.5V Operating Supply Voltage
- I^2C-Controlled Output Voltage: 0.5V to 1.275V in 6.25mV Steps
- Excellent Load-Transient Performance
- Programmable Compensation
- 2.2MHz or 1.1MHz Operation
- +1.5% Output Voltage Accuracy
- $\overline{\text{RESET}}$ Output
- Current Mode, Forced-PWM Operation
- Overtemperature and Short-Circuit Protection
- 3.5mm x 3.75mm, 17-Pin, Side-Wettable FC2QFN
- -40°C to +125°C Grade 1 Automotive Temperature Range
- AEC-Q100 Qualified

Applications

- Automotive Entertainment Systems
- SoC Core Power

Simplified Block Diagram



Ordering Information appears at end of data sheet.

19-100613; Rev 7; 5/22

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Absolute Maximum Ratings

PV, AV, EN, $\overline{\text{RESET}}$ to GND ..... -0.3V to +6V
SYNC, RS+, RS- to GND ..... -0.3V to AV+0.3V
SDA, SCL to GND ..... -0.3V to +6V
GND to PGND ..... -0.3V to +0.3V
BST to LX ..... -0.3V to +6V
LX to PGND ..... -0.3V to PV+0.3V
Output Short-Circuit Duration ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
17-FC2QFN (derate 38.5mW/°C > 70°C).....3077mW
Operating Junction Temperature (*Note 4*) .....-40°C to +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (Soldering, 10s).....+300°C
Soldering Temperature (Reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range			-40 to +125	°C

Note: These limits are not guaranteed.

Package Information

17 FC2QFN

Package Code	F173A3FY+2
Outline Number	21-100263
Land Pattern Number	90-100088
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction to Ambient (θ_{JA})	36.2°C/W
Junction to Case (θ_{JC})	8°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	26°C/W
Junction to Case (θ_{JC})	6°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{PV} = V_{AV} = 5V, T_J = -40°C to +150°C, unless otherwise noted (*Note 1*, *Note 2*, *Note 4*), typical values are at T_A = +25°C under normal conditions unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE						
PV Supply Voltage	V_{PV}		3.0		5.5	V
AV Supply Voltage	V_{AV}		3.0		5.5	V

Electrical Characteristics (continued)

(V_{PV} = V_{AV} = 5V, T_J = -40°C to +150°C, unless otherwise noted (Note 1, Note 2, Note 4), typical values are at T_A = +25°C under normal conditions unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO		Rising		2.7	2.9	V
		Falling	2.45	2.6		
Supply Current	I_{IN}	EN = high, I_{OUT} = 0mA, no switching		2.5		mA
Shutdown Supply Current	I_{IN}	EN = low, T_A ≤ +125°C		3	10	µA
PWM FREQUENCY						
PWM Switching Frequency	f_{SW}	Internally generated, CONFIG.FSW = 0	2.0	2.2	2.4	MHz
		Internally generated, CONFIG.FSW = 1	1.0	1.1	1.2	
Spread Spectrum		CONFIG.SS = 1		+3		%
OUTPUT VOLTAGE						
Voltage Accuracy	V_{OUT}	I_{LOAD} = 0A to I_{MAX}, V_{PV} = 3.3V, V_{OUT} = 1.0V	-1		+1	%
		I_{LOAD} = 0A to I_{MAX}, 3.0V ≤ V_{PV} ≤ 5.5V, V_{OUT} = 0.80V to 1.275V	-1.5		+1.5	
		I_{LOAD} = 0A to I_{MAX}, 3.0V ≤ V_{PV} ≤ 5.5V, V_{OUT} < 0.8V	-15		15	mV
OV Threshold Range		V_{OUT} rising	102.5		110	%
OV Threshold Accuracy		Percentage of nominal output, V_{OUT} = V_{SET} (0.8V to 1.275V)	-2		+2	%
		V_{OUT} = V_{SET} (< 0.8V)	-20		20	mV
UV Threshold Range		V_{OUT} falling	97.5		90	%
UV Threshold Accuracy		Percentage of nominal output, V_{OUT} = V_{SET} (0.8V to 1.275V)	-2		2	%
UV/OV Propagation Delay		V_{OUT} = V_{SET}		15		µs
Active Timeout Period		Option 1 (32768 clocks)		14.9		ms
		Option 2 (16384 clocks)		7.4		
		Option 3 (8192 clocks) (default)		3.7		
		Option 4 (1024 clocks)		0.5		
POWER FET						
HS nMOS On-Resistance		V_{PV} = V_{AV} = 5V, I_{LX} = 1A		8		mΩ
LS nMOS On-Resistance		V_{PV} = V_{AV} = 5V, I_{LX} = 1A		4		mΩ
HS nMOS Current-Limit Threshold		MAX20499A (8A) (Note 3)	11	14	17	A
		MAX20499B (12A) (Note 3)	15	18	22	
LX Leakage Current		V_{PV} = V_{AV} = 5V, LX = PGND or PV, T_A = +25°C		1		µA
LX Discharge Resistance		V_{EN} = 0V, I_{LOAD} = 10mA		11		Ω

Electrical Characteristics (continued)

(V_{PV} = V_{AV} = 5V, T_J = -40°C to +150°C, unless otherwise noted (*Note 1*, *Note 2*, *Note 4*), typical values are at T_A = +25°C under normal conditions unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL OVERLOAD						
Thermal Shutdown Temperature		T_J rising		165		°C
Hysteresis				15		°C
DIGITAL OUTPUT ($\overline{RESET}$, SYNC, SDA)						
$\overline{RESET}$ Output Low Level		3.0V ≤ V_{PV} ≤ 5.5V, 3.0V ≤ V_{AV} ≤ 5.5V, I_{SINK} = 2mA			0.4	V
$\overline{RESET}$ High Leakage Current				1		µA
SYNC Output High Level	V_{OH}	I_{SOURCE} = 3mA	4.2			V
SYNC Output Low Level	V_{OL}	I_{SINK} = 3mA			0.4	V
SDA Output Low Level	V_{OL_SDA}	I_{SINK} = 4mA			0.4	V
I^2C INTERFACE						
Clock Frequency					1.0	MHz
Setup Time (Repeated) START	$t_{SU:STA}$		260			ns
HOLD Time (Repeated) START	$t_{HD:STA}$		260			ns
SCL Low Time	t_{LOW}		500			ns
SCL High Time	t_{HIGH}		260			ns
DATA Setup Time	$t_{SU:DAT}$		50			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
Setup Time for STOP Condition	$t_{SU:STO}$		260			ns
Spike Suppression				20		ns
DIGITAL INPUT (SYNC)						
Input High Level	V_{IH}		1.8			V
Input Low Level	V_{IL}				0.4	V
SYNC Input Pull-Down				100		kΩ
SYNC Input Frequency Range		f_{OSC} = 2.2MHz	1.8		2.6	MHz
		f_{OSC} = 1.1MHz	0.9		1.3	
DIGITAL INPUT (EN, SDA, SCL)						
Input High Level			1.3			V
Input Low Level					0.5	V
Input Hysteresis				50		mV
Input Leakage Current				1		µA

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: The device is designed to operate under in-cabin automotive temperature profiles similar to *Typical Operating Characteristics* 1.

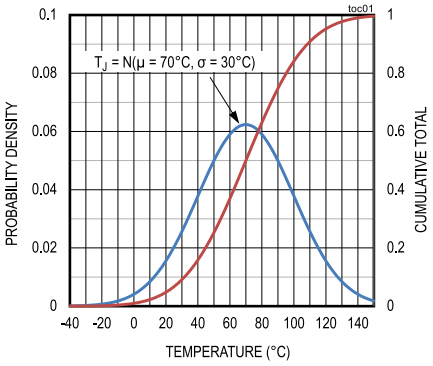
Note 3: Based on ATE measurements using scaled currents.

Note 4: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

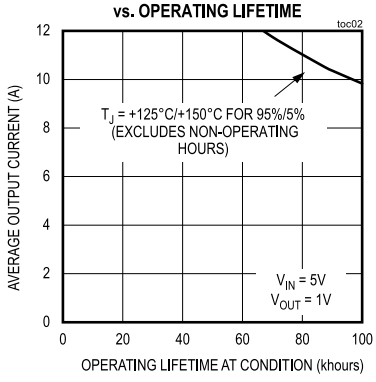
Typical Operating Characteristics

(V_{PV} = V_{AV} = 5V; T_A= +25°C unless otherwise noted)

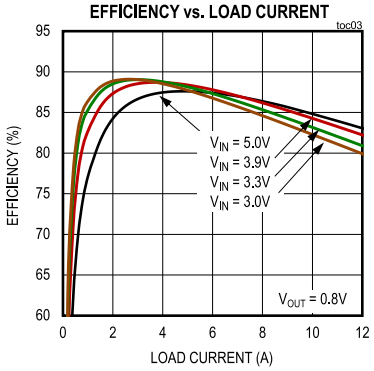
OPERATING TEMPERATURE PROFILE



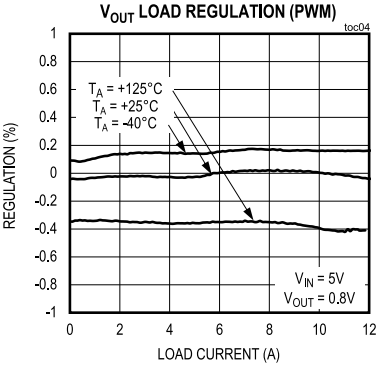
AVERAGE OUTPUT CURRENT vs. OPERATING LIFETIME



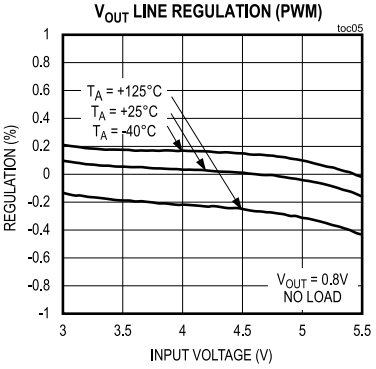
EFFICIENCY vs. LOAD CURRENT



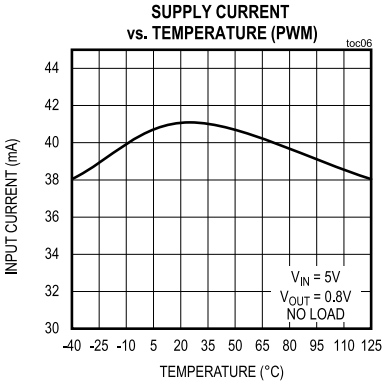
V_{OUT} LOAD REGULATION (PWM)



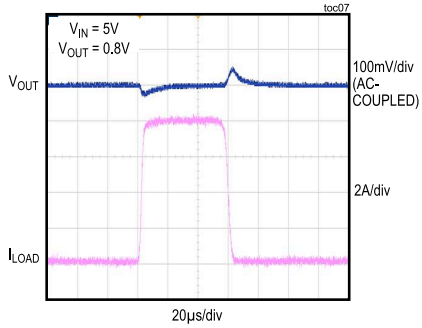
V_{OUT} LINE REGULATION (PWM)



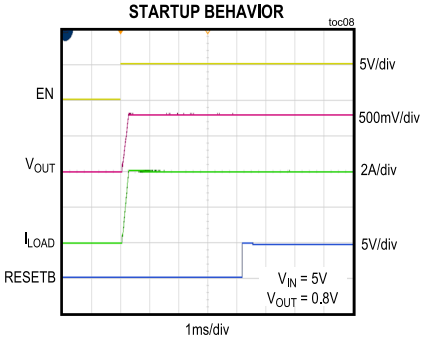
SUPPLY CURRENT vs. TEMPERATURE (PWM)



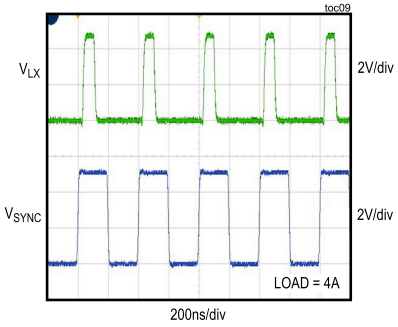
LOAD-TRANSIENT RESPONSE (PWM)



4A LOAD STARTUP BEHAVIOR

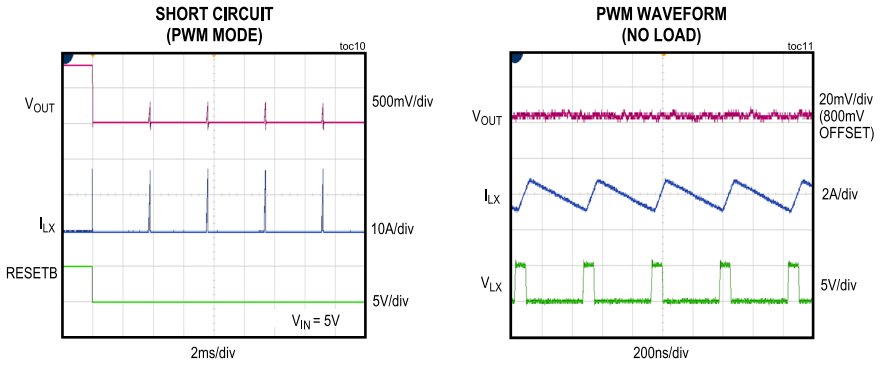


SYNC FUNCTION

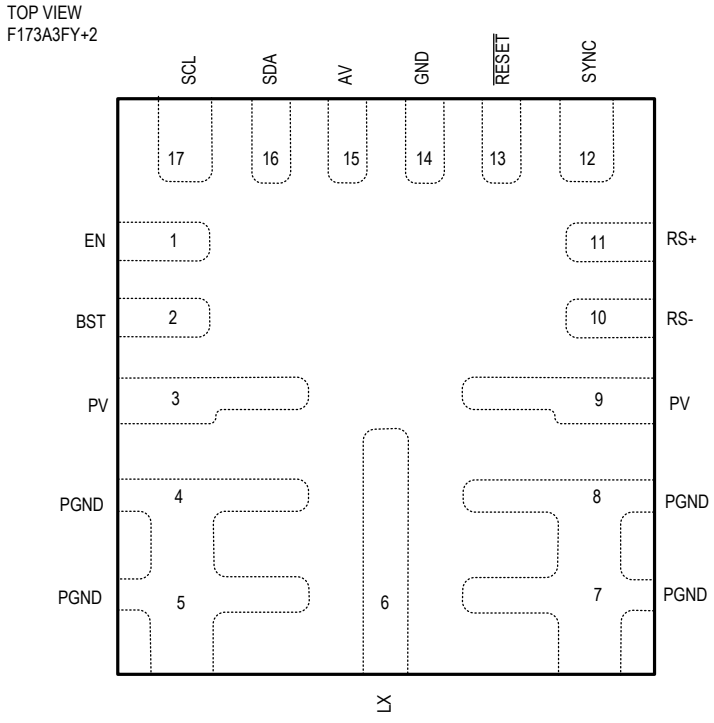


Typical Operating Characteristics (continued)

(V_{PV} = V_{AV} = 5V; T_A= +25°C unless otherwise noted)



Pin Configuration



Pin Description

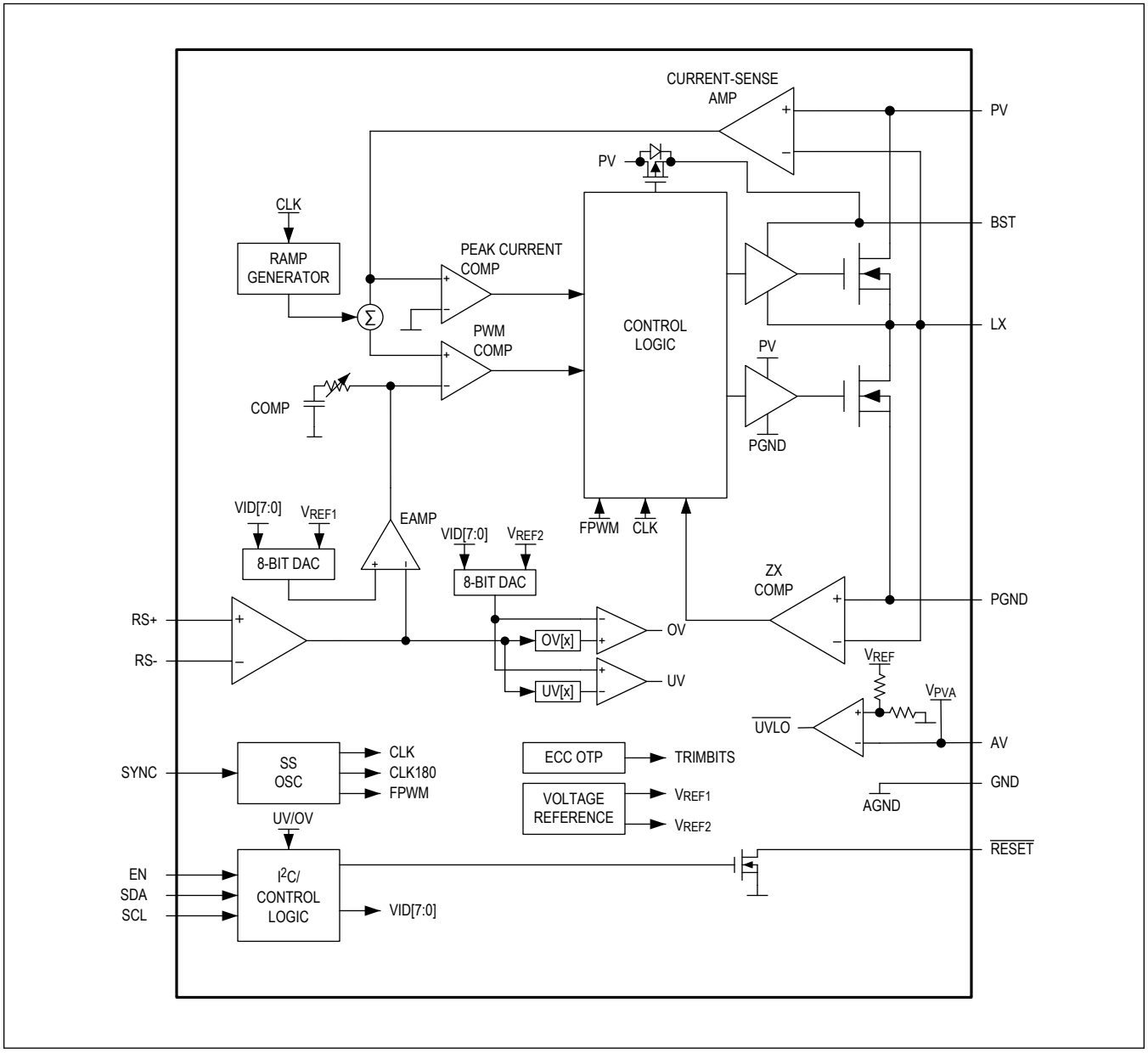
PIN	NAME	FUNCTION
1	EN	Active-High Enable Input. Drive EN HIGH for normal operation. The device enters soft-start on the rising edge and enters soft-shutdown on the falling edge.

Pin Description (continued)

PIN	NAME	FUNCTION
2	BST	Bootstrap Capacitor Connection
3, 9	PV	Power Input Supply. Connect a 10µF or larger ceramic capacitor from PV to PGND. Connect all PV pins together.
4, 5, 7, 8	PGND	Power Ground. Connect all PGND pins together.
6	LX	Inductor Connection. Connect LX to the switched side of the inductor. Connect all LX pins together.
10	RS-	Buck Regulator Remote Voltage-Sense Negative Input
11	RS+	Buck Regulator Remote Voltage-Sense Positive Input
12	SYNC	SYNC I/O. Connect SYNC to AV/GND or an external clock to enable fixed-frequency forced-PWM-mode operation. When configured as an output (CONFIG.SO[1:0] = 2'b10), connect SYNC to the other device's SYNC inputs.
13	$\overline{\text{RESET}}$	Open-Drain $\overline{\text{RESET}}$ Output. This output remains low for the programmed hold time after the output has reached its regulation level (see the *Electrical Characteristics* table). To obtain a logic signal, pull $\overline{\text{RESET}}$ up with an external resistor.
14	GND	Analog Ground
15	AV	Analog Input Supply
16	SDA	I^2C Data I/O
17	SCL	I^2C Clock Input

Functional Diagrams

Internal Block Diagram



Detailed Description

The MAX20499 is a high-efficiency, synchronous step-down converter that operates with a 3.0V to 5.5V input voltage range and provides a 0.50V to 1.275V output voltage range. The device delivers up to 12A of load current and regulates the output voltage over load, line, and temperature ranges.

Optional spread-spectrum frequency modulation minimizes radiated electromagnetic emissions caused by the switching frequency. The I²C-programmable I/O (SYNC) enables system synchronization.

Integrated low $R_{DS(ON)}$ switches help improve efficiency at heavy loads and make layout much simpler with respect to discrete solutions. The device is offered with a factory-preset output voltage that is dynamically adjustable through the I²C interface. The output voltage can be set to any desired value from 0.5V to 1.275V, in 6.25mV steps.

Additional features include adjustable soft-start, power-good delay, DVS rate, overcurrent, and overtemperature protections. See the *Internal Block Diagram*.

I²C Interface

The MAX20499 features an I²C, 2-wire serial interface that consists of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX20499 and the controller at clock rates up to 1MHz. The controller, typically a microcontroller, generates SCL and initiates data transfer on the bus. Figure 1 shows the 2-wire interface timing diagram.

A controller device communicates with the MAX20499 by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX20499 SDA line operates as both an input and an open-drain output. A pull-up resistor greater than 500Ω is required on the SDA bus. The MAX20499 SCL line operates as an input only. A pull-up resistor greater than 500Ω is required on SCL if there are multiple controllers on the bus, or if the controller in a single-controller system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation, even on a noisy bus.

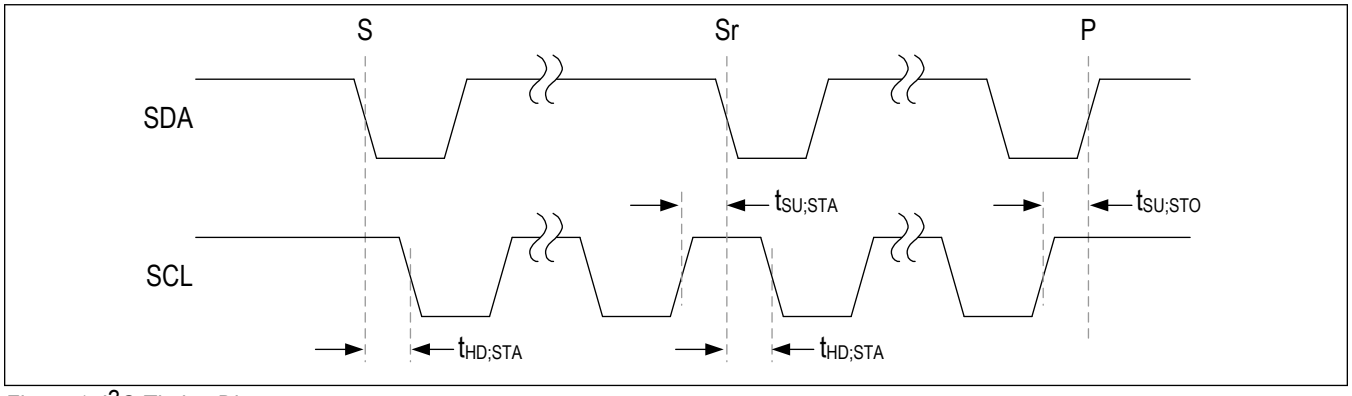


Figure 1. I²C Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *STOP and START Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

STOP and START Conditions

A controller device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (see Figure 1). A START (S) condition from the controller signals the beginning of a transmission to the MAX20499. The controller terminates

transmission and frees the bus by issuing a STOP (P) condition. The bus remains active if a REPEATED START (Sr) condition is generated instead of a STOP condition.

Early STOP Condition

The MAX20499 recognizes a STOP condition at any point during data transmission unless the STOP condition occurs in the same high pulse as a START condition.

Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the controller device. The I²C specification allows slow target devices to alter the clock signal by holding down the clock line, a process known as clock stretching. The MAX20499 does not use any form of clock stretching to hold down the clock line.

I²C General Call Address

The MAX20499 does not implement the I²C specifications general call address. If the MAX20499 sees the general call address (0b0000_0000), it will not issue an acknowledge.

Target Address

The address is defined as the seven most significant bits (MSbs) followed by the R/W bit. Set the R/W bit to 1 to configure the devices to read mode. Set the R/W bit to 0 to configure the devices to write mode. The address is the first byte of information sent to the devices after the START condition. The target address is factory preset (see the *Ordering Information* table for the 7-bit address for each version). The factory-programmable I²C addresses are 0x38 through 0x3F.

Acknowledge

The acknowledge bit (ACK) is a clocked ninth bit that the device uses to handshake receipt of each byte of data (see Figure 2). The device pulls down SDA during the controller-generated ninth clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus controller can reattempt communication.

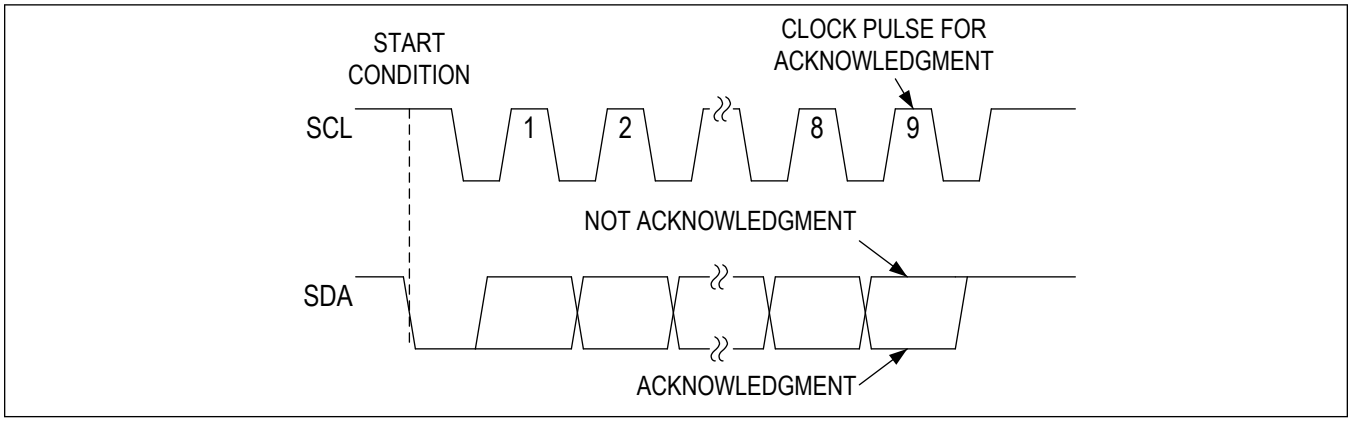


Figure 2. Acknowledge Condition

Write-Data Format

A write to the device includes transmission of the following:

- START condition
- Target address with the write bit set to 0
- 1 byte of data to the register address
- 1 byte of data to the command register

- STOP condition

Figure 3 illustrates the proper format for one frame.

Read-Data Format

A read from the device includes transmission of the following:

- START condition
- Target address with the write bit set to 0
- 1 byte of data to the register address
- Restart condition
- Target address with read bit set to 1
- 1 byte of data to the command register
- STOP condition

Figure 3 illustrates the proper format for one frame.

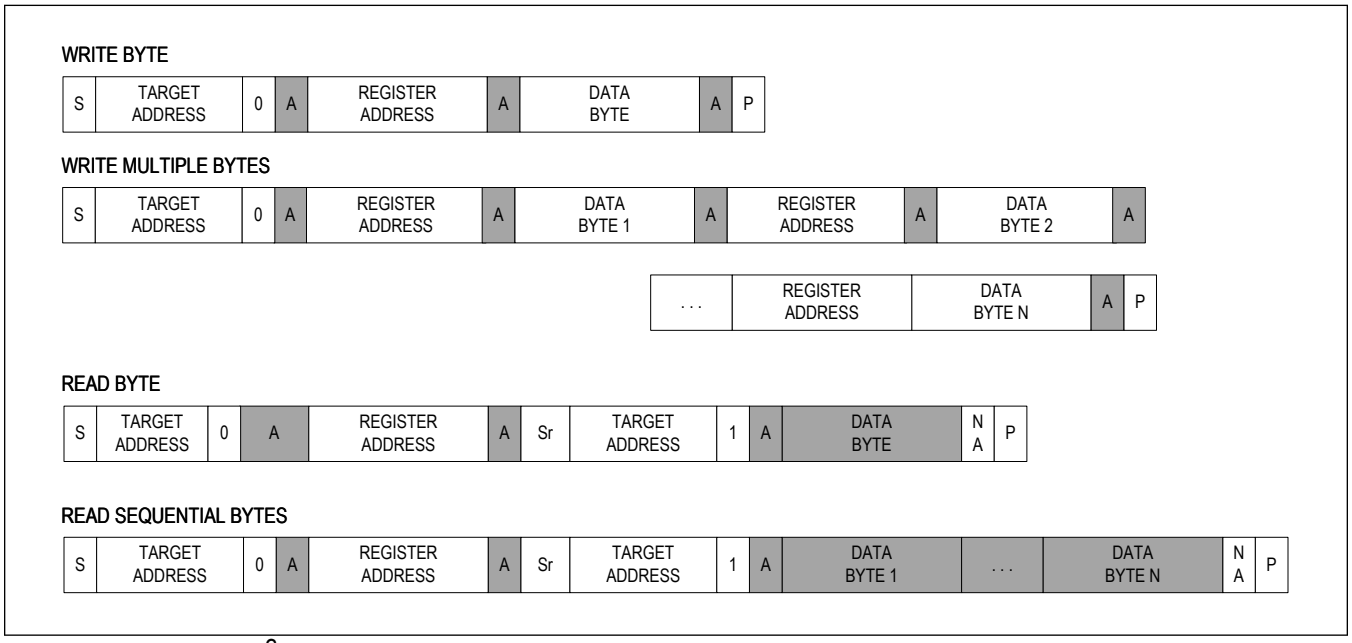


Figure 3. Data Format of I²C Interface

Writing to a Single Register

Figure 4 shows the protocol for the I²C controller device to write 1 byte of data to the MAX20499. This protocol is the same as the SMBus specification's write-byte protocol.

The write-byte protocol is as follows:

1. The controller sends a START command (S).
2. The controller sends the 7-bit target address followed by a write bit (R/nW = 0).
3. The addressed target asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The controller sends an 8-bit register pointer.
5. The target acknowledges the register pointer.
6. The controller sends a data byte.
7. The target updates with the new data.
8. The target sends ACKNOWLEDGE or NOT ACKNOWLEDGE for the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
9. The controller sends a STOP condition (P) or a REPEATED START condition (Sr).

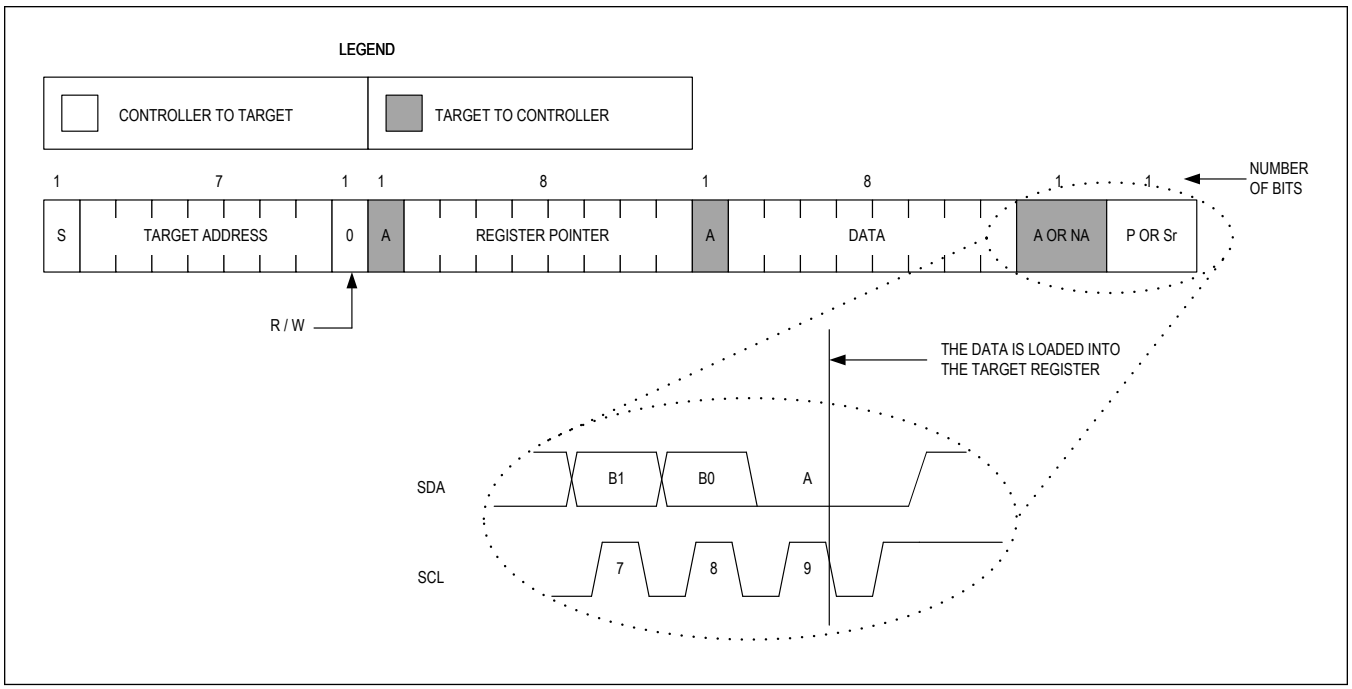


Figure 4. Write-Byte Format

Writing Multiple Bytes Using Register-Data Pairs

Figure 5 shows the protocol for the I²C controller device to write multiple bytes to the MAX20499 using register-data pairs. This protocol allows the I²C controller device to address the target only once and then send data to multiple registers in a random order. Registers may be written continuously until the controller issues a STOP condition.

The multiple-byte register-data pair protocol is as follows:

1. The controller sends a START command.
2. The controller sends the 7-bit target address, followed by a write bit.
3. The addressed target asserts an ACKNOWLEDGE by pulling SDA low.
4. The controller sends an 8-bit register pointer.
5. The target acknowledges the register pointer.
6. The controller sends a data byte.
7. The target acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
8. Steps 5 through 7 are repeated as many times as the controller requires.
9. The controller sends a STOP condition. During the rising edge of the STOP-related SDA edge, the data byte that was previously written is loaded into the target register and becomes active.

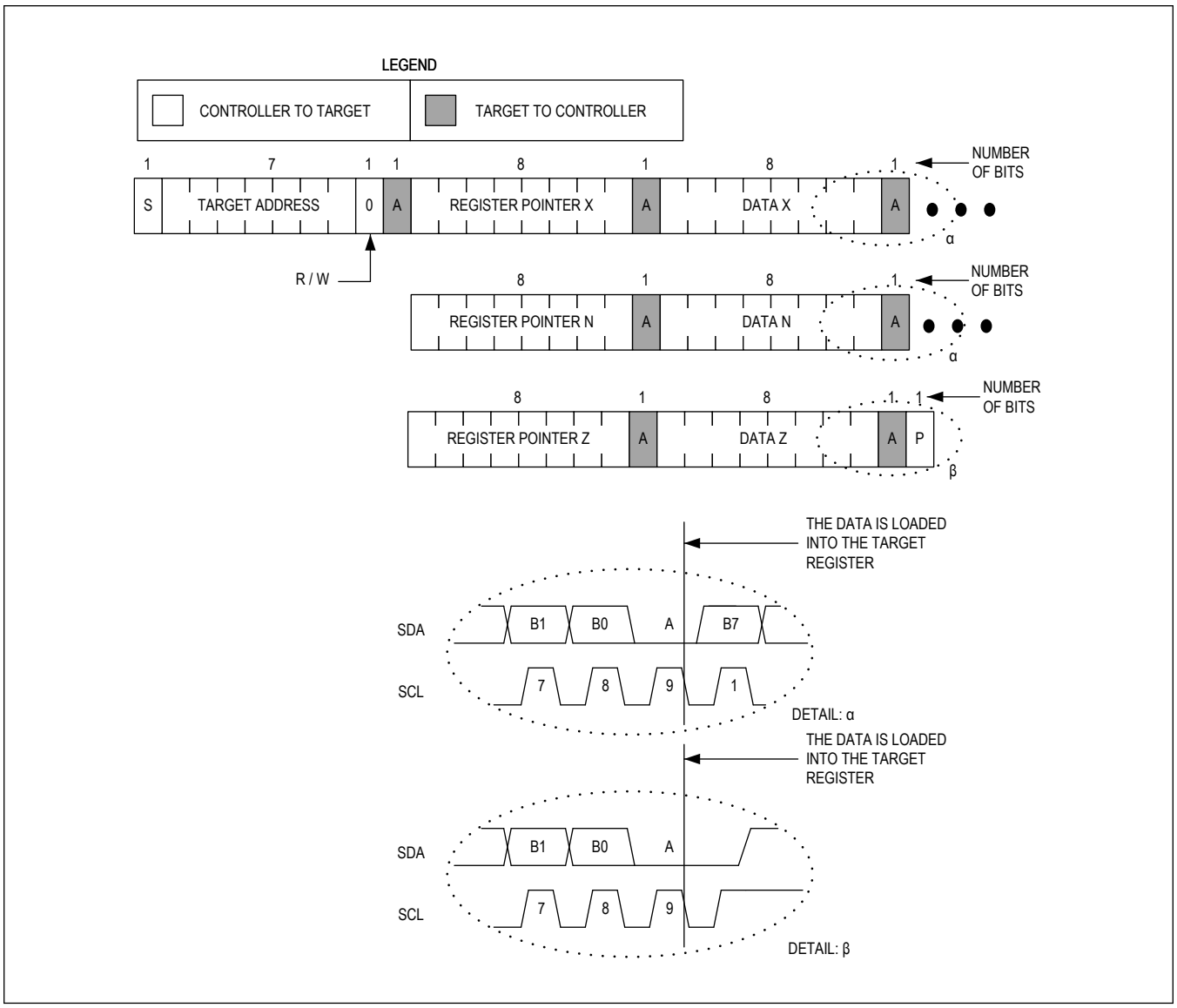


Figure 5. Write Register-Data Pair Format

Reading a Single Register

Figure 6 shows the protocol for the I2C controller device to read 1 byte of data from the MAX20499.

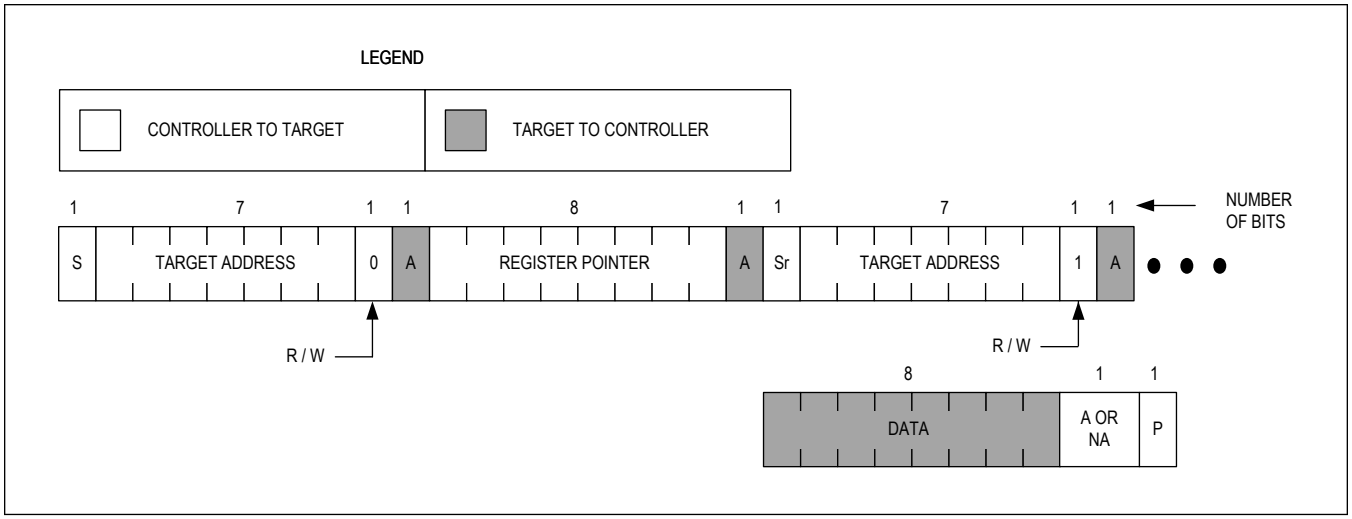


Figure 6. Read-Byte Format

Reading Multiple Bytes

Figure 7 shows the protocol for the I²C controller device to read multiple bytes sequentially from the MAX20499.

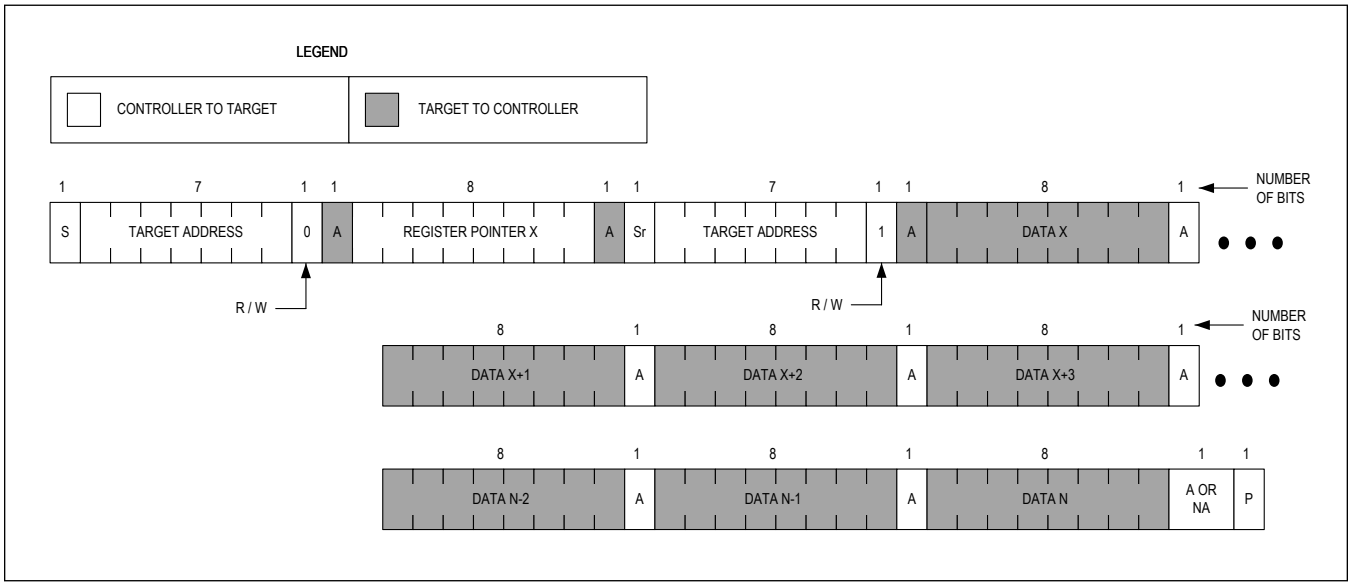


Figure 7. Sequential-Read Format

$\overline{\text{RESET}}$ Output

The MAX20499 features an open-drain $\overline{\text{RESET}}$ output that asserts when the output voltage deviates from the target regulated voltage by a programmed amount. $\overline{\text{RESET}}$ remains asserted for a fixed timeout period after the output is within the programmed regulation window. Connect $\overline{\text{RESET}}$ to a pull-up resistor.

Soft-Start

The MAX20499 includes a programmable soft-start feature to limit startup inrush current by forcing the output voltage to slowly ramp up towards its regulation point. The soft-start slew rate is set in the SLEW register.

Dynamic Voltage Scaling

The step-down regulator features dynamic voltage scaling (DVS) to allow loads to margin their supply voltage. The output voltage is set with VID[7:0]. The slew rate during DVS is adjustable with SR[3:0] in the SLEW register. The OV/UV comparators are masked to prevent false $\overline{\text{RESET}}$ assertions during the DVS period.

Shutdown

During shutdown, the output voltage is ramped down at the programmed soft-start slew rate. After the soft-shutdown is complete, an 11Ω pull-down resistor is enabled to discharge the remaining output voltage.

Spread-Spectrum Option

The MAX20499 featuring spread-spectrum (SS) operation varies the internal operating frequency by +3% relative to the internally generated operating frequency of 2.2MHz or 1.1MHz (typ). This function does not apply to externally applied clock.

Synchronization (SYNC)

SYNC is factory-programmable I/O. When SYNC is configured as an input, a logic-high on PWM enables SYNC to accept a signal frequency in the range of 1.8MHz < f_{SYNC} < 2.6MHz (CONFIG.FSW = 0) or 0.9MHz < f_{SYNC} < 1.3MHz (CONFIG.FSW = 1) . When SYNC is configured as an output, SYNC outputs the internal PWM switching frequency.

Current Limit/Short-Circuit Protection

The MAX20499 features a current limit that protects the device against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side MOSFET will reach the high-side MOSFET's current-limit threshold and turn off. The converter then turns on the low-side MOSFET to allow the inductor current to ramp down. Once the inductor current falls below the low-side MOSFET valley current-limit threshold, the converter allows the high-side MOSFET to turn on again. This cycle repeats until the short-circuit or overload condition is removed.

Boost Refresh

When the device is enabled, the bootstrap capacitor must be charged by turning on the low-side FET before initiating soft-start.

Overtemperature Protection

Thermal overload protection limits the total power dissipation in the MAX20499. When the junction temperature exceeds +165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C.

Register Map

IC

ADDRESS	NAME	MSB							LSB
Customer_I2C									
0x00	ID[7:0]	DEV[3:0]				RevID[3:0]			
0x02	VIDMAX[7:0]	VMAX[7:0]							
0x03	CONFIG2[7:0]	PROT	–	–	–	–	–	–	–
0x04	STATUS[7:0]	–	INTERR	VRHOT	UV	OV	OC	VMERR	--
0x05	CONFIG[7:0]	–	FSW	–	–	RSVD	SS	SO[1:0]	
0x06	SLEW[7:0]	–	–	–	–	SR[3:0]			
0x07	VID[7:0]	VID[7:0]							
0x08	COMP[7:0]	ENFFZ	FFGM[1:0]		FFZ	RCOMP[3:0]			
0x09	OVUV[7:0]	OV[3:0]				UV[3:0]			

Register Details

ID (0x00)

BIT	7	6	5	4	3	2	1	0
Field	DEV[3:0]				RevID[3:0]			
Reset	0x6				0x1			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
DEV	7:4	Device ID 0x6
RevID	3:0	Revision ID Pass2 = 0x1

VIDMAX (0x02)

BIT	7	6	5	4	3	2	1	0
Field	VMAX[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VMAX	7:0	Max VID Setting	Valid range for VMAX[7:0] is 41 to 165 (0.5V to 1.275V). $VOUT_{MAX}$ = 0.24375 + VMAX[7:0] x 6.25mV

CONFIG2 (0x03)

BIT	7	6	5	4	3	2	1	0
Field	PROT	–	–	–	–	–	–	–
Reset	OTP	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
PROT	7	Register Protection Bit. If this bit is set to 1 in OTP, then writes are always ignored. If set to 0 in OTP, then register writes can be enabled by setting this bit to 0 through the I^2C.	0 = Do not block register writes. 1 (OTP) = Block all register writes. 1 (User) = Block all register writes except to CONFIG2.

STATUS (0x04)

BIT	7	6	5	4	3	2	1	0
Field	–	INTERR	VRHOT	UV	OV	OC	VMERR	--
Reset	–							
Access Type	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
INTERR	6	Internal Error Detected. This bit is set when one or more of the following errors are detected: OV/UV BIST Error GOK (Ground Check) Error Redundant VID Register Error	0 - No internal error 1 - Internal error detected
VRHOT	5	Thermal Shutdown Indication	0 - No thermal shutdown has occured 1 - Thermal shutdown has occured since last read
UV	4	Output Undervoltage	0 - No undervoltage detected 1 - An undervoltage condition is detected
OV	3	Output Overvoltage	0 - No overvoltage detected 1 - An overvoltage condition is detected
OC	2	Output Overcurrent	0 - No overcurrent detected 1 - An overcurrent was detected since the last read
VMERR	1	VID Error	0 - No VID error detected 1 - VID was set higher than VID_{MAX}
--	0	Reserved	

CONFIG (0x05)

BIT	7	6	5	4	3	2	1	0
Field	–	FSW	–	–	RSVD	SS	SO[1:0]	
Reset	–	OTP	–	–	–	OTP	OTP	
Access Type	–	Write, Read	–	–	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
FSW	6	Switching Frequency Selection. Do not change while the output is enabled.	0 - 2.2MHz 1 - 1.1MHz
RSVD	3	Reserved. This bit must always be set to 1.	
SS	2	Spread-Spectrum Clock Setting	0 - Disabled 1 - Enabled. Clock has +3% spread
SO	1:0	SYNC I/O Select	00 - Input, rising edge starts cycle 01 - Input, falling edge starts cycle 10 - Output, falling edge starts cycle 11 - Unused

SLEW (0x06)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SR[3:0]			
Reset	–	–	–	–	OTP			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
SR	3:0	Slew Rate Selection	VALUE = Soft-start/DVS slew rates (mV/µs) 0000 = 14 / 14 0001 = 7 / 14 0010 = 3.4 / 14 0011 = 7 / 7 0100 = 3.4 / 7 0101 = 14 / 14 0110 = 14 / 14 0111 = 7 / 14 1000 = 3.4 / 14 1001 = 3.4 / 3.4

VID (0x07)

BIT	7	6	5	4	3	2	1	0
Field	VID[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VID	7:0	Output Voltage Setting	Valid range for VID[7:0] is 41 to 165 (0.5V to 1.275V). V_{OUT} = 0.24375 + VID[7:0] x 6.25mV

COMP (0x08)

BIT	7	6	5	4	3	2	1	0
Field	ENFFZ	FFGM[1:0]		FFZ	RCOMP[3:0]			
Reset	OTP	OTP		OTP	OTP			
Access Type	Write, Read	Write, Read		Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
ENFFZ	7	Enable FF Zero	0 - Disable FF zero 1 - Enable FF zero
FFGM	6:5	FF Gm Selection	00 - 30µS 01 - 63µS 10 - 90µS 11 - 113µS
FFZ	4	FF Zero	0 - 300kΩ zero at lower frequency 1 - 80kΩ zero at higher frequency
RCOMP	3:0	Compensation Resistor. The compensation resistor is programmable from 35kΩ to 297.5kΩ in 17.5kΩ steps.	RC = 35kΩ + 17.5kΩ x RCOMP[3:0]

OVUV (0x09)

BIT	7	6	5	4	3	2	1	0
Field	OV[3:0]				UV[3:0]			
Reset	OTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
OV	7:4	Overvoltage Threshold Setting	$OV_{THRESHOLD}$ = 102.5% + 0.5% x OV[3:0]
UV	3:0	Undervoltage Threshold Setting	$UV_{THRESHOLD}$ = 97.5% - 0.5% x UV[3:0]

Applications Information

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit switching.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}(V_{PV} - V_{OUT})}}{V_{PV}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{PV} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)} / 2$.

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input voltage ripple consists of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{PV} - V_{OUT}) \times V_{OUT}}{V_{PV} \times f_{SW} \times L}$$

and

$$C_{IN} = \frac{I_{OUT} \times D(1 - D)}{\Delta V_Q \times f_{SW}} \text{ and } D = \frac{V_{OUT}}{V_{PV}}$$

I_{OUT} is the maximum output current; D is the duty cycle.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX20499: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the maximum output current capability of the output. A lower inductor value minimizes size and cost, improves large-signal and transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output-voltage ripple for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ripple current. Resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels, especially when the inductance is increased without also allowing for larger inductor dimensions. The MAX20499 is designed for ΔI_{P-P} equal to 20% to 40% of the full load current. Use the following equation to calculate the inductance:

$$L_{MIN1} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times I_{MAX} \times 40\,\%}$$

V_{IN} and V_{OUT} are typical values so that efficiency is optimum for typical conditions. The switching frequency is typically 2.2MHz or 1.1MHz. The maximum output capability is 8A or 12A, based on the specific part number of the device. See the *Output Capacitor* section to verify that the worst-case output ripple is acceptable. The inductor saturation current is also important for avoiding runaway current during continuous-output short circuit.

Table 1. Inductor Selection Parameters

PARAMETER	DESCRIPTION

Table 1. Inductor Selection Parameters (continued)

V_{IN}	Nominal input voltage (3.3V or 5V, typ)
V_{OUT}	Nominal output voltage
L_{TOL}	Inductor tolerance (±20%, typ)
I_{MAX}	8A or 12A, depending on part number
f_{SW}	Operating frequency. This value is 2.2MHz or 1.1MHz unless externally synchronized to a different frequency.

$L_{MIN} = (1 + L_{TOL}) \times L_{MIN1}$

The maximum recommended inductor value is 2 times the chosen value from the above formula.

$L_{MAX} = 2.0 \times L_{MIN}$

Select a nominal inductor value based on the following formula. For optimal load transient performance select the first standard inductor value greater than L_{MIN}:

$L_{MIN} < L_{NOM} < L_{MAX}$

Table 2. Recommended Inductor Values

V_{IN}	V_{OUT}	I_{MAX}	L_{MIN}	L_{MAX}	RECOMMENDED
3.3V	1V	8A	100nH	200nH	100nH, 150nH
3.3V	1V	12A	70nH	140nH	70nH, 80nH, 100nH

Inductors are rated for maximum saturation current. The maximum inductor current equals the maximum load current in addition to half of the peak-to-peak ripple current

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

The actual peak-to-peak inductor ripple current is calculated in the ΔI_L equation above.

The saturation current should be larger than I_{PEAK}, or at least in a range where the inductance does not degrade significantly.

Output Capacitor

The compensation is programmable to allow application-specific optimization between output capacitance and AC performance. The typical output capacitor range is 100µF (typ) to 500µF (typ). Using the default COMP value of 0xE2, the following equation provides a good starting point:

$$C_{OUTNOM} = 15 \times I_{OUTMAX} \times \frac{R_{COMP}}{70K\Omega} \times \frac{\mu sec}{V}$$

Where I_{OUTMAX} is 8A or 12A, depending on the part number.

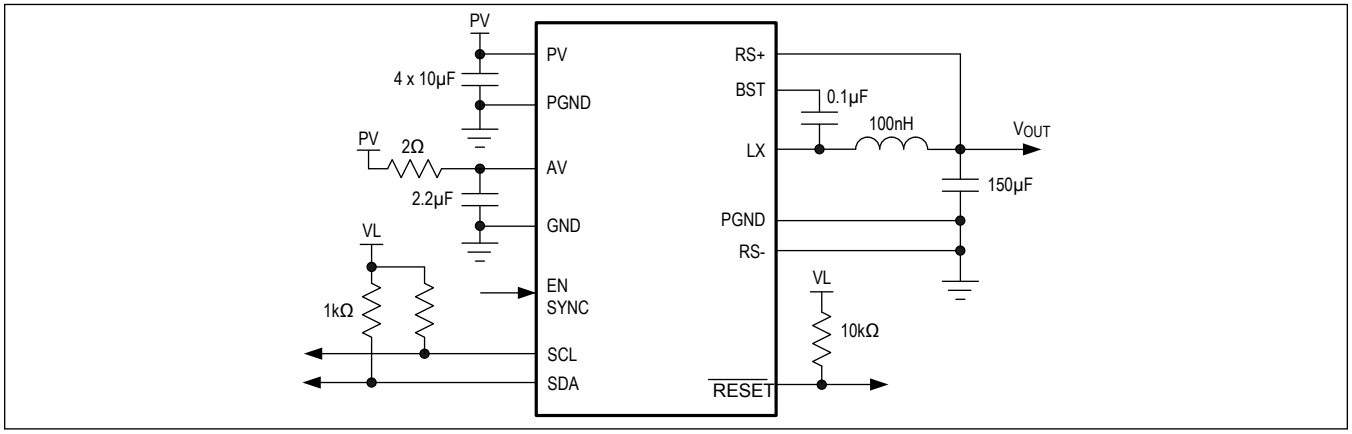
This places the unity gain bandwidth at approximately 200kHz, which is at the peak of the phase boost and results in the best phase margin. Phase margin can be traded for a lower output capacitance from this point. Always measure the phase margin with the fully derated output capacitance to ensure stability.

Programmable Compensation

The device has a programmable zero, along with a programmable compensation resistor. In most cases, the zero should be enabled with the g_m set to 113µS and resistance set at 300kΩ. This provides the largest phase boost possible and allows the highest crossover frequency. This is done by setting the upper nibble of the COMP register to 0xE. The compensation resistor is set based on the application requirements. A higher value resistance results in increased AC performance and an increased output-capacitor requirement, while a lower compensation resistance results in a decrease in AC performance with a lower output-capacitance requirement.

It is recommended that the compensation optimization be completed on the application PCB to account for PCB parasitics when trying to maximize AC performance and/or minimize output capacitance.

Typical Application Circuits



Ordering Information

PART	I_{OUT}	V_{OUT}	V_{MAX}	SLEW	COMP	CONFIG	CONFIG2	OVUV	RESET HOLD	I^2C
MAX20499AFOB/VY+	8A	0.85V	0.85V	0x03	0xE5	0x08	0x80	0x77	0.5ms	0x3A
MAX20499AFOE/VY+	8A	1V	1.275V	0x09	0xEF	0x0C	0x00	0xBB	7.4ms	0x38
MAX20499AFOG/VY+	8A	0.8125V	0.8125V	0x09	0xE6	0x0C	0x00	0xFF	7.4ms	0x38
MAX20499BFOF/VY+	12A	0.85V	1.275V	0x09	0xE3	0x08	0x00	0xBB	3.7ms	0x39
MAX20499BFOG/VY+*	12A	1.1V	1.1V	0x09	0xEF	0x0C	0x00	0xFF	7.4ms	0x38
MAX20499BFOH/VY+	12A	1V	1.275V	0x09	0xEA	0x0C	0x00	0xBB	7.4ms	0x38
MAX20499BFOI/VY+	12A	0.9V	1.01875V	0x03	0xE5	0x08	0x00	0x77	0.5ms	0x38
MAX20499BFOL/VY+	12A	0.8V	1V	0x09	0xE2	0x08	0x00	0x33	0.5ms	0x3B
MAX20499BFOM/VY+	12A	0.9V	1.01875V	0x03	0xE3	0x08	0x00	0xFF	0.5ms	0x38
MAX20499BFON/VY+	12A	0.825V	0.9V	0x03	0xE3	0x08	0x00	0xFF	0.5ms	0x36
MAX20499BFOO/VY+	12A	1V	1.275V	0x09	0xEF	0x0C	0x00	0xBB	7.4ms	0x38

/VY+ Denotes side-wettable automotive-qualified parts.

+ Indicates a lead (Pb)-free/RoHS-compliant package.

** Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/19	Initial release	—
1	8/19	Updated Electrical Characteristics Note 1 and removed future-product status from MAX20499AFOE/VY+ in Ordering Information	9, 28
2	1/20	Updated Pin Description, Register Map, Applications Information, and Ordering Information	12, 22, 25, 27, 28
3	3/21	Updated package name in Absolute Maximum Ratings and Package Information. Y+ COMP setting updated to 0xEA in Ordering Information. Added MAX20499BFOI/VY+, MAX20499BFOL/VY+, MAX20499BFOM/VY+ and MAX20499BFON/VY+ to Ordering Information.	6, 27
4	12/21	Updated Ordering Information to remove future product notation from MAX20499BFOL/VY+, MAX20499BFOM/VY+, and MAX20499BFON/VY+; added MAX20499BFOO/VY+	27
5	1/22	Updated Ordering Information to remove future product notation from MAX20499AFOB/VY+	27
6	5/22	Updated Ordering Information to remove future product notation from MAX20499BFOI/VY+ and add MAX20499BFOF/VY+	27
7	5/22	Updated Ordering Information to remove future product notation from MAX20499BFOF/VY+ and MAX20499BFOO/VY+	27