

### FEATURES

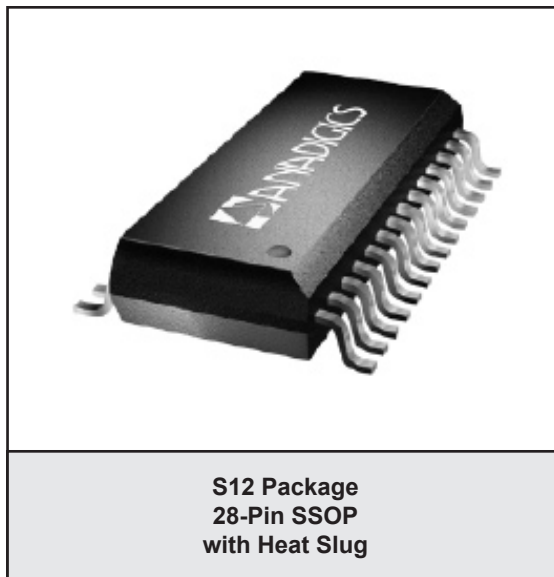
- Low cost integrated amplifier with Step Attenuator
- Attenuation Range: 0 - 59 dB, adjustable in 1 dB increments via a 3-wire Serial Control
- Meets DOCSIS distortion requirements at a +60 dBmV output signal level
- Low distortion and low noise
- Frequency range: 5 - 100 MHz
- 5 Volt Operation
- -40 to +85 °C temperature range
- RoHS Compliant Package Option

### APPLICATIONS

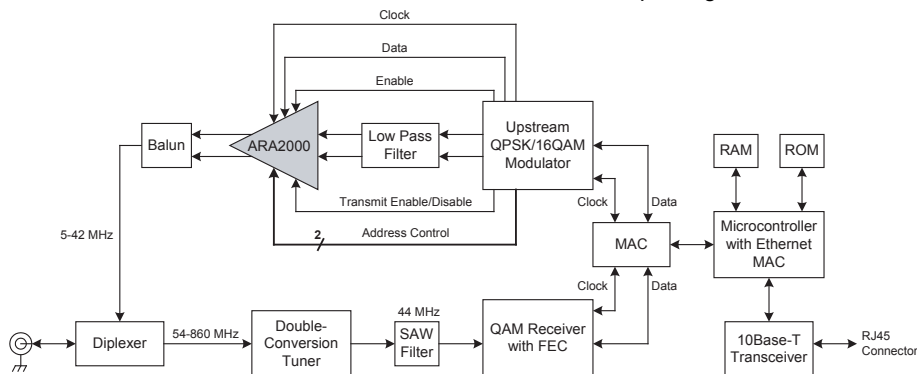
- MCNS/DOCSIS Compliant Cable Modems
- CATV Interactive Set-Top Box
- Telephony over Cable Systems
- OpenCable Set-Top Box
- Residential Gateway

### PRODUCT DESCRIPTION

The ARA2004 is designed to provide the reverse path amplification and output level control functions in a CATV Set-Top Box or Cable Modem. It incorporates a digitally controlled precision step attenuator that is preceded by an ultra low noise amplifier stage, and followed by an ultra-linear output driver amplifier. This device uses a balanced circuit design that exceeds the MCNS/DOCSIS requirement for harmonic performance



at a +60 dBmV output level while only requiring a single polarity +5 V supply. Both the input and output are matched to 75 ohms with an appropriate transformer. The precision attenuator provides up to 58 dB of attenuation in 1 dB increments via a three-wire serial interface. With external passive components, this device meets IEC 1000-4-12 and ANSI/IEEE C62.41-1991 100KHz ringwave tests, as well as IEC1000-4-5 1.2/50  $\mu$ S surge tests. The ARA2004 is offered in a 28-pin SSOP package featuring a heat slug on the bottom of the package.



**Figure 1: Functional Block Diagram for DOCSIS 3.0 Application**

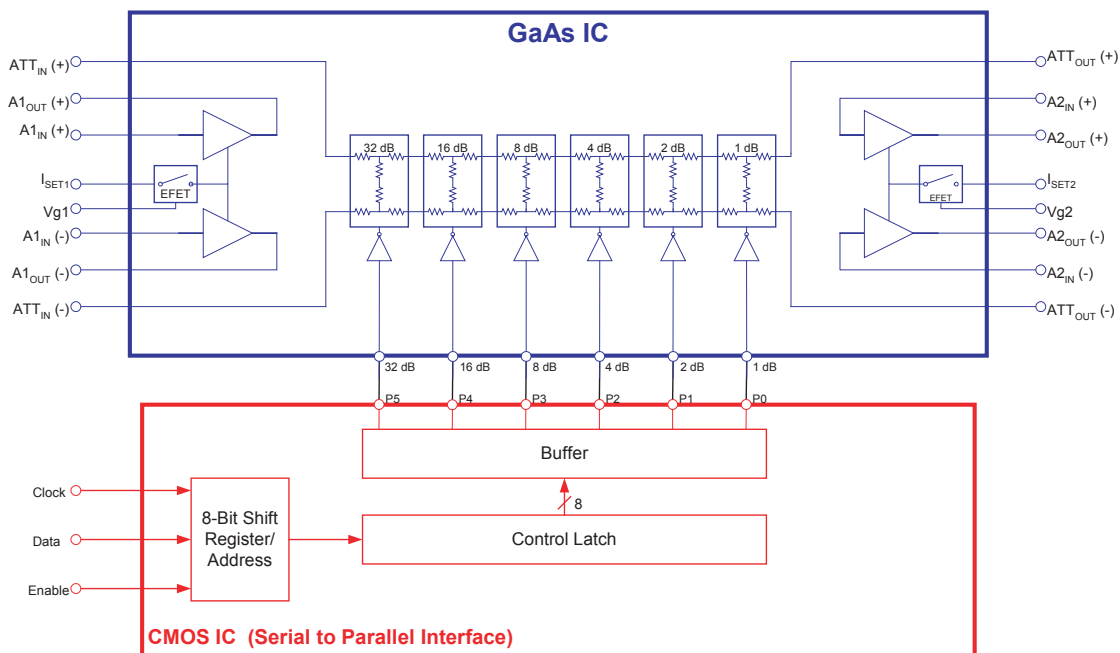


Figure 2: Functional Block Diagram

|    |                       |                        |    |
|----|-----------------------|------------------------|----|
| 1  | GND                   | GND                    | 28 |
| 2  | V <sub>ATTN</sub>     | N/C                    | 27 |
| 3  | ATT <sub>IN</sub> (+) | ATT <sub>OUT</sub> (+) | 26 |
| 4  | A1 <sub>OUT</sub> (+) | A2 <sub>IN</sub> (+)   | 25 |
| 5  | A1 <sub>IN</sub> (+)  | A2 <sub>OUT</sub> (+)  | 24 |
| 6  | Vg1                   | Vg2                    | 23 |
| 7  | I <sub>SET1</sub>     | I <sub>SET2</sub>      | 22 |
| 8  | A1 <sub>IN</sub> (-)  | A2 <sub>OUT</sub> (-)  | 21 |
| 9  | A1 <sub>OUT</sub> (-) | A2 <sub>IN</sub> (-)   | 20 |
| 10 | ATT <sub>IN</sub> (-) | ATT <sub>OUT</sub> (-) | 19 |
| 11 | V <sub>CMOS</sub>     | GND <sub>CMOS</sub>    | 18 |
| 12 | CLK                   | N/C                    | 17 |
| 13 | DAT                   | C1                     | 16 |
| 14 | EN                    | C0                     | 15 |

Figure 3: Pin Out

Table 1: Pin Description

| PIN | NAME                  | DESCRIPTION                           | PIN | NAME                   | DESCRIPTION                           |
|-----|-----------------------|---------------------------------------|-----|------------------------|---------------------------------------|
| 1   | GND                   | Ground                                | 15  | N/C                    | No Connection <sup>(1)</sup>          |
| 2   | V <sub>ATTN</sub>     | Supply Attenuator                     | 16  | N/C                    | No Connection <sup>(1)</sup>          |
| 3   | ATT <sub>IN</sub> (+) | Attenuator (+) Input <sup>(2)</sup>   | 17  | N/C                    | No Connection <sup>(1)</sup>          |
| 4   | A1 <sub>OUT</sub> (+) | Amplifier A1 (+) Output               | 18  | GND <sub>CMOS</sub>    | Ground for Digital CMOS Circuit       |
| 5   | A1 <sub>IN</sub> (+)  | Amplifier A1 (+) Input <sup>(2)</sup> | 19  | ATT <sub>OUT</sub> (-) | Attenuator (-) Output <sup>(2)</sup>  |
| 6   | V <sub>g1</sub>       | Amplifier A1 (+/-) Control            | 20  | A2 <sub>IN</sub> (-)   | Amplifier A2 (-) Input <sup>(2)</sup> |
| 7   | I <sub>SET1</sub>     | Amplifier A1 (+/-) Current Adjust     | 21  | A2 <sub>OUT</sub> (-)  | Amplifier A2 (-) Output               |
| 8   | A1 <sub>IN</sub> (-)  | Amplifier A1 (-) Input <sup>(2)</sup> | 22  | I <sub>SET2</sub>      | Amplifier A2 (+/-) Current Adjust     |
| 9   | A1 <sub>OUT</sub> (-) | Amplifier A1 (-) Output               | 23  | V <sub>g2</sub>        | Amplifier A2 (+/-) Control            |
| 10  | ATT <sub>IN</sub> (-) | Attenuator (-) Input <sup>(2)</sup>   | 24  | A2 <sub>OUT</sub> (+)  | Amplifier A2 (+) Output               |
| 11  | V <sub>CMOS</sub>     | Supply For Digital CMOS Circuit       | 25  | A2 <sub>IN</sub> (+)   | Amplifier A2 (+) Input <sup>(2)</sup> |
| 12  | CLK                   | Clock                                 | 26  | ATT <sub>OUT</sub> (+) | Attenuator (+) Output <sup>(2)</sup>  |
| 13  | DAT                   | Data                                  | 27  | N/C                    | No Connection <sup>(1)</sup>          |
| 14  | EN                    | Enable                                | 28  | GND                    | Ground                                |

**Notes:**

(1) All N/C pins should be grounded.

(2) Pins should be AC-coupled. No external DC bias should be applied.

## ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

| PARAMETER                                            | MIN  | MAX            | UNIT |
|------------------------------------------------------|------|----------------|------|
| Analog Supply (pins 2, 4, 9, 21, 24)                 | 0    | 9              | VDC  |
| Digital Supply: $V_{CMOS}$ (pin 11)                  | 0    | 6              | VDC  |
| Amplifier Controls: $V_{g1}$ , $V_{g2}$ (pins 6, 23) | -5   | 2              | V    |
| RF Power at Inputs ( pins 5, 8)                      | -    | +60            | dBmV |
| Digital Interface (pins 12, 13, 14)                  | -0.5 | $V_{CMOS}+0.5$ | V    |
| Storage Temperature                                  | -55  | +200           | °C   |
| Soldering Temperature                                | -    | 260            | °C   |
| Soldering Time                                       | -    | 5              | Sec  |

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Notes:

(1) Pins 3, 5, 8, 10, 19, 20, 25, 26 should be AC-coupled. No external DC bias should be applied.

(2) Pins 7 and 22 should be grounded or pulled to ground through a resistor. No external DC bias

Table 3: Operating Ranges

| PARAMETER                                           | MIN          | TYP | MAX        | UNIT |
|-----------------------------------------------------|--------------|-----|------------|------|
| Amplifier Supply: $V_{DD}$ (pins 4, 9, 21, 24)      | 4.5          | 5   | 7          | VDC  |
| Attenuator Supply: $V_{ATTN}$ (pin 2)               | $V_{DD}-0.5$ | 5   | 7          | VDC  |
| Digital Supply: $V_{CMOS}$ (pin 11)                 | 3.0          | -   | 5.5        | VDC  |
| Digital Interface                                   | 0            | -   | $V_{CMOS}$ | V    |
| Amplifier Controls $V_{g1}$ , $V_{g1}$ (pins 6, 23) | -5           | 1   | 2          | V    |
| Case Temperature                                    | -40          | 25  | 85         | °C   |

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

**Table 4: DC Electrical Specifications****T<sub>A</sub> = 25 °C; V<sub>DD</sub>, V<sub>ATTN</sub>, V<sub>CMOS</sub> = +5.0 VDC; Vg1, Vg2 = +1.0 V (Tx enabled); Vg1, Vg2 = 0 V (Tx disabled)**

| PARAMETER                          | MIN    | TYP        | MAX         | UNIT    | COMMENTS                  |
|------------------------------------|--------|------------|-------------|---------|---------------------------|
| Amplifier A1 Current (pins 4, 9)   | -<br>- | 48<br>2.4  | 80<br>6     | mA      | Tx enabled<br>Tx disabled |
| Amplifier A2 Current (pins 21, 24) | -<br>- | 77<br>3.7  | 120<br>9    | mA      | Tx enabled<br>Tx disabled |
| Attenuator Current (pin 2)         | -      | 9          | 15          | mA      |                           |
| Total Power Consumption            | -<br>- | 0.67<br>75 | 1.08<br>150 | w<br>mW | Tx enabled<br>Tx disabled |
| Thermal Resistance (θJC)           | -      | 38         | -           | °C/W    |                           |

**Table 5a: AC Electrical Specifications****T<sub>A</sub> = 25 °C; V<sub>DD</sub>, V<sub>ATTN</sub>, V<sub>CMOS</sub> = +5.0 VDC; Vg1, Vg2 = +1.0 V (Tx enabled); Vg1, Vg2 = 0 V (Tx disabled)**

| PARAMETER                                          | MIN    | TYP         | MAX    | UNIT  | COMMENTS                   |
|----------------------------------------------------|--------|-------------|--------|-------|----------------------------|
| Gain (10 MHz)                                      | 27.5   | 29.3        | 30.5   | dB    | 0 dB attenuation setting   |
| Gain Flatness                                      | -<br>- | 0.75<br>1.5 | -<br>- | dB    | 5 to 42 MHz<br>5 to 65 MHz |
| Gain Variation over Temperature                    | -      | -0.006      | -      | dB/°C |                            |
| Attenuation Steps:                                 |        |             |        |       |                            |
| 1 dB                                               | 0.65   | 0.83        | 1.00   | dB    | Monotonic                  |
| 2 dB                                               | 1.6    | 1.70        | 2.05   |       |                            |
| 4 dB                                               | 3.6    | 3.75        | 4.0    |       |                            |
| 8 dB                                               | 7.5    | 7.75        | 8.0    |       |                            |
| 16 dB                                              | 15.0   | 15.40       | 15.8   |       |                            |
| 32 dB                                              | 30.2   | 30.75       | 31.3   |       |                            |
| Maximum Attenuation                                | 58.6   | 60.3        | -      | dB    |                            |
| 2 <sup>nd</sup> Harmonic Distortion Level (10 MHz) | -      | -75         | -53    | dBc   | +60 dBmV into 75 Ohms      |
| 3 <sup>rd</sup> Harmonic Distortion Level (10 MHz) | -      | -60         | -53    | dBc   | +60 dBmV into 75 Ohms      |
| 3rd Order Output Intercept                         | 78     | -           | -      | dBmV  |                            |
| 1 dB Gain Compression Point                        | -      | 68.5        | -      | dBmV  |                            |
| Noise Figure                                       | -      | 3.0         | 4.0    | dB    | Includes input balun loss  |

Note:

As measured in ANADIGICS test fixture.

**Table 5b: AC Electrical Specifications (Continued)**

$T_A = 25\text{ }^{\circ}\text{C}$ ;  $V_{DD}$ ,  $V_{ATTN}$ ,  $V_{CMOS} = +5.0\text{ VDC}$ ;  $V_{g1}$ ,  $V_{g2} = +1.0\text{ V}$  (Tx enabled);  $V_{g1}$ ,  $V_{g2} = 0\text{ V}$  (Tx disabled)

| PARAMETER                                                                                            | MIN    | TYP        | MAX            | UNIT  | COMMENTS                                                     |
|------------------------------------------------------------------------------------------------------|--------|------------|----------------|-------|--------------------------------------------------------------|
| Output Noise Power<br>Active / No Signal / Min. Atten. Set.<br>Active / No Signal / Max. Atten. Set. | -<br>- | -<br>-     | -38.5<br>-53.8 | dBmV  | Any 160 kHz bandwidth from 5 to 42 MHz                       |
| Isolation (45 MHz) in Tx disable mode                                                                | -      | 65         | -              | dB    | Difference in output signal between Tx enable and Tx disable |
| Differential Input Impedance                                                                         | -      | 300        | -              | Ohms  | between pins 5 and 8 (Tx enabled)                            |
| Input Impedance                                                                                      | -      | 75         | -              | Ohms  | with transformer (Tx enabled)                                |
| Input Return Loss<br>(75 Ohm characteristic impedance)                                               | -<br>- | -20<br>-5  | -12<br>-       | dB    | Tx enabled<br>Tx disabled                                    |
| Differential Output Impedance                                                                        | -      | 300        | -              | Ohms  | between pins 21 and 24                                       |
| Output Impedance                                                                                     | -      | 75         | -              | Ohms  | with transformer                                             |
| Output Return Loss<br>(75 Ohm characteristic impedance)                                              | -<br>- | -17<br>-15 | -12<br>-10     | dB    | Tx enabled<br>Tx disabled                                    |
| Output Voltage Transient<br>Tx enable / Tx disable                                                   | -<br>- | -<br>4     | 100<br>7       | mVp-P | 0 dB attenuator setting<br>24 dB attenuator setting          |

Note: As measured in ANADIGICS test fixture.



Figure 5: Attenuation Level vs Control Word

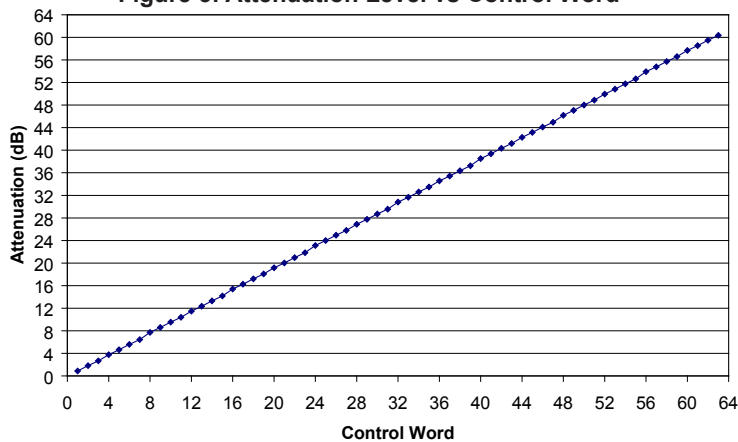
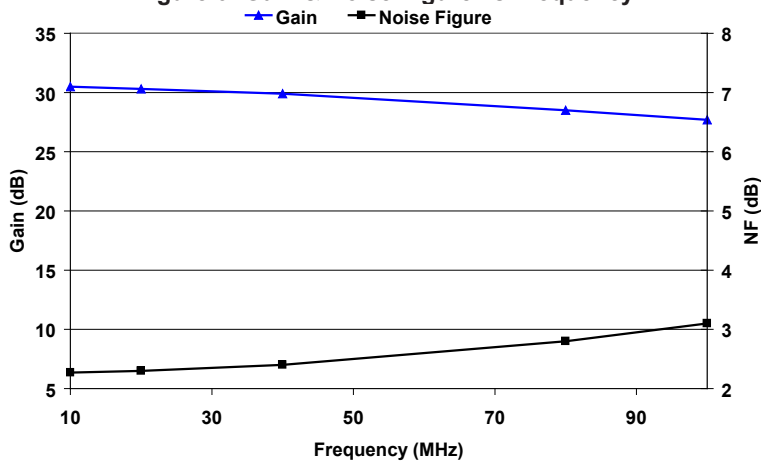
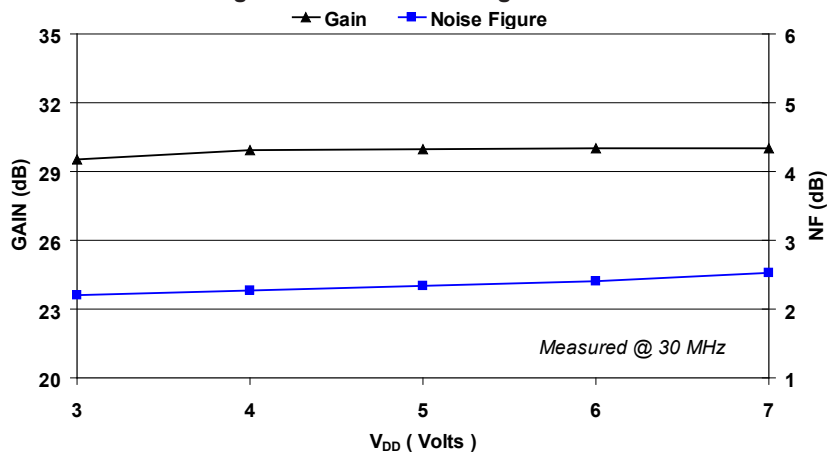


Figure 6: Gain &amp; Noise Figure vs Frequency

Figure 7: Gain & Noise Figure vs  $V_{DD}$ 

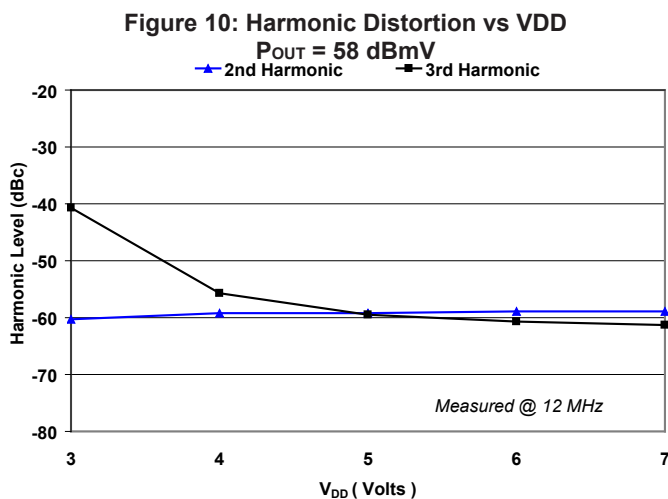
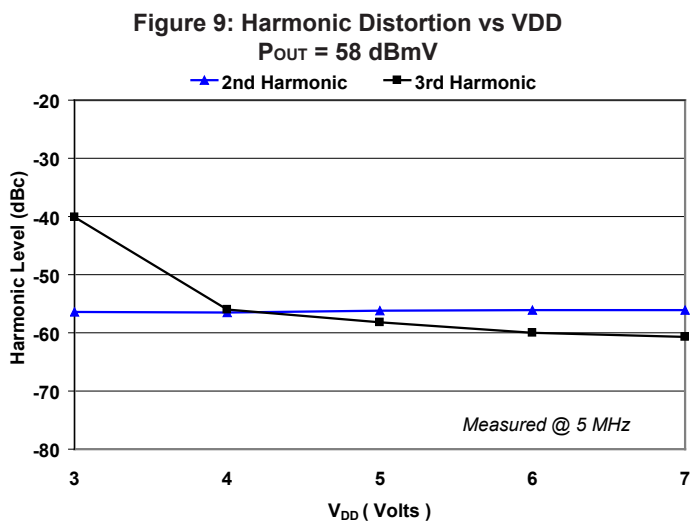
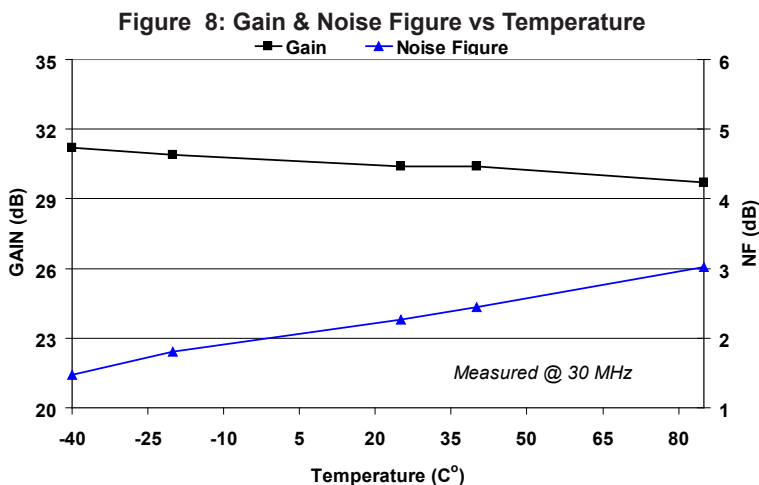


Figure 11: Harmonic Distortion vs Temperature

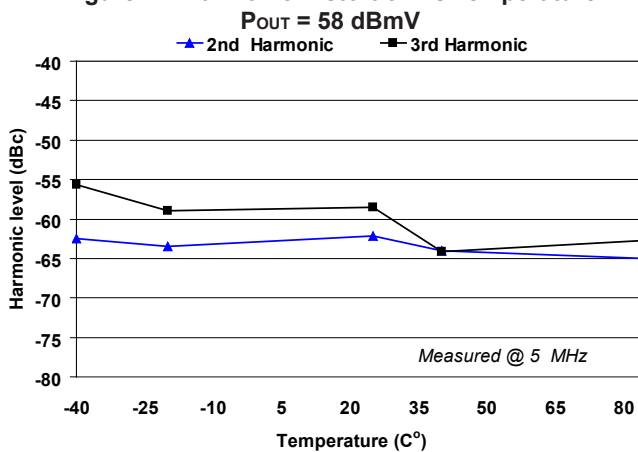


Figure 12: Harmonic Distortion vs Power Out

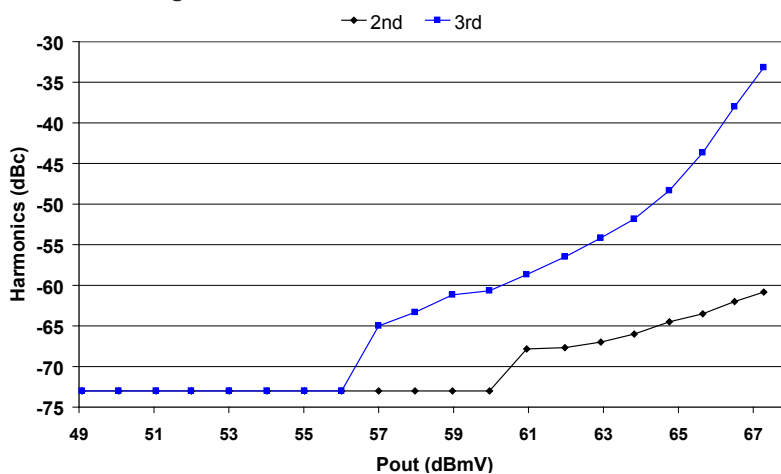
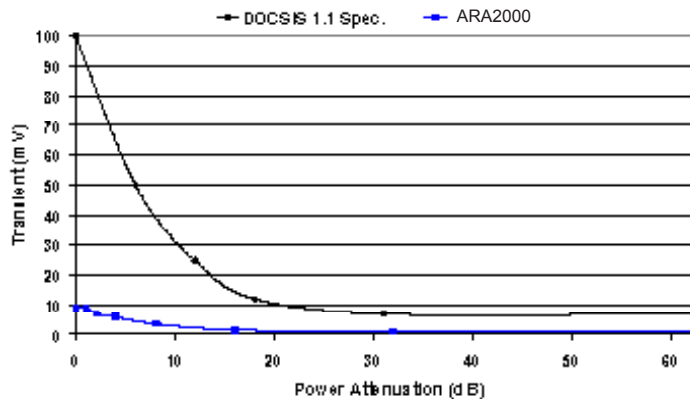
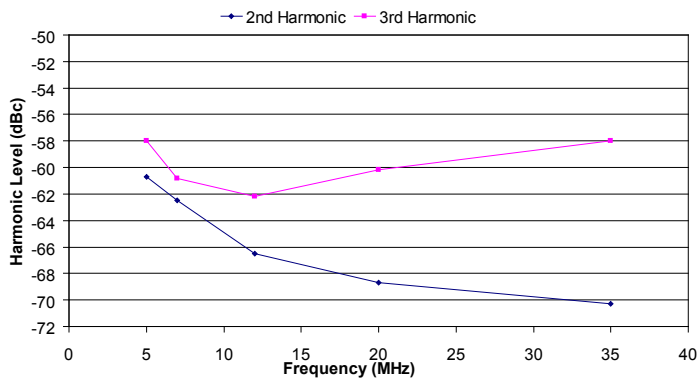


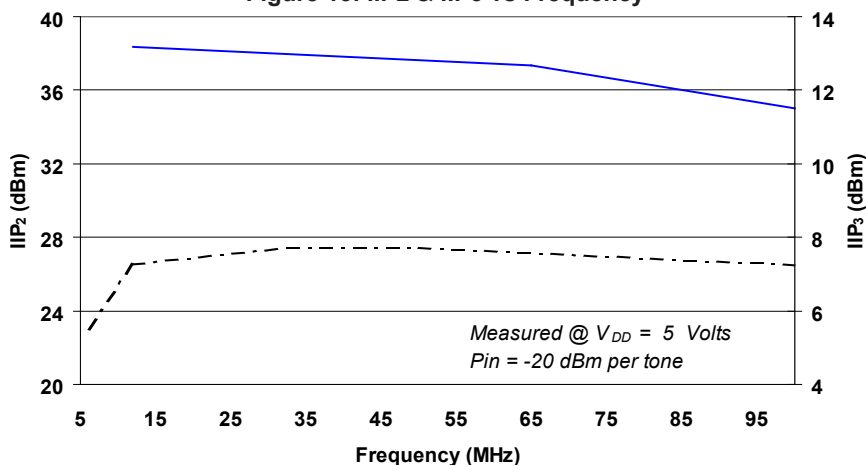
Figure 13: Transients vs Attenuation

 $P_{OUT} = 55 \text{ dBmV}$  at 0 dB attenuation

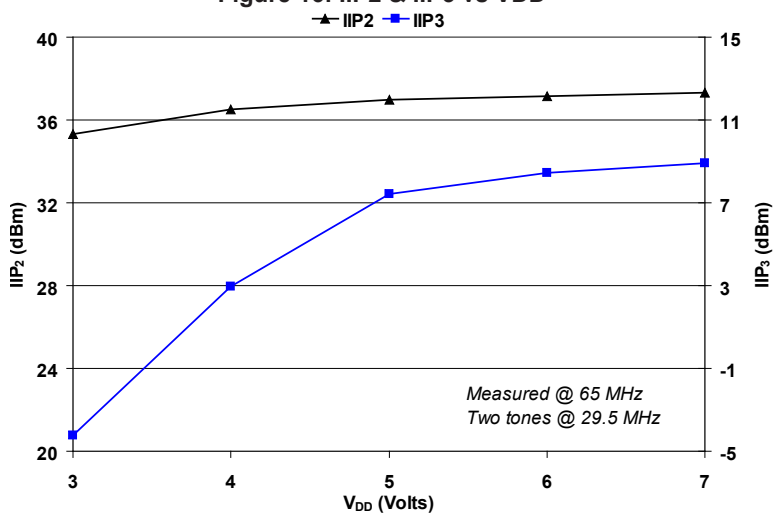
**Figure 14: Harmonic Performance over Frequency**  
**P<sub>OUT</sub> = +62 dBmV**



**Figure 15: IIP2 & IIP3 vs Frequency**



**Figure 16: IIP2 & IIP3 vs VDD**



## LOGIC PROGRAMMING

### Programming Instructions

The programming word is set through an 8 bit shift register via the data, clock and enable lines. The data is entered in order with the most significant bit (MSB) first and the least significant bit (LSB) last. The enable line must be low for the duration of the data entry, then

set high to latch the shift register. The rising edge of the clock pulse shifts each data value into the register. Software is Available from ANADIGICS Application Engineering to set the data bits through the serial cable on the ARA2004 evaluation board.

**Table 6: Programming Register**

| DATA BIT | D <sub>7</sub> | D <sub>6</sub> | D <sub>5</sub> | D <sub>4</sub> | D <sub>3</sub> | D <sub>2</sub> | D <sub>1</sub> | D <sub>0</sub> |
|----------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| FUNCTION | P7             | P6             | P5             | P4             | P3             | P2             | P1             | P0             |

**Table 7: Data Description**

| VALUE | FUNCTION<br>(1 = on, 0 = bypass) |
|-------|----------------------------------|
| P7    | N/A                              |
| P6    | N/A                              |
| P5    | 32 dB Attenuator Bit             |
| P4    | 16 dB Attenuator Bit             |
| P3    | 8 dB Attenuator Bit              |
| P2    | 4 dB Attenuator Bit              |
| P1    | 2 dB Attenuator Bit              |
| P0    | 1 dB Attenuator Bit              |

Table 8: Digital Interface Specification

| PARAMETER                                 | MIN | TYP | MAX  | UNIT |
|-------------------------------------------|-----|-----|------|------|
| Logic High Input: $V_H$                   | 2.0 | -   | -    | V    |
| Logic Low Input: $V_L$                    | -   | -   | 0.8  | V    |
| Logic Input Current Consumption           | -   | -   | 0.01 | mA   |
| Data to Clock Set Up Time: $t_{cs}$       | 50  | -   | -    | ns   |
| Data to Clock Hold Time: $t_{ch}$         | 10  | -   | -    | ns   |
| Clock Pulse Width High: $t_{cwh}$         | 50  | -   | -    | ns   |
| Clock Pulse Width Low: $t_{cwl}$          | 50  | -   | -    | ns   |
| Clock to Load Enable Setup Time: $t_{es}$ | 50  | -   | -    | ns   |
| Load Enable Pulse Width: $t_{ew}$         | 50  | -   | -    | ns   |
| Rise Time: $t_r$                          | -   | 10  | -    | ns   |
| Fall Time: $t_f$                          | -   | 10  | -    | ns   |

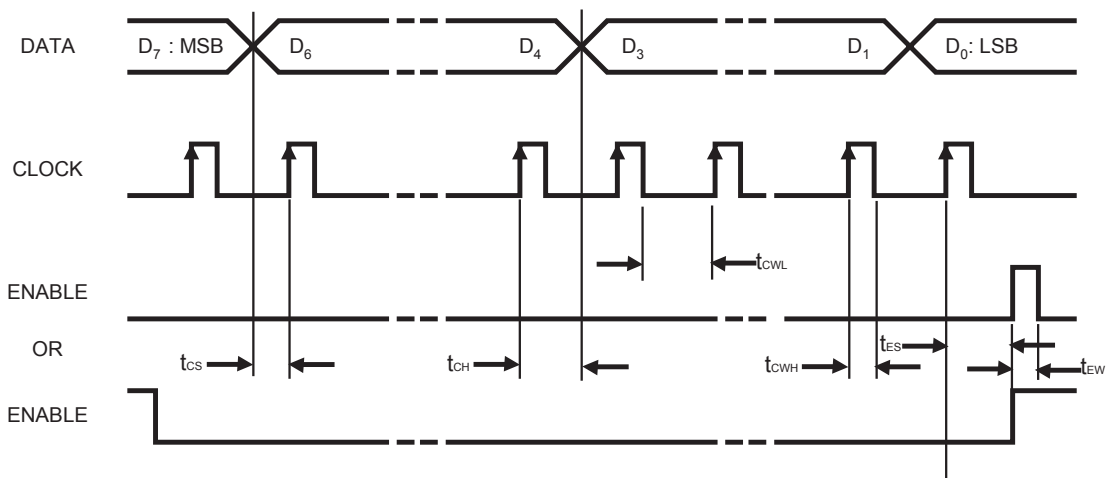


Figure 17: Serial Data Input Timing

## APPLICATION INFORMATION

### Transmit Enable / Disable

The ARA2004 includes two amplification stages that each can be shut down through external control pins Vg1 and Vg2 (pins 6 and 23, respectively.) By applying a slightly positive bias of typically +1.0 Volts, the amplifier is enabled. In order to disable the amplifier, the control pin needs to be pulled to ground.

A practical way to implement the necessary control is to use bias resistor networks similar to those shown in the test circuit schematic (Figure 4.) Each network includes a resistor shunted to ground that serves as a pull-down to disable the amplifier when no control voltage is applied. When a positive voltage is applied, the network acts as a voltage divider that presents the required +1.0 Volts to enable the amplifier. By selecting different resistor values for the voltage divider, the network can accommodate different control voltage inputs.

The Vg1 and Vg2 pins may be connected together directly, and controlled through a single resistor network from a common control voltage.

### Amplifier Bias Current

The ISET pins (7 and 22) set the bias current for the amplification stages. Grounding these pins results in the maximum possible current. By placing a resistor from the pin to ground, the current can be reduced. The recommended bias conditions use the configuration shown in the test circuit schematic in Figure 4.

### Thermal Layout Considerations

The device package for the ARA2004 features a heat slug on the bottom of the package body. Use of the heat slug is an integral part of the device design. Soldering this slug to the ground plane of the PC board will ensure the lowest possible thermal resistance for the device, and will result in the longest MTF (mean time to failure.)

A PC board layout that optimizes the benefits of the heat slug is shown in Figure 18. The via holes located under the body of the device must be plated through to a ground plane layer of metal, in order to provide a sufficient heat sink. The recommended solder mask outline is shown in Figure 19.

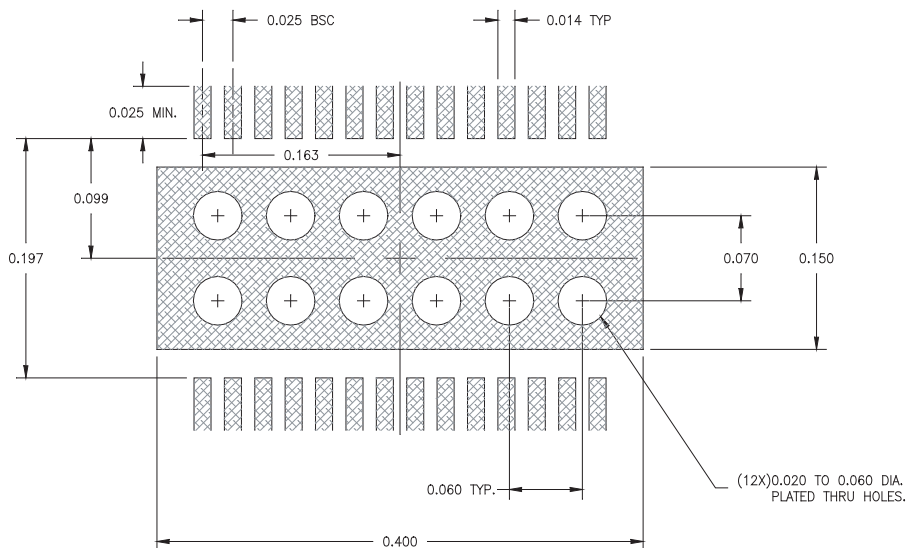


Figure 18: PC Board Layout

## Output Transformer

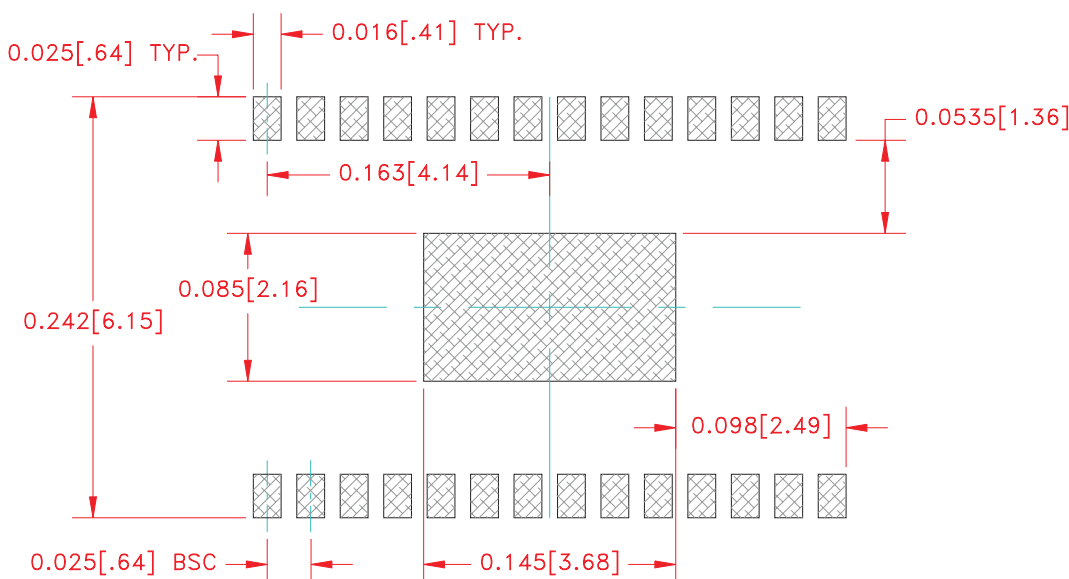
Matching the output of the ARA2004 to a 75 Ohm load is accomplished using a 2:1 turns ratio transformer. In addition to providing an impedance transformation, this transformer provides the bias to the output amplifier stage via the center tap.

The transformer also cancels even mode distortion products and common mode signals, such as the voltage transients that occur while enabling and disabling the amplifiers. As a result, care must be taken when selecting the transformer to be used at the output. It must be capable of handling the RF and DC power requirements without saturating the core,

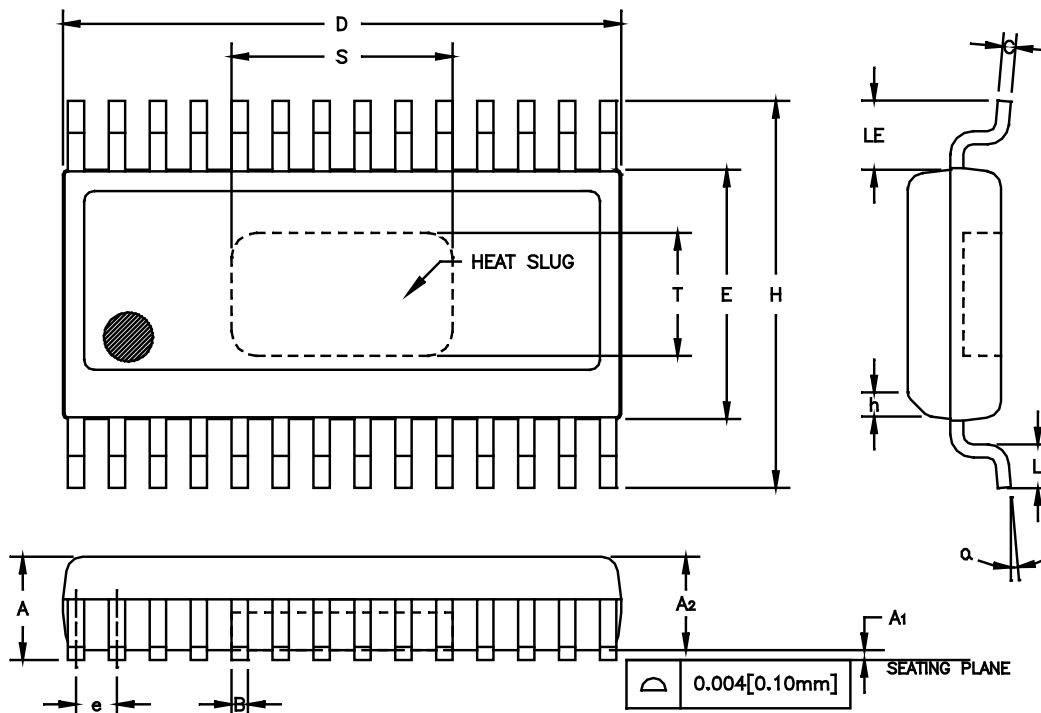
and it must have adequate isolation and good phase and amplitude balance. It also must operate over the desired frequency and temperature range for the intended application.

## ESD Sensitivity

Electrostatic discharges can cause permanent damage to this device. Electrostatic charges accumulate on test equipment and the human body, and can discharge without detection. Although the ARA2004 has some built-in ESD protection, proper precautions and handling are strongly recommended. Refer to the ANADIGICS application note on ESD precautions.



**Figure 19: Solder Mask Outline**



| Symbol         | INCHES    |       | MILLIMETERS |      | NOTE |
|----------------|-----------|-------|-------------|------|------|
|                | MIN.      | MAX.  | MIN.        | MAX. |      |
| A              | 0.058     | 0.068 | 1.47        | 1.73 |      |
| A <sub>1</sub> | 0.000     | 0.004 | 0.00        | 0.10 |      |
| A <sub>2</sub> | 0.054     | 0.060 | 1.37        | 1.52 |      |
| B              | 0.008     | 0.014 | 0.20        | 0.35 | 5    |
| C              | 0.007     | 0.012 | 0.18        | 0.30 | 5    |
| D              | 0.385     | 0.393 | 9.78        | 9.98 | 2    |
| E              | 0.151     | 0.157 | 3.84        | 3.99 | 3    |
| e              | 0.025 BSC |       | 0.64 BSC    |      | 4    |
| H              | 0.228     | 0.244 | 5.79        | 6.20 |      |
| h              | 0.015x45° |       | 0.38x45°    |      |      |
| L              | 0.016     | 0.032 | 0.41        | 0.81 |      |
| LE             | 0.042     | —     | 1.07        | —    |      |
| q              | 0°        | 8°    | 0°          | 8°   |      |
| S              | 0.105     | 0.135 | 2.67        | 3.43 | 6    |
| T              | 0.045     | 0.075 | 1.41        | 1.91 | 6    |

**NOTES:**

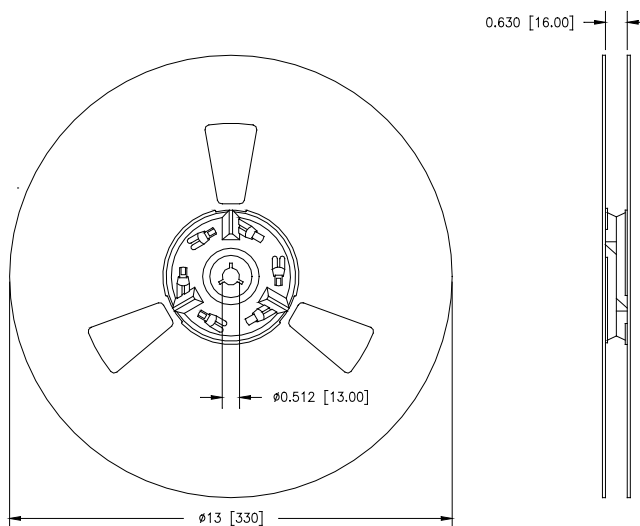
1. CONTROLLING DIMENSION: INCHES
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.
4. MAXIMUM LEAD TWIST/SKEW TO BE  $\pm 0.0035$  [0.089mm].
5. LEAD WIDTH "B" AND THICKNESS "C" MAX. DIMENSION IS AFTER PLATING.
6. DIMENSIONS "S" AND "T" INDICATE EXPOSED SLUG AREA.

0-012

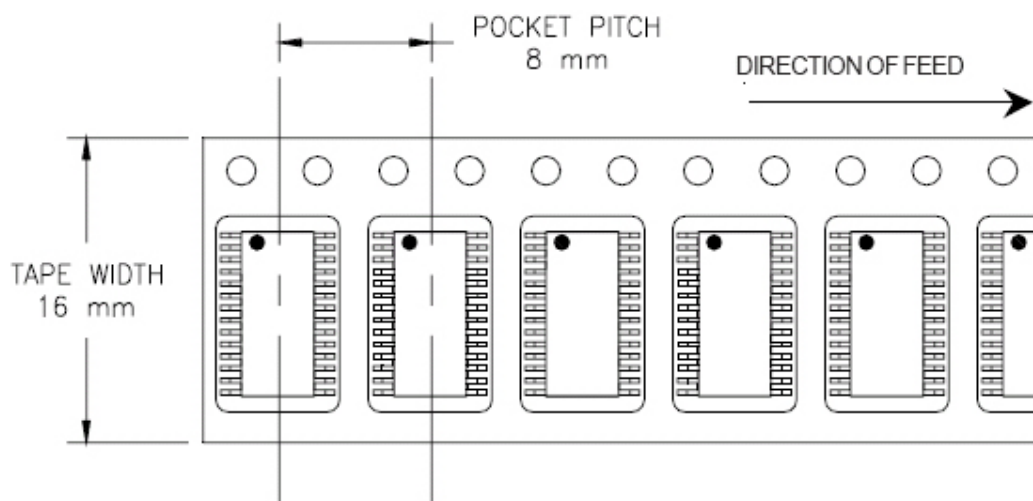
**Figure 20: S12 Package Outline - 28 SSOP with Heat Slug**

## COMPONENT PACKAGING

Volume quantities for the ARA2000 are supplied on tape and reel. Each reel holds 3,500 pieces.



**Figure 21: Reel Dimensions**



**Figure 22: Tape Dimensions**



NOTES





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URL: <http://www.anadigics.com>

**IMPORTANT NOTICE**

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