Product Document

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Datasheet

DS001036

AS7056

Biosignal Converting Unit

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Content Guide

1 General Description

The AS7056 Biosignal Sensor Analog Frontend (AFE) is the next generation Vital Sign Sensor. It enables the user to detect biosignals such as photoplethysmogram (PPG) and pulse transit time (PTT), as well as proximity. PPG is the most used HRM method. It measures the pulse rate - by sampling light modulated by the blood vessels, which expand and contract as blood pulses through them. Apart from HRM/HRV, optical blood pressure and SpO_2 are also enabled by the two independent working photodiode inputs of the AS7056. The AS7056 is a size and performances optimized Analog Frontend to support space-limited applications such as in-ear vital sign monitoring.

The AS7056 provides two LEDs and one VCSEL driver outputs, samples up to three photodiode inputs, and supports proximity detection integrated into one of the PPG signal channels. This enables high flexibility for several LED and photodiode arrangements in different applications. Furthermore, the AS7056 Biosignal Sensor Analog Frontend provides two ADC channels for simultaneous PPG measurements and an automatic photodiode offset control.

The AS7056's low-power design and small form factor are particularly well-suited for application in earbuds, fitness bands, smartwatches, sports watches, and smart patches. In these cases, board space is limited, and users look for extended, multi-day intervals between battery recharges. A thin package dimension makes the AS7056 suitable for height-constrained solutions like earbuds.

1.1 Key Benefits & Features

The benefits and features of the AS7056 Biosignal Converting Unit are listed below:

Figure 1:
Added Value of Using AS7056

Benefits	Features
Flexible LED/photodiode configuration.	2 LED + 1 VCSEL driver and 3 photodiode input pins.
Allows smallest application size, e.g. in-ear vital sign monitoring	Small Wafer-Level-Chip-Scale-Package (WLCSP).
Enables optical blood pressure measurements.	Two synchronized PPG acquisition channels.
Enables proximity detection for additional energy savings	Two independent, programmable sequence blocks inside the PPG signal acquisition.
Good HRM measurement quality.	Low noise analog optical front-end.
Long operating time.	Hardware sequencer to offload processor. Adjustable LED driver with current control.

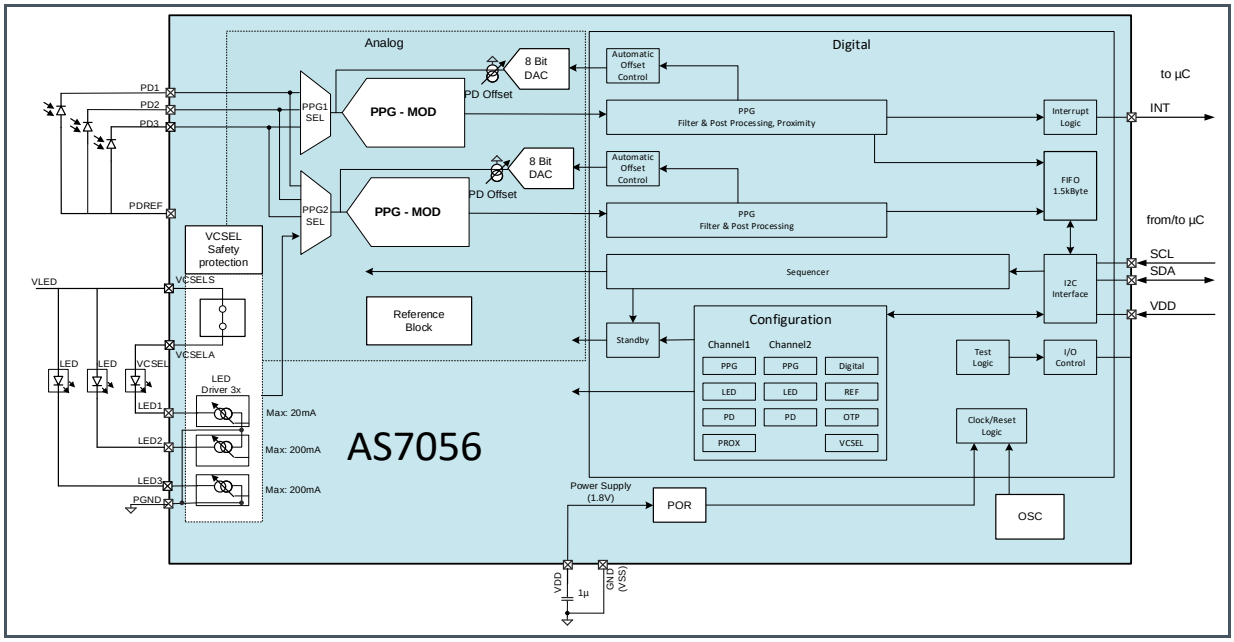
1.2 Applications

- Earbuds
- Hearables
- Optical sensor platform
- Fitness band
- Smart watch
- Smart patches
- Heart rate monitor
- Cuff-less optical blood pressure measurements

1.3 Block Diagram

The diagram below shows the functional blocks of this device:

Figure 2:
Functional Blocks of AS7056



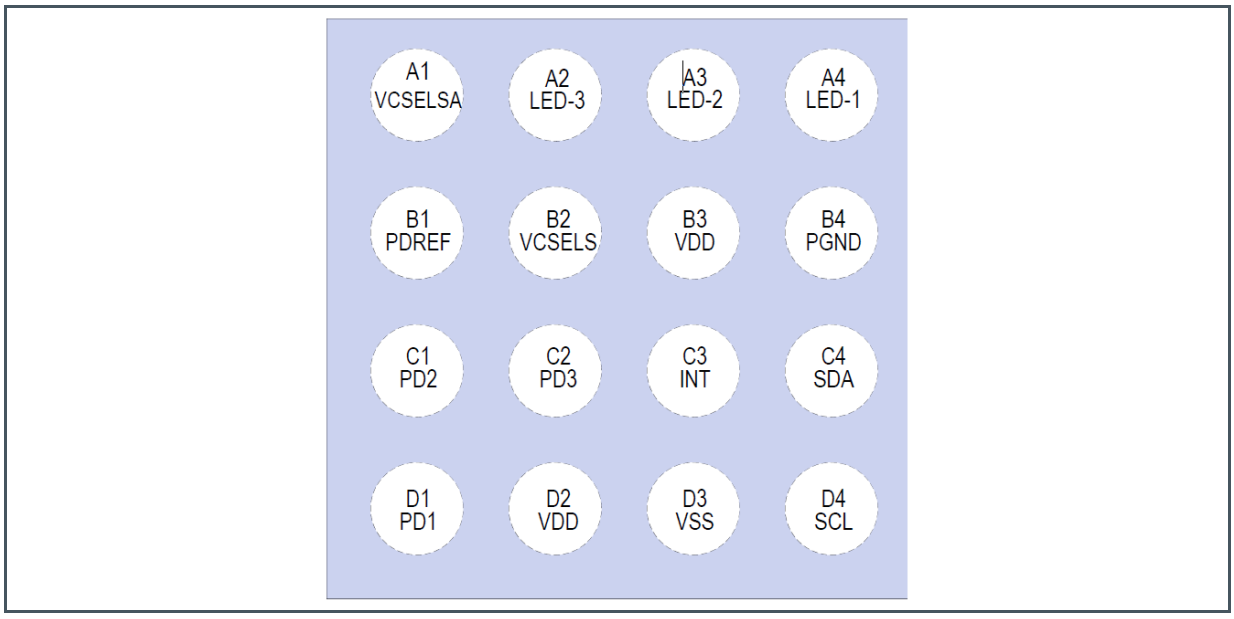
2 Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS7056-BWLM	WLCSP	AS7056, AS7056/57	Tape & Reel	500 pcs/reel
AS7056-BWLT	WLCSP	AS7056, AS7056/57	Tape & Reel	10000 pcs/reel

3 Pin Assignment

3.1 Pin Diagram

Figure 3:
Top View of AS7056 Pin Diagram



3.2 Pin Description

Figure 4:
Pin Description of AS7056

Pin Number	Pin Name	Pin Type[1]	Description
A1	VCSELA	AO	VCSEL output (anode)
A2	LED3	AO	Output LED driver 3
A3	LED2	AO	Output LED driver 2
A4	LED1	AO	Output LED driver 1
B1	PDREF	AO	Reference potential for photodiodes
B2	VCSELS	AI	VCSEL input (supply)
B3	VDD	P	Digital Supply
B4	PGND	G	Ground for LED drivers 1-3

Pin Number	Pin Name	Pin Type(1)	Description
C1	PD2	AI	Photodiode input
C2	PD3	AI	Photodiode input
C3	INT	DO	Interrupt
C4	SDA	DO	I^2C Data
D1	PD1	AI	Photodiode input
D2	VDD	P	Digital supply
D3	VSS	G	Ground
D4	SCL	DI	Clock for I^2C

(1) **Abbreviations:**

DI	Digital Input
DO	Digital Output
AI	Analog Input
AO	Analog Output
P	Power Supply
G	Ground

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5
Absolute Maximum Ratings of AS7056

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_{DD}	Supply Voltage		1.98	V	
V_{IN}	Input Pin Voltage to Ground pins	-0.3	V_{DD}+0.3 max. 1.98	V	Internal diode to V_{DD}
$V_{LED1/2/3/VCSELA}$	Voltage at Pins VLED1,VLED2,VLED3, VVCSELA	-0.3	5.5	V	
$V_{VCSELS/A}$	VCSEL voltage supply	-0.3	5.5	V	
$V_{VCSELA-VCSELS}$	Voltage at Pin VCSELA		0.3	V	Internal diode to V_{VCSELS}
$V_{GND-PGND}$	Analog to Power Ground Voltage Difference		±0.3	V	
I_{SCR}	Input Current (latch-up immunity)		±100	mA	JEDEC JESD78 Connect the specified capacitor on PDREF during latch-up test.
I_{LEDON}	Average LED ON Current		35	mA	DC current with all LEDs ON during all 8 time slots
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM		±2.0	kV	JS-001-2017
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage Temperature Range	-40	125	°C	JESD22-A103
T_{AMB}	Operating Free-air Temperature	-30	85	°C	
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020 (1)
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level		1		Maximum floor life time unlimited @ 30°C/85% RH_{max}

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices.”

5 Electrical Characteristics

All limits are guaranteed at an ambient temperature of 25 °C. The parameters with minimum (Min) and maximum (Max) values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Electrical Characteristics of AS7056

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		1.7	1.8	1.98	V
I_{VDD}	Supply current in power down mode			1.1		µA
	Supply current in idle mode	lf_osc_on=1		2.92		µA
	Supply current PPG ADC active	One subsample, one modulator @25 SpS; enabled Stand-by Mode pll_on=1 hf_osc_on=1 lf_osc_on=1 en_bg=1 en_vcm_ppg=1 en_vr_led=1 en_bias=1 byp_ref_lp=0 mod1_en=1 mod2_en=0 stby_en_on=0x7f		10	60	µA
$f_{Sampling}$	Sampling frequency		0.5	25	1000	Hz
Photodiode						
I_{OS}	DAC offset current full scale range	ppg_ios_fs=0		1		µA
		ppg_ios_fs=1		2		
		ppg_ios_fs=2		4		
		ppg_ios_fs=3		8		
		ppg_ios_fs=4		16		
		ppg_ios_fs=5		32		
		ppg_ios_fs=6		64		
		ppg_ios_fs=7		128		

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{PD}	Total photodiode capacitance connected to PPG_ADC	0 V reserve voltage		60	300	pF
I_{PD}	Photo current input	(∑ signal range 1 µA-64 µA)	0		64	µA
LED Driver						
V_{LED}	LED pad voltage				5	V
LED Driver 2-3						
I_{LED}	Allowed operating LED output current	ledx_ictrl=127		200.00		mA
V_{Compl}	Compliance voltage	ledx_ictrl=0…127			0.3	V
VCSEL Driver						
I_{VCSEL}	Allowed operating LED output current	ledx_ictrl=63		20.00		mA
V_{Compl}	Compliance voltage	ledx_ictrl=0…63			0.3	V
SDA, SCL						
V_{IH}	Input high	Switching threshold while rising edge of the input signal is introduced	0.54		1.26	V
V_{IL}	Input low	Switching threshold while falling edge of the input signal is introduced	0.54		1.26	V
SDA						
V_{OH}	Output high	Pin's source load current is 6 mA condition: E2=E4="1" (full available driver strength)			V_{DD}-0.4	V
V_{OL}	Output low	Pin's sink load current is 6 mA condition: E2=E4="1" (full available driver strength)			0.4	V
INT						
V_{OH}	Output high	Pin's source load current is 2 mA condition: E2=E4="1" (full available driver strength)			V_{DD}-0.4	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output low	Pin’s sink load current is 2 mA condition: E2=E4=”1” (full available driver strength)			0.4	V

6 Register Description

The device is controlled and monitored by registers accessed through the I²C interface. These registers provide device control functions and can be read - to determine the device status and acquire device data.

The register set is summarized below in Figure 7. The values of all registers and fields that are listed as reserved, or are not listed, must not be changed. Two-byte fields are always latched with the low byte, followed by the high byte. The “Name” column illustrates the purpose of each register - by highlighting the function associated with each bit. The bits are shown from MSB (D7) to LSB (D0). The grey fields are reserved, and their values must not be changed.

6.1 Register Overview

Figure 7:
Register Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0X10	**CONTROL**								i2c_fm_plus
0X11	**CGB_CFG**	bgcal_done_sel	bgcal_en				pll_on	hf_osc_on	lf_osc_on
0X12	**INT_CFG**		int_e2	int_e4	int_sr	int_pu	int_pd		int_inv
0X13	**CSXN_CFG**		csxn_e2	csxn_e4	csxn_sr	csxn_pu	csxn_pd		
0X14	**IO_CFG**		sda_e2	sda_e4	sda_sr				
0X15	**REF_CFGA**	en_bg	sel_ln_iled	en_vcm_ppg	sel_strtup	en_vr_led	en_bias	en_ptat	byp_ref_lp
0X16	**REF_CFGB**	iled_tc					sel_iref_ln	byp_progtc	sel_ref
0X19	**MOD_CFGA**							mod_opamp_ibias	
0X1A	**MOD_CFGB**		mod_dsm_mode		mod_comp_mode		mod_ref_mode		
0X1B	**MOD1_CFGA**			mod1_ios_mux	mod1_en	mod1_ios_dir	mod1_ios_fs		
0X1C	**MOD1_CFGB**					mod1_iref_scale			
0X1D	**MOD1_CFGC**			mod1_seq1_dsm_ampl	mod1_seq1_cint				
0X1E	**MOD1_CFGD**	mod1_seq1_iref							
0X1F	**MOD1_CFGE**			mod1_seq2_dsm_ampl		mod1_seq2_cint			

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0X20	**MOD1_CFGF**	mod1_seq2_iref							
0X21	**MOD2_CFGA**			mod2_ios_mux	mod2_en	mod2_ios_dir	mod2_ios_fs		
0X22	**MOD2_CFGB**					mod2_iref_scale			
0X23	**MOD2_CFGC**			mod2_seq1_dsm_ampl	mod2_seq1_cint				
0X24	**MOD2_CFGD**	mod2_seq1_iref							
0X25	**MOD2_CFGE**			mod2_seq2_dsm_ampl	mod2_seq2_cint				
0X26	**MOD2_CFGF**	mod2_seq2_iref							
0X28	**VCSEL_CFG**	vcsel_we_disable	vcsel_safety_disable	vcsel_vrsel		vcsel_short_vdd_wait		vcsel_short_vss_wait	
0X29	**SEQ1_LED1_CURR**		seq1_led1_curr						
0X2A	**SEQ2_LED1_CURR**		seq2_led1_curr						
0X2B	**SEQ1_LED2_CURR**		seq1_led2_curr						
0X2C	**SEQ2_LED2_CURR**		seq2_led2_curr						
0X2D	**SEQ1_LED3_CURR**		seq1_led3_curr						
0X2E	**SEQ2_LED3_CURR**		seq2_led3_curr						
0X2F	**LED_SEQ1_SUB12**		led_seq1_sub1				led_seq1_sub2		
0X30	**LED_SEQ1_SUB34**		led_seq1_sub3				led_seq1_sub4		
0X31	**LED_SEQ1_SUB56**		led_seq1_sub5				led_seq1_sub6		
0X32	**LED_SEQ1_SUB78**		led_seq1_sub7				led_seq1_sub8		
0X33	**LED_SEQ2_SUB12**		led_seq2_sub1				led_seq2_sub2		
0X34	**LED_SEQ2_SUB34**		led_seq2_sub3				led_seq2_sub4		
0X35	**LED_LOWVDS_WAIT**	lowvds_wait							
0X37	**PP_CFG**	asat_on				asat_fil			
0X38	**SEQ1_SUB12_PP**	mod1_seq1_sub1_pp		mod2_seq1_sub1_pp		mod1_seq1_sub2_pp		mod2_seq1_sub2_pp	
0X39	**SEQ1_SUB34_PP**	mod1_seq1_sub3_pp		mod2_seq1_sub3_pp		mod1_seq1_sub4_pp		mod2_seq1_sub4_pp	

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0X3A	**SEQ1_SUB56_PP**	mod1_seq1_sub5_pp		mod2_seq1_sub5_pp		mod1_seq1_sub6_pp		mod2_seq1_sub6_pp	
0X3B	**SEQ1_SUB78_PP**	mod1_seq1_sub7_pp		mod2_seq1_sub7_pp		mod1_seq1_sub8_pp		mod2_seq1_sub8_pp	
0X3C	**SEQ2_SUB12_PP**	mod1_seq2_sub1_pp		mod2_seq2_sub1_pp		mod1_seq2_sub2_pp		mod2_seq2_sub2_pp	
0X3D	**SEQ2_SUB34_PP**	mod1_seq2_sub3_pp		mod2_seq2_sub3_pp		mod1_seq2_sub4_pp		mod2_seq2_sub4_pp	
0X3F	**IRQ_ENABLE**	irq_en_prox_on	irq_en_prox_off	irq_en_vcsel	irq_en_asat	irq_en_led_lowvds	irq_en_fifooverflow	irq_en_fifotreshold	irq_en_sequencer
0X40	**SEQ_SAMPLE**	seq_sample							
0X41	**SEQ_SUB_WAIT**	sub_wait							
0X42	**SEQ_MODCONF**				mod_reset_delay			modclk	
0X43	**SEQ_CONFIG**	seq2_en		seq2_sub_sample		seq1_en	seq1_sub_sample		
0X44	**SEQ_SAR_WAIT**	sar_wait							
0X45	**SEQ_LED_INIT**	led_init							
0X46	**SEQ_FREQL**	seq_freq[7:0]							
0X47	**SEQ_FREQH**	seq_freq[15:8]							
0X48	**SEQ1_FREQDIVL**	seq1_freqdiv[7:0]							
0X49	**SEQ1_FREQDIVH**	seq1_freqdiv[15:8]							
0X4A	**SEQ2_FREQDIVL**	seq2_freqdiv[7:0]							
0X4B	**SEQ2_FREQDIVH**	seq2_freqdiv[15:8]							
0X4C	**MOD1_SEQ1_SUB_EN**	mod1_seq1_sub_en							
0X4D	**MOD1_SEQ2_SUB_EN**					mod1_seq2_sub_en			
0X4E	**MOD2_SEQ1_SUB_EN**	mod2_seq1_sub_en							
0X4F	**MOD2_SEQ2_SUB_EN**					mod2_seq2_sub_en			
0X50	**SEQ1_MODE_A**	seq1_sub1_mode		seq1_sub2_mode		seq1_sub3_mode		seq1_sub4_mode	
0X51	**SEQ1_MODE_B**	seq1_sub5_mode		seq1_sub6_mode		seq1_sub7_mode		seq1_sub8_mode	
0X52	**SEQ2_MODE**	seq2_sub1_mode		seq2_sub2_mode		seq2_sub3_mode		seq2_sub4_mode	
0X53	**PD_SEQ1_SUB1**		mod1_seq1_sub1_pdsel			mod2_seq1_sub1_pdsel			

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0X54	**PD_SEQ1_SUB2**		mod1_seq1_sub2_pdsel			mod2_seq1_sub2_pdsel			
0X55	**PD_SEQ1_SUB3**		mod1_seq1_sub3_pdsel			mod2_seq1_sub3_pdsel			
0X56	**PD_SEQ1_SUB4**		mod1_seq1_sub4_pdsel			mod2_seq1_sub4_pdsel			
0X57	**PD_SEQ1_SUB5**		mod1_seq1_sub5_pdsel			mod2_seq1_sub5_pdsel			
0X58	**PD_SEQ1_SUB6**		mod1_seq1_sub6_pdsel			mod2_seq1_sub6_pdsel			
0X59	**PD_SEQ1_SUB7**		mod1_seq1_sub7_pdsel			mod2_seq1_sub7_pdsel			
0X5A	**PD_SEQ1_SUB8**		mod1_seq1_sub8_pdsel			mod2_seq1_sub8_pdsel			
0X5B	**PD_SEQ2_SUB1**		mod1_seq2_sub1_pdsel			mod2_seq2_sub1_pdsel			
0X5C	**PD_SEQ2_SUB2**		mod1_seq2_sub2_pdsel			mod2_seq2_sub2_pdsel			
0X5D	**PD_SEQ2_SUB3**		mod1_seq2_sub3_pdsel			mod2_seq2_sub3_pdsel			
0X5E	**PD_SEQ2_SUB4**		mod1_seq2_sub4_pdsel			mod2_seq2_sub4_pdsel			
0X5F	**PDSEL_CFG**								pdref_sel
0X61	**SEQ1_SINC_CFGA**	seq1_sinc_ovs			seq1_sinc_dec				
0X62	**SEQ1_SINC_CFGB**		seq1_os_delay					seq1_sel_order	seq1_filter_mode
0X63	**SEQ1_SINC_CFGC**	seq1_start_delay							
0X64	**SEQ2_SINC_CFGA**	seq2_sinc_ovs			seq2_sinc_dec				
0X65	**SEQ2_SINC_CFGB**		seq2_os_delay					seq2_sel_order	seq2_filter_mode
0X66	**SEQ2_SINC_CFGC**	seq2_start_delay							
0X70	**AOC_MOD1_SEQ1_SUB1**	aoc_mod1_seq1_sub1							
0X71	**AOC_MOD1_SEQ1_SUB2**	aoc_mod1_seq1_sub2							
0X72	**AOC_MOD1_SEQ1_SUB3**	aoc_mod1_seq1_sub3							
0X73	**AOC_MOD1_SEQ1_SUB4**	aoc_mod1_seq1_sub4							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0X74	**AOC_MOD1_SEQ1_SUB5**	aoc_mod1_seq1_sub5							
0X75	**AOC_MOD1_SEQ1_SUB6**	aoc_mod1_seq1_sub6							
0X76	**AOC_MOD1_SEQ1_SUB7**	aoc_mod1_seq1_sub7							
0X77	**AOC_MOD1_SEQ1_SUB8**	aoc_mod1_seq1_sub8							
0X78	**AOC_MOD1_SEQ2_SUB1**	aoc_mod1_seq2_sub1							
0X79	**AOC_MOD1_SEQ2_SUB2**	aoc_mod1_seq2_sub2							
0X7A	**AOC_MOD1_SEQ2_SUB3**	aoc_mod1_seq2_sub3							
0X7B	**AOC_MOD1_SEQ2_SUB4**	aoc_mod1_seq2_sub4							
0X7C	**AOC_MOD2_SEQ1_SUB1**	aoc_mod2_seq1_sub1							
0X7D	**AOC_MOD2_SEQ1_SUB2**	aoc_mod2_seq1_sub2							
0X7E	**AOC_MOD2_SEQ1_SUB3**	aoc_mod2_seq1_sub3							
0X7F	**AOC_MOD2_SEQ1_SUB4**	aoc_mod2_seq1_sub4							
0X80	**AOC_MOD2_SEQ1_SUB5**	aoc_mod2_seq1_sub5							
0X81	**AOC_MOD2_SEQ1_SUB6**	aoc_mod2_seq1_sub6							
0X82	**AOC_MOD2_SEQ1_SUB7**	aoc_mod2_seq1_sub7							
0X83	**AOC_MOD2_SEQ1_SUB8**	aoc_mod2_seq1_sub8							
0X84	**AOC_LEDOFF**	aoc_ledoff							
0X85	**AOC_CFG**				dis_ledoff		aoc_ovs		
0X86	**AOC_MOD1_THH**	aoc_mod1_thh							
0X87	**AOC_MOD1_THL**	aoc_mod1_thl							

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0X88	**AOC_MOD2_THH**	aoc_mod2_thh							
0X89	**AOC_MOD2_THL**	aoc_mod2_thl							
0X8A	**AOC_SAR_THRES**	sar_thres							
0X8B	**MOD1_SEQ1_AOC_EN**	mod1_seq1_aoc_en							
0X8C	**MOD2_SEQ1_AOC_EN**							mod2_seq1_aoc_en	
0X98	**PROX_CFG**				prox_en			prox_sub	
0X99	**PROX_OVS**		prox_on_ovs				prox_off_ovs		
0X9A	**PROX_THH_L**	prox_thh[7:0]							
0X9B	**PROX_THH_H**	prox_thh[15:8]							
0X9C	**PROX_THL_L**	prox_thl[7:0]							
0X9D	**PROX_THL_H**	prox_thh[15:8]							
0XA0	**STANDBY_ON**		stby_en_on						
0XA1	**STANDBY_EN1**	stby_en1_time							
0XA2	**STANDBY_EN2**	stby_en2_time							
0XA3	**STANDBY_EN3**	stby_en3_time							
0XA4	**STANDBY_EN4**	stby_en4_time							
0XA5	**STANDBY_EN5**	stby_en5_time							
0XA6	**STANDBY_EN6**	stby_en6_time1			stby_en6_time2				
0XA7	**STANDBY_EN7**	stby_en7_time1			stby_en7_time2				
0XD0	**FIFO_TRESHOLD**	fifo_treshold[7:0]							
0XD1	**FIFO_CTRL**	fifo_clear				sar_data_en			fifo_treshold[8]
0XEC	**PRODUCT_ID**	otp_part_id							
0XED	**SILICON_ID**	silicon_id							
0XEE	**REVISION**					revision			
0XEF	**CHIP_CTRL**								chip_reset
0XF0	**SEQ_START**								seq_start
0XF4	**STATUS_CGBB**					pll_lock	clk_pll_ok	lf_bgcal_ok	lf_bgcal_ready

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0XF5	**STATUS_SEQ**							seq_end	seq_error
0XF6	**STATUS_LED**						led_lowvds		
0XF7	**STATUS_ASAT**	mod1_asat				mod2_asat			
0XF8	**STATUS_VCSEL**						vcsel_short_vss	vcsel_short_vdd	vcsel_wd
0XF9	**STATUS_PROX**		prox_high	prox_high_on	prox_high_off		prox_low	prox_low_on	prox_low_off
0XFA	**STATUS**	irq_prox	irq_vcsel	irq_asat	irq_led_lowvds	irq_fifooverflow	irq_fifotreshold		irq_sequencer
0XFB	**FIFO_LEVEL0**	fifo_level[7:0]							
0XFC	**FIFO_LEVEL1**						fifo_overflow	fifo_level[9:8]	
0XFD	**FIFOL**	fifol							
0XFE	**FIFOM**	fifom							
0XFF	**FIFOH**	fifoh							

7 Functional Description

The AS7056 Biosignal Sensor AFE is a low-power solution for photoplethysmogram (PPG) signal acquisition, used in optical vital sign sensing applications such as heart-rate, blood oxygen saturation, and blood pressure monitoring. The AS7056 provides two low-noise current sensing channels and can sense two PPG signals simultaneously.

The AS7056 is optimized for biosignal-sensing products with the following strengths:

- Low noise, high dynamic range PPG acquisition
- Simultaneous sampling by two PPG channels
- Small size
- LED/VCSEL drivers
- Proximity detection
- Automatic offset cancellation
- Temperature and power supply monitoring
- Low power consumption

The AS7056 Biosignal Sensor AFE contains two main blocks. An analog front-end for LED driving, signal acquisition, photodiode selection, and signal preconditioning. Moreover, a digital backend for signal filtering, balancing, and sampling. Furthermore, the digital block will handle the sensor configuration, control, and communication to the external MCU.

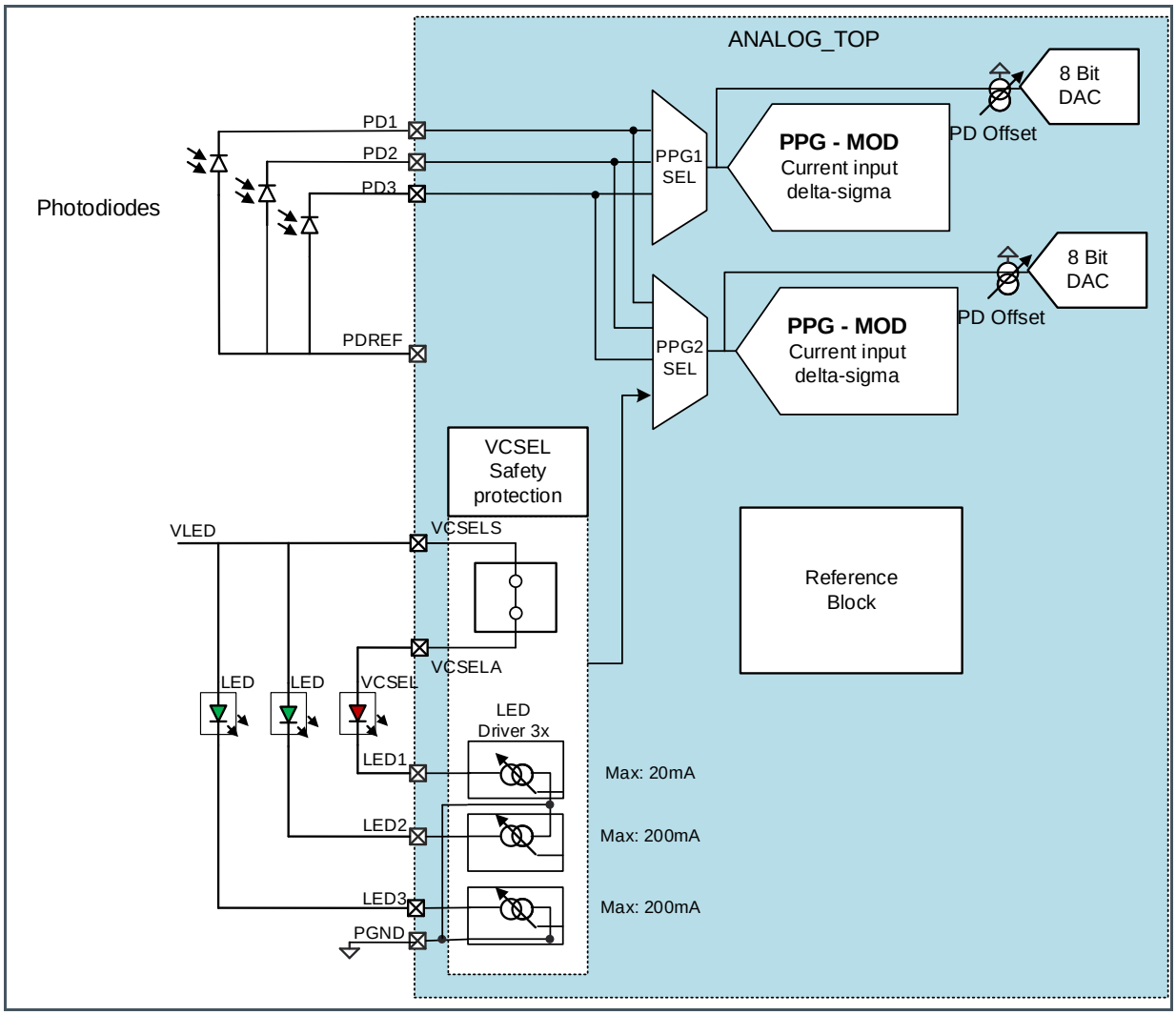
The I^2C interface controls all the functions of the AS7056. All the functions can be controlled with an external MCU via the I^2C interface if the AS7056 is in active mode.

7.1 Analog Blocks

The AS7056 analog frontend includes the following main functional blocks:

- LED/VCSEL Drivers
- VCSEL safety protection
- PPG front-end
  - PD Selection
  - PD Offset
  - PPG-ADC - Current input ADC for PPG
- Reference Block - Generates all internal references.

Figure 8:
Analog Block Diagram

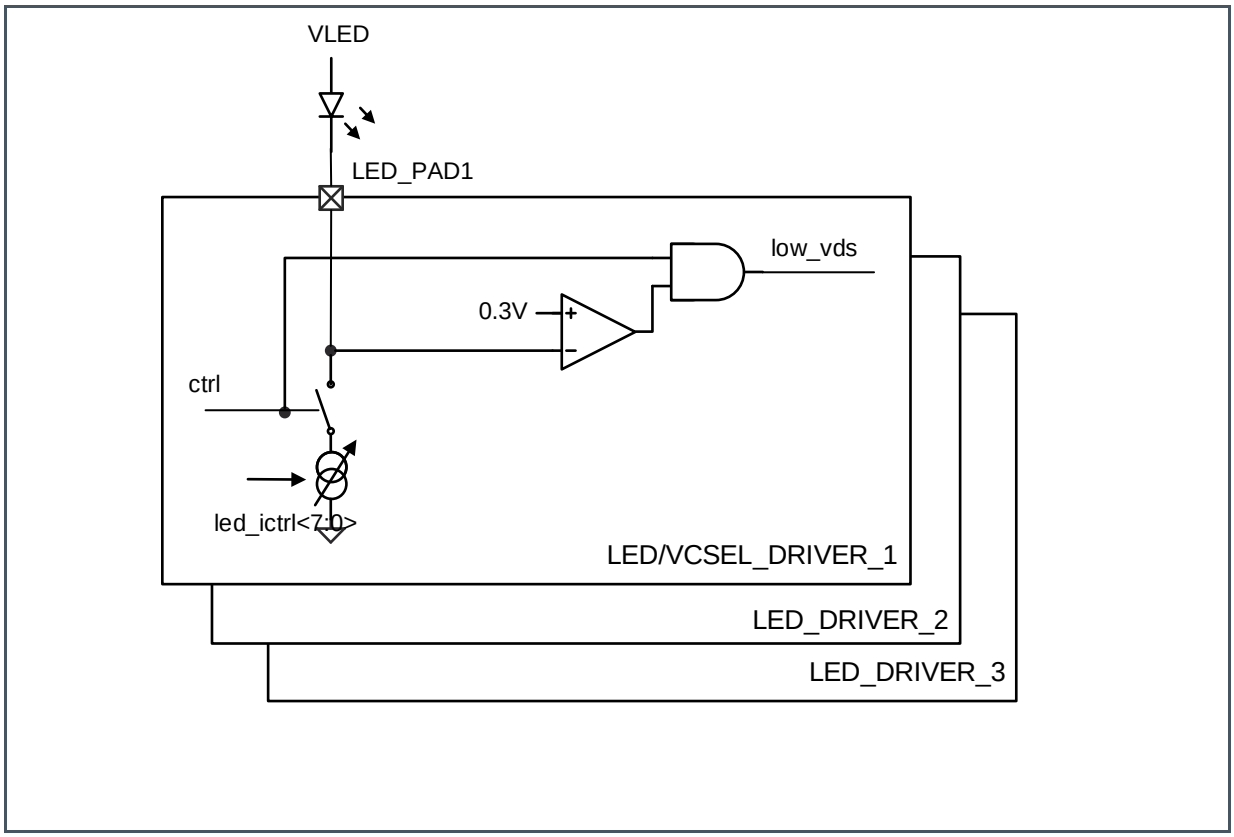


7.1.1 LED/VCSEL Drivers

The AS7056 Biosignal AFE controls two internal LEDs and one VCSEL driver. The drivers will be controlled and configured via a digital sequencer.

The LED/VCSEL1 driver can be configured for a maximum current of 20 mA. The other two drivers have a maximum current of 200 mA. The 200 mA LED drivers can be adjusted in 128 steps and the 20 mA VCSEL driver in 64 steps.

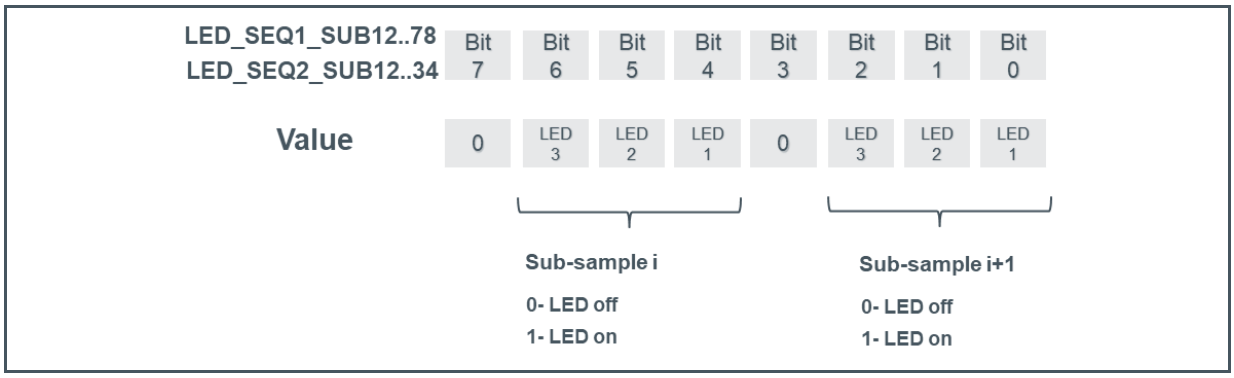
Figure 9:
LED/VCSEL Drivers



Two register sets can be used to configure the LED/VCSEL selection in the subsamples of measurement sequences and the LED/VCSEL current.

Six registers, as shown below, are used to select which LED/VCSEL, out of the available three, should be connected to which subsample and subsequence. Each LED or VCSEL could be connected to any subsample inside sequence 1 and sequence 2. The figure below shows a general 8-bit register. Bit 6:4 corresponds to one subsample and bit 2:0 to the adjacent subsample. For instance, for the register LED_SEQ1_SUB12, we have: bit 7 set to zero, bit 6 corresponds to LED3 in subsample 1, bit 5 to LED2 in subsample 1, and bit 4 to LED/VCSEL 1 in subsample 1. Bit 7 and 3 remain unused and set to zero. Just like bits 6:4, bits 2:0 correspond to LED3, LED2, and LED/VCSEL1 respectively, but for subsample 2.

Figure 10:
LED/VCSEL Selection



The LED/VCEL current of each LED can also be programmed. Note that the LED current can be programmed for each sequence but not for each subsample. As shown in the register description below, bit 7 remains unused. For instance, SEQ1_LED1_CURR is used to set the current of LED1 for sequence 1. All subsamples inside sequence 1 will have to measure the same LED1 current. The output current for the different LEDs and the VCSEL can be given as:

$$I_{OUT} = SEQ_X\_LED_Y\_CURR\big|_{dec} \times \frac{I_{OUT\_MAX}}{64}\Bigg|_{Y=1}$$

$$I_{OUT} = SEQ_X\_LED_Y\_CURR\big|_{dec} \times \frac{I_{OUT\_MAX}}{128}\Bigg|_{Y=2,3}$$

In the above equation, I_{OUT_MAX} is 200mA for LED2 and LED3. For LED/VCSEL1 the I_{OUT_MAX} is given as 20 mA.

SEQ1_LED1_CURR Register (Address 0x29)

Figure 11:
SEQ1_LED1_CURR Register

Addr: 0x29		SEQ1_LED1_CURR		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:0	seq1_led1_curr	0	RW	Current for LED1 in Sequence1; LED1 Current range 0.3125 mA … 20 mA for Seqx_led1_curr=0..63 (1LSB=20 mA/64=3.3125 mA)

SEQ2_LED1_CURR Register (Address 0x2a)

Figure 12:
SEQ2_LED1_CURR Register

Addr: 0x2a		SEQ2_LED1_CURR		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:0	Seq2_led1_curr	0	RW	Current for LED1 in Sequence2.

SEQ1_LED2_CURR Register (Address 0x2b)

Figure 13:
SEQ1_LED2_CURR Register

Addr: 0x2b		SEQ1_LED2_CURR		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:0	seq1_led2_curr	0	RW	Current for LED2 in Sequence1.

SEQ2_LED2_CURR Register (Address 0x2c)

Figure 14:
SEQ2_LED2_CURR Register

Addr: 0x2c		SEQ2_LED2_CURR		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:0	Seq2_led2_curr	0	RW	Current for LED2 in Sequence2.

SEQ1_LED3_CURR Register (Address 0x2d)

Figure 15:
SEQ1_LED3_CURR Register

Addr: 0x2d		SEQ1_LED3_CURR		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:0	seq1_led3_curr	0	RW	Current for LED3 in Sequence1.

SEQ2_LED3_CURR Register (Address 0x2e)

Figure 16:
SEQ2_LED3_CURR Register

Addr: 0x2e		SEQ2_LED3_CURR		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:0	Seq2_led3_curr	0	RW	Current for LED3 in Sequence2.

LED_SEQ1_SUB12 Register (Address 0x2f)

Figure 17:
LED_SEQ1_SUB12 Register

Addr: 0x2f		LED_SEQ1_SUB12			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
6:4	led_seq1_sub1	0	RW	Select LED for SubSample1 in Sequence1.	
				Bit	**LED**
				0	Off
				1	On
2:0	led_seq1_sub2	0	RW	Select LED for SubSample2 in Sequence1.	
				Bit	**LED**
				0	Off
				1	On

LED_SEQ1_SUB34 Register (Address 0x30)

Figure 18:
LED_SEQ1_SUB34 Register

Addr: 0x30		LED_SEQ1_SUB34		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:4	led_seq1_sub3	0	RW	Select LED for SubSample3 in Sequence1. **Bit** **LED** 0 Off 1 On
2:0	led_seq1_sub4	0	RW	Select LED for SubSample4 in Sequence1. **Bit** **LED** 0 Off 1 On

LED_SEQ1_SUB56 Register (Address 0x31)

Figure 19:
LED_SEQ1_SUB56 Register

Addr: 0x31		LED_SEQ1_SUB56		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:4	led_seq1_sub5	0	RW	Select LED for SubSample5 in Sequence1. **Bit** **LED** 0 Off 1 On
2:0	led_seq1_sub6	0	RW	Select LED for SubSample6 in Sequence1. **Bit** **LED** 0 Off 1 On

LED_SEQ1_SUB78 Register (Address 0x32)

Figure 20:
LED_SEQ1_SUB78 Register

Addr: 0x32		LED_SEQ1_SUB78		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:4	led_seq1_sub7	0	RW	Select LED for SubSample7 in Sequence1. **Bit** **LED** 0 Off 1 On
2:0	led_seq1_sub8	0	RW	Select LED for SubSample8 in Sequence1. **Bit** **LED** 0 Off 1 On

LED_SEQ2_SUB12 Register (Address 0x33)

Figure 21:
LED_SEQ2_SUB12 Register

Addr: 0x33		LED_SEQ2_SUB12		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:4	led_seq2_sub1	0	RW	Select LED for SubSample1 in Sequence2. **Bit** **LED** 0 Off 1 On
2:0	led_seq2_sub2	0	RW	Select LED for SubSample2 in Sequence2. **Bit** **LED** 0 Off 1 On

LED_SEQ2_SUB34 Register (Address 0x34)

Figure 22:
LED_SEQ2_SUB34 Register

Addr: 0x34		LED_SEQ1_SUB34			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
6:4	led_seq2_sub3	0	RW	Select LED for SubSample3 in Sequence2.	
				Bit	**LED**
				0	Off
				1	On
2:0	led_seq2_sub4	0	RW	Select LED for SubSample4 in Sequence2.	
				Bit	**LED**
				0	Off
				1	On

LED_LOWVDS_WAIT Register (Address 0x35)

Figure 23:
LED_LOWVDS_WAIT Register

Addr: 0x35		LED_LOWVDS_WAIT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	lowvds_wait	0	RW	The LOWVDS_WAIT defines the time between switching on a LED and the start of voltage monitoring. All LEDs use the same time. time = lowvds_wait * 1 µs

VCSEL Safety Protection

The VCSEL safety protection provides the functional monitoring of the VCSEL/LED1 driver.

It can detect short circuits of the VCSEL diode on pin LED/VCSEL1 to the ground and monitors the on-time of the VCSEL LED.

To enable the error detection, the VCSEL diode, which has to be monitored, must be connected between the pins LED/VCSEL1 and VCSELA.

The short-circuit detection is done automatically before the start of a measurement. If a short circuit is detected, the subsequent measurement does not start.

The monitoring of the LED On-Time is activated when the LED is switched on. If the On-Time exceeds the limit of the maximum On-Time (typ. 3 ms), the LED will be switched off.

All safety functions can be configured via I^2C registers and the status will be displayed in the status registers.

VCSEL_CFG Register (Address 0x28)

Figure 24:
VCSEL_CFG Register

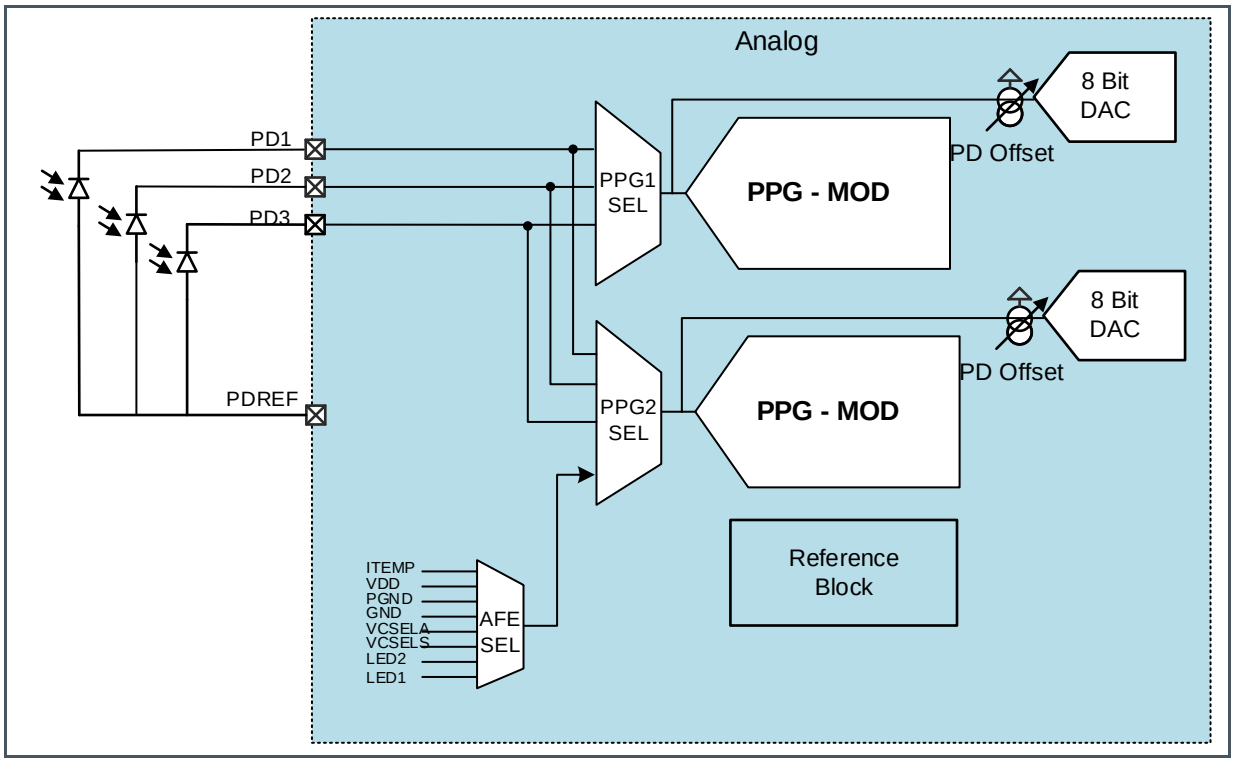
Addr: 0x28		VCSEL_CFG			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	vcsel_wd_disable	0	RW	Disable VCSEL/LED watchdog.	
6	vcsel_safety_disable	0	RW	Disable the safety control logic evaluation of the short to VSS/VDD signals.	
5:4	vcsel_vrsel	0	RW	Selection of the reference voltage for the comparators.	
				Number	**Function**
				0	50 mV
				1	100 mV
				2	150 mV
				3	200 mV
3:2	vcsel_short_vdd_wait	0	RW	The short_vdd_wait defines the time between switching on Short detection and the valid result. All VCSEL LEDs use the same time.	
				Number	**Function**
				0	2 µs
				1	4 µs
				2	8 µs
				3	12 µs

Addr: 0x28		VCSEL_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1:0	vcsel_short_vss_wait	0	RW	The short_vss_wait defines the time between switching on Short detection and the valid result. All VCSEL LEDs use the same time. **Number** / **Function** 0 / 2 µs 1 / 4 µs 2 / 8 µs 3 / 12 µs

7.1.2 Analog PPG Frontends

The PPG frontends consist of three main functional blocks: photodiode (PD) selection, PD offset, and the PPG ADC. The PD selection supports up to three different photodiodes. The photodiodes are connected via a multiplexer to the PPG ADC. To minimize daylight impacts, the photodiode input currents can be compensated by the PD offset. After amplifying and converting the PD currents, the digital PD output signals pass to the digital PPG filter inside the digital block of the AS7056.

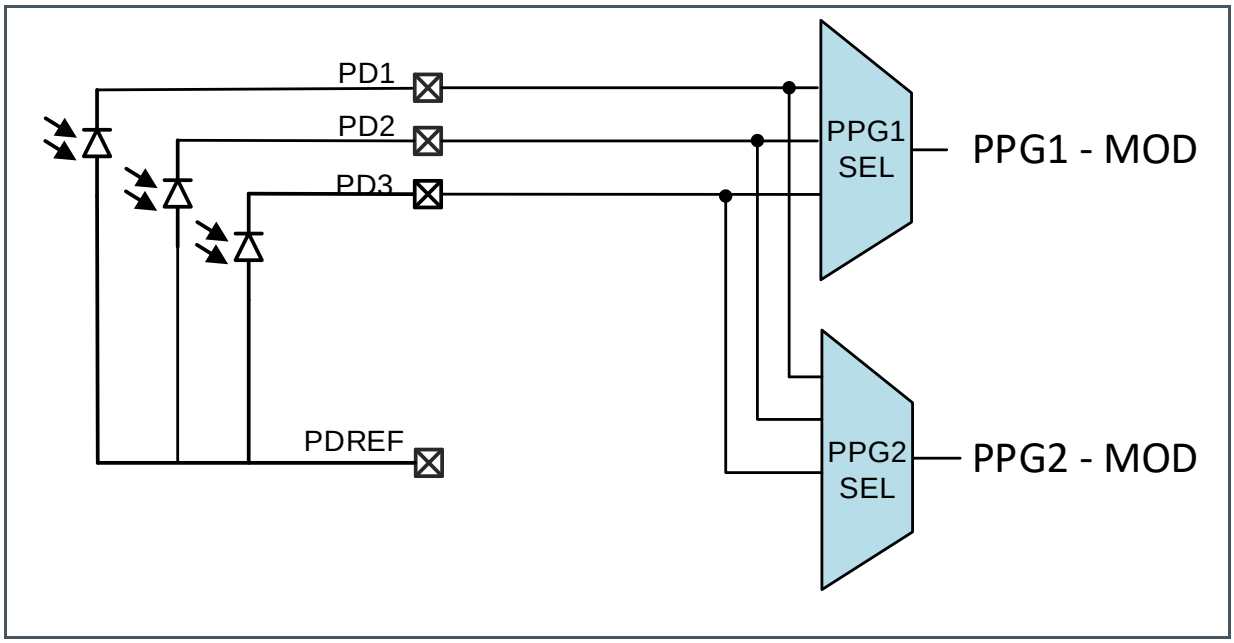
Figure 25:
Analog PPG Frontend



7.1.3 PPG Selection

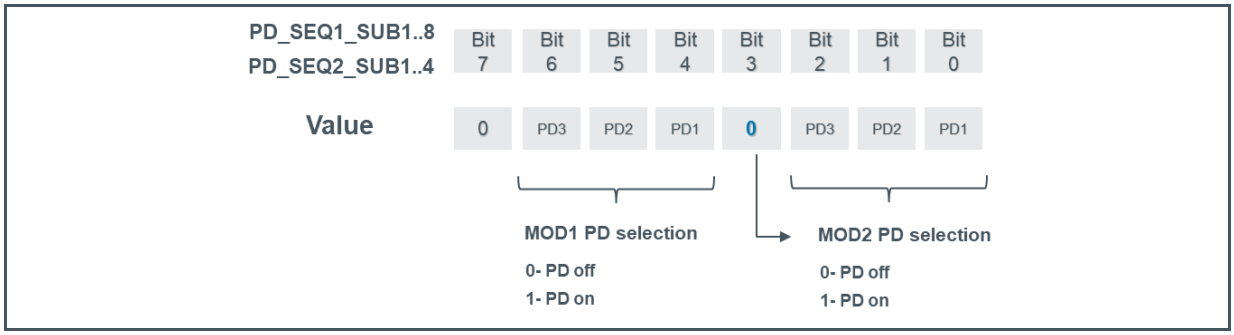
The PPG selection is independently controlled by the sequencer for each time slot. It is used to connect the photodiodes to the PPG ADCs.

Figure 26:
PPG Selection



Each of the three photodiodes can be connected to PPG1-MOD or PPG2-MOD. The generic form of the register can be written as PD_SEQx_SUBy, where “x” shows the sequence number for each channel and “y” shows the subsample number inside each sequence. In the default mode, bit 7 and bit 3 remain set to zero. Bits 6:4 are used to select the PDs for MOD1, while bits 2:0 are used to select the PDs for MOD2. For MOD1, bit 6 corresponds to PD3, bit 5 corresponds to PD2, and bit 4 to PD1. Similarly, bit 2:0 is used for MOD2 as shown in Figure 27 below. PD3, PD2, and PD1 are different photodiodes and occupy different positions on the evaluation board.

Figure 27:
Photodiode Selection



The table below (Figure 28) shows the connection of the PD3, PD2, and PD1 to MOD1, MOD2, and the corresponding binary and hexadecimal code. If two or all three PDs are connected to MOD1 or MOD2, they must be interleaved in time, since at a specified time, only one MOD can be connected to

a PD. However, two different PDs can be simultaneously connected to different MODs. For instance, PD1 and PD2 can be simultaneously applied to MOD1 and MOD2 respectively.

Figure 28:
Photodiode Selection Settings

Synchronous / Time Interleaved	PD_SEQx_SUBy Photodiode Selection			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3=0	Bit 2	Bit 1	Bit 0	PD_SEQx_SUBy
hex	PD3	PD2	PD1									hex
T	-	-	-	0	0	0	0	0	0	0	0	0x00
T	-	-	MOD1	0	0	0	1	0	0	0	0	0x10
T	-	-	MOD2	0	0	0	0	0	0	0	1	0x01
T	-	MOD1	-	0	0	1	0	0	0	0	0	0x20
T	-	MOD1	MOD1	0	0	1	1	0	0	0	0	0x30
S	-	MOD1	MOD2	0	0	1	0	0	0	0	1	0x21
T	-	MOD2	-	0	0	0	0	0	0	1	0	0x02
S	-	MOD2	MOD1	0	0	0	1	0	0	1	0	0x12
T	-	MOD2	MOD2	0	0	0	0	0	0	1	1	0x03
T	MOD1	-	-	0	1	0	0	0	0	0	0	0x40
T	MOD1	-	MOD1	0	1	0	1	0	0	0	0	0x50
S	MOD1	-	MOD2	0	1	0	0	0	0	0	1	0x41
T	MOD1	MOD1	-	0	1	1	0	0	0	0	0	0x60
T	MOD1	MOD1	MOD1	0	1	1	1	0	0	0	0	0x70
S	MOD1	MOD1	MOD2	0	1	1	0	0	0	0	1	0x61
S	MOD1	MOD2	-	0	1	0	0	0	0	1	0	0x42
S	MOD1	MOD2	MOD1	0	1	0	1	0	0	1	0	0x52
S	MOD1	MOD2	MOD2	0	1	0	0	0	0	1	1	0x43
T	MOD2	-	-	0	0	0	0	0	1	0	0	0x04
S	MOD2	-	MOD1	0	0	0	1	0	1	0	0	0x14
T	MOD2	-	MOD2	0	0	0	0	0	1	0	1	0x05
S	MOD2	MOD1	-	0	0	1	0	0	1	0	0	0x24
S	MOD2	MOD1	MOD1	0	0	1	1	0	1	0	0	0x34
S	MOD2	MOD1	MOD2	0	0	1	0	0	1	0	1	0x25
T	MOD2	MOD2	-	0	0	0	0	0	1	1	0	0x06
S	MOD2	MOD2	MOD1	0	0	0	1	0	1	1	0	0x16
T	MOD2	MOD2	MOD2	0	0	0	0	0	1	1	1	0x07

MOD1 is configured to be connected only to the PDs and not any external voltage, while MOD2 can be configured to be connected to either the PDs or the external voltages. To connect MOD2 to an external voltage, bit 3 has to be set to one inside the PD_SEQx_SUBy register.

Figure 29 below shows bit 3 of the PD_SEQx_SUBy register set to logic high. In this case, bit 2:0 decides which of the external voltages will be connected to the MOD2. The PDs current and the external voltages can be simultaneously measured via MOD1 and MOD2 respectively.

Figure 29:
Bit 3 Enabled External Voltage

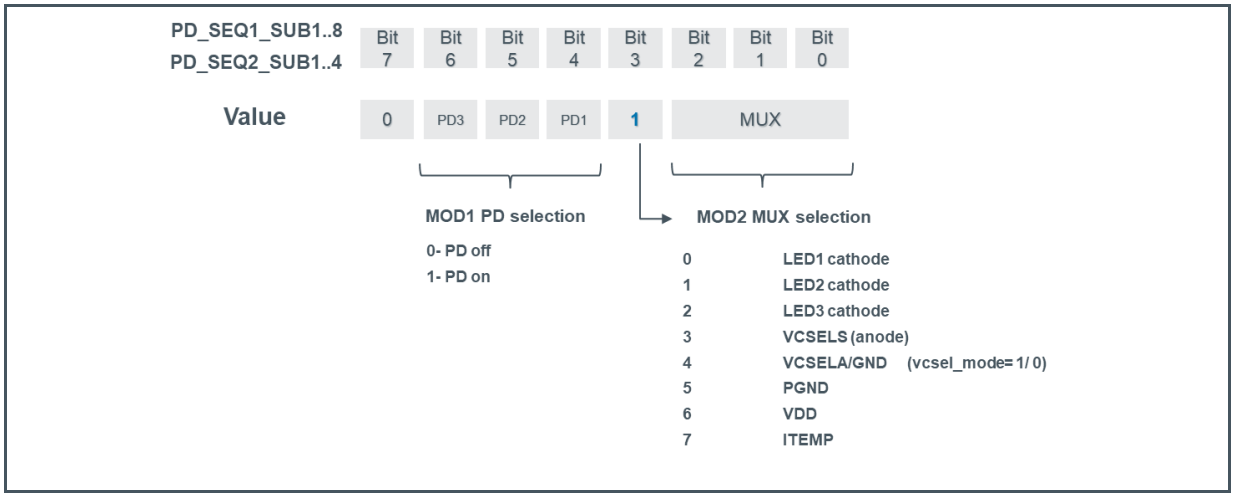


Figure 30:
PD_SEQx_SUBy Photodiode Settings

PD_SEQx_SUBy PD Selection			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PD3	PD2	PD1								
-	-	-	0	0	0	0	1	0…7		
-	-	MOD1	0	0	0	1	1	0…7		
-	MOD1	-	0	0	1	0	1	0…7		
-	MOD1	MOD1	0	0	1	1	1	0…7		
MOD1	-	-	0	1	0	0	1	0…7		
MOD1	-	MOD1	0	1	0	1	1	0…7		
MOD1	MOD1	-	0	1	1	0	1	0…7		
MOD1	MOD1	MOD1	0	1	1	1	1	0…7		

In order to measure the analog input values (0:6) as described in Figure 30 above, two methods can be used:

- Ratio-metric method

- Slope-based method

Ratio-Metric Method:

This method is preferred over the slope-based method because, in this case, two measurements are taken over the same channel, thereby eliminating the effect of AGAIN values, gain error, and offset error during measurements. For the selected voltage input, using bit 2:0 (0-6), a 250K Ohm resistor converts it into a current, which is applied at the input of MOD2. One end of this resistor is connected to VCM (input port of MOD2), while the other end is to one of the voltages to be measured.

1. First, measure the VCSELA/GND by setting a decimal value of 4 in the above register. The twenty bit signed ADC output (d0 d1 d2 ... d19) for this register setting can then be converted into its analog counterpart as shown below:

$$ADC_{OUT\_GND} = \frac{d1}{2^1} + \frac{d2}{2^2} + ... + \frac{d19}{2^{19}}$$

or

$$ADC_{OUT\_GND} = \frac{d1 \times 2^{N-1} + d2 \times 2^{N-2} + ... + d19 \times 2^{N-N}}{2^N}$$

Note that the above formulae do not include d0 or MSB, which serves as a "*sign*" bit for the signed binary output. The above formulae scale the digital output into its analog counterpart part between zero and one.

2. Afterwards, set the register to a value required for measuring the voltages, such as LED1, and scale the ADC output into its analog counterpart, ADC_{OUT}, as done in step 1, and use the following formulae to estimate the input voltage:

$$V_{IN} = VCM\left(1 - \frac{ADC_{OUT}}{ADC_{OUT\_GND}}\right)$$

If V_{IN} is connected to ground, ADC_{OUT} is equal to ADC_{OUT_GND}. If V_{IN} is the same as VCM, ADC_{OUT} is equivalent to zero input current.

Slope-Based Method:

This method requires us to use the slope for the given AGAIN value.

1. Once we know the reference slope, which can be measured using a DAC input, and the measured ADC output, ADC_{OUT}, we can find out the corresponding ADC input current ADC_{IN}:

$$ADC_{IN} = \frac{ADC_{OUT}}{SLOPE_{REF}}$$

2. Use this value of ADC_{IN} in the formulae below to calculate V_{IN}, which is one of the six external voltages applied:

$$V_{IN} = VCM - (ADC_{IN} \times 250K)$$

This method requires you to measure the current through the resistor, and depends on the gain and offset error of the ADC. Therefore, this method is not preferred.

PD_SEQ1_SUB1 Register (Address 0x53)

Figure 31:
PD_SEQ1_SUB1 Register

Addr: 0x53		PD_SEQ1_SUB1			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
6:4	mod1_seq1_sub1_pdsel	0	RW	Select the PD for Modulator1 in SubSample1/Sequence1.	
				Bit	**Function**
				0	PD will not be used
				1	PD will be used
3:0	mod2_seq1_sub1_pdsel	0	RW	Select an Input for Modulator2 in SubSample1/Sequence1.	
				Bit3	**Function**
				0	Select PD with bit(2:0)
				1	Select AFE
				Bit(2:0)	**Function (Bit3=0)**
				0	PD will not be used
				1	PD will be used
				Bit(2:0)	**Value (Bit3 =1)**
				0	LED1
				1	LED2
				2	LED3
				3	VCSELS
				4	VCSELA
				5	PGND
				6	VDD
				7	ITEMP

PD_SEQ1_SUB2 Register (Address 0x54)

Figure 32:
PD_SEQ1_SUB2 Register

Addr: 0x54		PD_SEQ1_SUB2			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
6:4	mod1_seq1_sub2_pdsel	0	RW	Select the PD for Modulator1 in SubSample2/Sequence1.	
				Bit	**Function**
				0	PD will not be used
				1	PD will be used
3:0	mod2_seq1_sub2_pdsel	0	RW	Select an Input for Modulator2 in SubSample2 / Sequence1.	
				Bit3	**Function**
				0	Select PD with bit(2:0)
				1	Select AFE
				Bit(2:0)	**Function (Bit3=0)**
				0	PD will not be used
				1	PD will be used
				Bit(2:0)	**Value (Bit3=1)**
				0	LED1
				1	LED2
				2	LED3
				3	VCSELS
				4	VCSELA
				5	PGND
				6	VDD
				7	ITEMP

PD_SEQ1_SUB3 Register (Address 0x55)

Figure 33:
PD_SEQ1_SUB3 Register

Addr: 0x55		PD_SEQ1_SUB3			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
6:4	mod1_seq1_sub3_pdsel	0	RW	Select the PD for Modulator1 in SubSample3/Sequence1.	
				Bit	**Function**
				0	PD will not be used
				1	PD will be used
3:0	mod2_seq1_sub3_pdsel	0	RW	Select an Input for Modulator2 in SubSample3/Sequence1.	
				Bit3	**Function**
				0	Select PD with bit(2:0)
				1	Select AFE
				Bit(2:0)	**Function (Bit3=0)**
				0	PD will not be used
				1	PD will be used
				Bit(2:0)	**Value (Bit3=1)**
				0	LED1
				1	LED2
				2	LED3
				3	VCSELS
				4	VCSELA
				5	PGND
				6	VDD
				7	ITEMP

PD_SEQ1_SUB4 Register (Address 0x56)

Figure 34:
PD_SEQ1_SUB4 Register

Addr: 0x56		PD_SEQ1_SUB4			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
6:4	mod1_seq1_sub4_pdsel	0	RW	Select the PD for Modulator1 in SubSample4/Sequence1.	
				Bit	**Function**
				0	PD will not be used
				1	PD will be used
3:0	mod2_seq1_sub4_pdsel	0	RW	Select an Input for Modulator2 in SubSample4/Sequence1.	
				Bit3	**Function**
				0	Select PD with bit(2:0)
				1	Select AFE
				Bit(2:0)	**Function (Bit3=0)**
				0	PD will not be used
				1	PD will be used
				Bit(2:0)	**Value (Bit3=1)**
				0	LED1
				1	LED2
				2	LED3
				3	VCSELS
				4	VCSELA
				5	PGND
				6	VDD
				7	ITEMP

PD_SEQ1_SUB5 Register (Address 0x57)

Figure 35:
PD_SEQ1_SUB5 Register

Addr: 0x57		PD_SEQ1_SUB5			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
6:4	mod1_seq1_sub5_pdsel	0	RW	Select the PD for Modulator1 in SubSample5/Sequence1.	
				Bit	**Function**
				0	PD will not be used
				1	PD will be used
3:0	mod2_seq1_sub5_pdsel	0	RW	Select an Input for Modulator2 in SubSample5/Sequence1.	
				Bit3	**Function**
				0	Select PD with bit(2:0)
				1	Select AFE
				Bit(2:0)	**Function (Bit3=0)**
				0	PD will not be used
				1	PD will be used
				Bit(2:0)	**Value (Bit3=1)**
				0	LED1
				1	LED2
				2	LED3
				3	VCSELS
				4	VCSELA
				5	PGND
				6	VDD
				7	ITEMP

PD_SEQ1_SUB6 Register (Address 0x58)

Figure 36:
PD_SEQ1_SUB6 Register

Addr: 0x58		PD_SEQ1_SUB6			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
6:4	mod1_seq1_sub6_pdsel	0	RW	Select the PD for Modulator1 in SubSample6/Sequence1.	
				Bit	**Function**
				0	PD will not be used
				1	PD will be used
3:0	mod2_seq1_sub6_pdsel	0	RW	Select an Input for Modulator2 in SubSample6/Sequence1.	
				Bit3	**Function**
				0	Select PD with bit(2:0)
				1	Select AFE
				Bit(2:0)	**Function (Bit3=0)**
				0	PD will not be used
				1	PD will be used
				Bit(2:0)	**Value (Bit3=1)**
				0	LED1
				1	LED2
				2	LED3
				3	VCSELS
				4	VCSELA
				5	PGND
				6	VDD
				7	ITEMP

PD_SEQ1_SUB7 Register (Address 0x59)

Figure 37:
PD_SEQ1_SUB7 Register

Addr: 0x59		PD_SEQ1_SUB7			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
6:4	mod1_seq1_sub7_pdsel	0	RW	Select the PD for Modulator1 in SubSample7/Sequence1.	
				Bit	**Function**
				0	PD will not be used
				1	PD will be used
3:0	mod2_seq1_sub7_pdsel	0	RW	Select an Input for Modulator2 in SubSample7/Sequence1.	
				Bit3	**Function**
				0	Select PD with bit(2:0)
				1	Select AFE
				Bit(2:0)	**Function (Bit3=0)**
				0	PD will not be used
				1	PD will be used
				Bit(2:0)	**Value (Bit3=1)**
				0	LED1
				1	LED2
				2	LED3
				3	VCSELS
				4	VCSELA
				5	PGND
				6	VDD
				7	ITEMP

PD_SEQ1_SUB8 Register (Address 0x5a)

Figure 38:
PD_SEQ1_SUB8 Register

Addr: 0x5a		PD_SEQ1_SUB8			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
6:4	mod1_seq1_sub8_pdsel	0	RW	Select the PD for Modulator1 in SubSample8/Sequence1.	
				Bit	**Function**
				0	PD will not be used
				1	PD will be used
3:0	mod2_seq1_sub8_pdsel	0	RW	Select an Input for Modulator2 in SubSample8/Sequence1.	
				Bit3	Function
				0	Select PD with bit(2:0)
				1	Select AFE
				Bit(2:0)	**Function (Bit3=0)**
				0	PD will not be used
				1	PD will be used
				Bit(2:0)	**Value (Bit3=1)**
				0	LED1
				1	LED2
				2	LED3
				3	VCSELS
				4	VCSELA
				5	PGND
				6	VDD
				7	ITEMP

PD_SEQ2_SUB1 Register (Address 0x5b)

Figure 39:
PD_SEQ2_SUB1 Register

Addr: 0x5b		PD_SEQ2_SUB1			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
6:4	mod1_seq2_sub1_pdsel	0	RW	Select the PD for Modulator1 in SubSample1/Sequence2.	
				Bit	**Function**
				0	PD will not be used
				1	PD will be used
3:0	mod2_seq2_sub1_pdsel	0	RW	Select an Input for Modulator2 in SubSample1/Sequence2.	
				Bit3	**Function**
				0	Select PD with bit(2:0)
				1	Select AFE
				Bit(2:0)	**Function (Bit3=0)**
				0	PD will not be used
				1	PD will be used
				Bit(2:0)	**Value (Bit3=1)**
				0	LED1
				1	LED2
				2	LED3
				3	VCSELS
				4	VCSELA
				5	PGND
				6	VDD
				7	ITEMP

PD_SEQ2_SUB2 Register (Address 0x5c)

Figure 40:
PD_SEQ1_SUB1 Register

Addr: 0x5c		PD_SEQ2_SUB2			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
6:4	mod1_seq2_sub2_pdsel	0	RW	Select the PD for Modulator1 in SubSample2/Sequence2.	
				Bit	**Function**
				0	PD will not be used
				1	PD will be used
3:0	mod2_seq2_sub2_pdsel	0	RW	Select an Input for Modulator2 in SubSample2/Sequence2.	
				Bit3	**Function**
				0	Select PD with bit(2:0)
				1	Select AFE
				Bit(2:0)	**Function (Bit3=0)**
				0	PD will not be used
				1	PD will be used
				Bit(2:0)	**Value (Bit3=1)**
				0	LED1
				1	LED2
				2	LED3
				3	VCSELS
				4	VCSELA
				5	PGND
				6	VDD
				7	ITEMP

PD_SEQ2_SUB3 Register (Address 0x5d)

Figure 41:
PD_SEQ2_SUB3 Register

Addr: 0x5d		PD_SEQ2_SUB3			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
6:4	mod1_seq2_sub3_pdsel	0	RW	Select the PD for Modulator1 in SubSample3/Sequence2.	
				Bit	**Function**
				0	PD will not be used
				1	PD will be used
3:0	mod2_seq2_sub3_pdsel	0	RW	Select an Input for Modulator2 in SubSample3/Sequence2.	
				Bit3	**Function**
				0	Select PD with bit(2:0)
				1	Select AFE
				Bit(2:0)	**Function (Bit3=0)**
				0	PD will not be used
				1	PD will be used
				Bit(2:0)	**Value (Bit3=1)**
				0	LED1
				1	LED2
				2	LED3
				3	VCSELS
				4	VCSELA
				5	PGND
				6	VDD
				7	ITEMP

PD_SEQ2_SUB4 Register (Address 0x5e)

Figure 42:
PD_SEQ2_SUB4 Register

Addr: 0x5e		PD_SEQ2_SUB4			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
6:4	mod1_seq2_sub4_pdsel	0	RW	Select the PD for Modulator1 in SubSample4/Sequence2.	
				Bit	**Function**
				0	PD will not be used
				1	PD will be used
3:0	mod2_seq2_sub4_pdsel	0	RW	Select an Input for Modulator2 in SubSample4/Sequence2.	
				Bit3	**Function**
				0	Select PD with bit(2:0)
				1	Select AFE
				Bit(2:0)	**Function (Bit3=0)**
				0	PD will not be used
				1	PD will be used
				Bit(2:0)	**Value (Bit3=1)**
				0	LED1
				1	LED2
				2	LED3
				3	VCSELS
				4	VCSELA
				5	PGND
				6	VDD
				7	ITEMP

PDSEL_CFG Register (Address 0x5f)

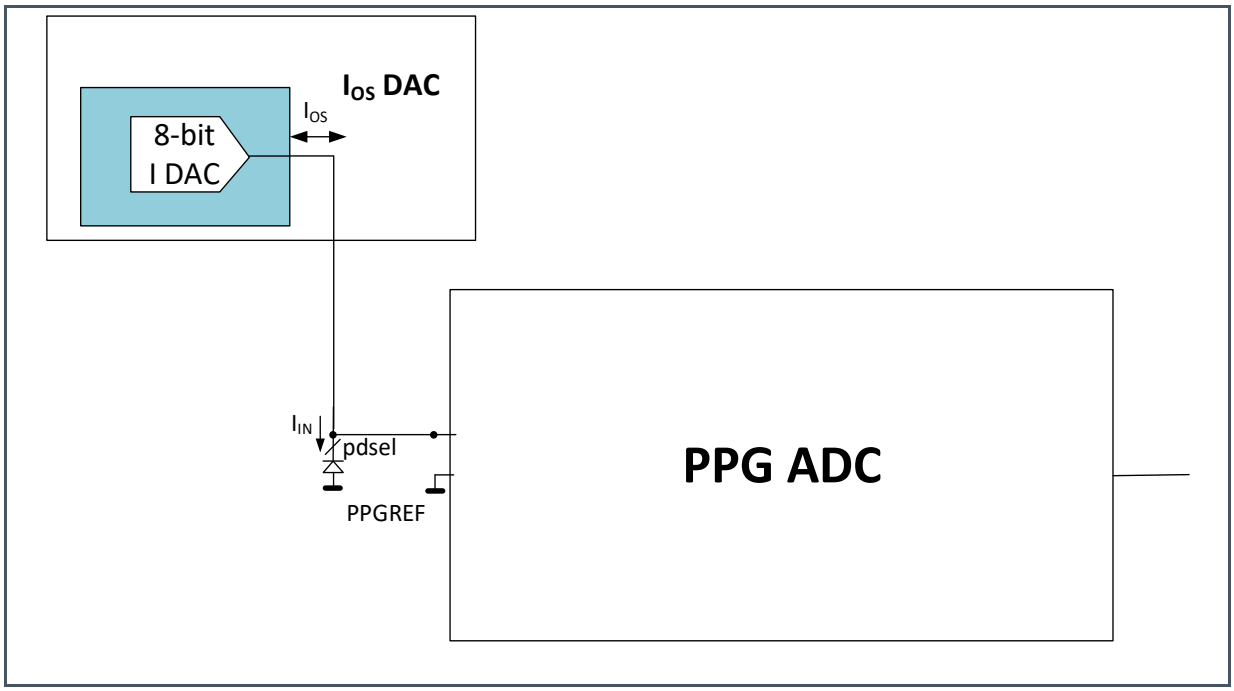
Figure 43:
PDSEL_CFG Register

Addr: 0x5f		PDSEL_CFG			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
0	pdref_sel	0	RW	Selection of PDREF Voltage.	
				Number	**Function**
				0	Connected to VCM_PPG
				1	Connected to VSSA

7.1.4 PD Offset

PD Offset is part of PPG ADC. It can be configured by digital registers or used as a part of an integrated AOC (Automated Offset Control) loop. The PD offset current is controlled by the 8-bit PPG DAC and has eight programmable ranges. The programmable offset current flows in an opposite direction of the photodiode DC and reduces the effective signal at the entrance of the PPG-Modulator. This enables the use of a more sensitive ADC signal range, resulting in a large number of PPG signal counts and better SNR compared to the case without offset correction. Furthermore, the AS7056 also offers the capability to adjust the PD offset during a running measurement.

Figure 44:
PPG DAC (Offset)



MODx_CGFA[2:0] is used to set the IOS DAC Full-Scale current independently from MOD1 and MOD2 as shown below. Setting the three bits to 111 enables the IOS DAC current up to 128 µA.

Figure 45:
IOS DAC Full-Scale Range (FSR)

				IOS_FS					
Register	**Address**	**Bit**	**Bit Name**	**4 µA**	**8 µA**	**16 µA**	**32 µA**	**64 µA**	**128 µA**
MOD1_CFGA	0x1b	2:0	mod1_ios_fs	2	3	4(1)	5	6	7
MOD2_CFGA	0x1b	2:0	mod2_ios_fs	2	3	4(1)	5	6	7

(1) Default

MODx_SEQy_AOC_EN is the register that enables or disables AOC control. To run the calibration algorithm with the IOS DAC, in order to eliminate the input offset accompanied by the ambient light, this register must be set to logic high.

Figure 46:
MODx_SEQy_AOC_EN Settings

Register	Address	Bit	Bit Name	AOC disabled, MODx_SEQy_AOC Registers Used(1)
MOD1_SEQ1_AOC_EN	0x8b	7:0	mod1_seq1_aoc_en	0x00
MOD2_SEQ1_AOC_EN	0x8c	1:0	mod2_seq1_aoc_en	0x00

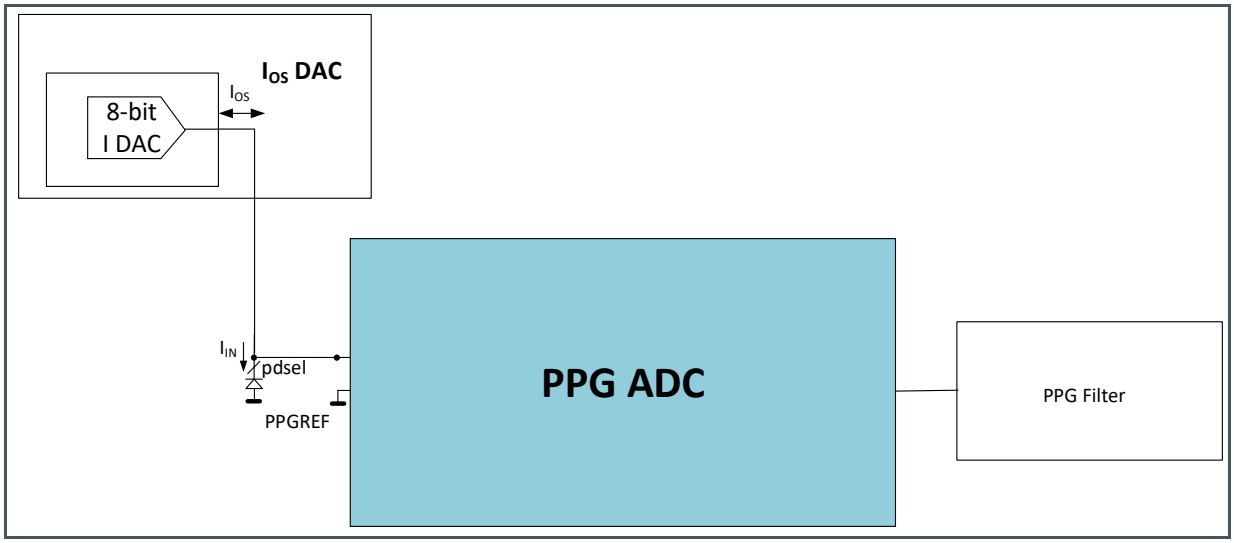
(1) Default

The digital input to the IOS DAC is provided by the registers AOC_MODx_SEQy_SUBz. These 20 8-bit registers enable us to write different digital inputs for the IOS DAC for different subsamples.

7.1.5 PPG ADCs

The PPG ADCs are current input ADCs. They are controlled by the sequencer for each time slot.

Figure 47:
PPG ADC



The ADC Input Full-Scale Range (ADC_FSR=1 µA...64 µA), from PDs to PPG-ADC, has been programmed by the reference DAC (DAC_FSR) full-scale range. A stable operation is enabled; by proper operation conditions using a DAC with bipolar references.

MODx_CFGB is used to scale the reference DAC current inside MODx. By default, it is set to 4, which allows the MODx to cover nearly 30% of the PD's output current range. Configuration registers MODx_CFGC and MODx_CFGD contain parameters that vary with the AGAIN. Each AGAIN, and the corresponding configuration registers, address a different input full-scale range as shown in the figure below. Configuration registers C&D vary AGAIN parameters for sequence1 and registers E&F vary

parameters for sequence2. The default values of these registers for each AGAIN setting are shown in Figure 48 below.

Figure 48:
MOD1 and MOD2 FSR Settings

			IFS	4 µA	8 µA	16 µA	32 µA	64 µA
Register	Address	MOD	AGAIN	2	3	4	5	6
MOD1_CFGC	0x1d	MOD1	SEQ1	0x27	0x27	0x2F	0x1F	0x1F
MOD1_CFGD	0x1e			0x03	0x07	0x0F	0x1F	0x3F
MOD1_CFGE	0x1f		SEQ2	0x27	0x27	0x2F	0x1F	0x1F
MOD1_CFGF	0x20			0x03	0x07	0x0F	0x1F	0x3F
MOD2_CFGC	0x23	MOD2	SEQ1	0x27	0x27	0x2F	0x1F	0x1F
MOD2_CFGD	0x24			0x03	0x07	0x0F	0x1F	0x3F
MOD2_CFGE	0x25		SEQ2	0x27	0x27	0x2F	0x1F	0x1F
MOD2_CFGF	0x26			0x03	0x07	0x0F	0x1F	0x3F

MOD_CFGA Register (Address 0x19)

Figure 49:
MOD_CFGA Register

Addr: 0x19		MOD_CFGA		
Bit	Bit Name	Default	Access	Bit Description
1:0	mod_opamp_ibias	0	RW	OPAMP bias current scaling; internal test of MOD power supply. Number: 0 – Value: x1 1 – Reserved 2 – Reserved 3 – Reserved

MOD_CFGB Register (Address 0x1a)

Figure 50:
MOD_CFGB Register

Addr: 0x1a		MOD_CFGB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:5	mod_dsm_mode	0	RW	Modulator operation mode **Number** **Function** 0 vint1-vcm 1 Reserved 2 Reserved 3 Reserved
4:3	mod_comp_mode	0	RW	PPG comparator operation mode
2:0	mod_ref_mode	0	RW	Reference DAC operation mode irefp/irefn

MOD1_CFGA Register (Address 0x1b)

Figure 51:
MOD1_CFGA Register

Addr: 0x1b		MOD1_CFGA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5	mod1_ios_mux	0	RW	Multiplex IOS DAC2 to modulator 1 for calibration **Number** **Function** 0 ios DAC to MOD1 1 ios DAC to MOD2, if mod1_ios_dir=1
4	mod1_en	0	RW	Enable Modulator1 **Number** **Function** 0 Off 1 On

Addr: 0x1b		MOD1_CFGA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	mod1_ios_dir	0	RW	Offset DAC current direction **Number**: **Function** 0: PMOS (Ambient Light Cancellation) PD Current - PD Offset Current 1: Reserved
2:0	mod1_ios_fs	4	RW	Offset DAC Full Scale Current **Number**: **Value** 0: 1 µA 1: 2 µA 2: 4 µA 3: 8 µA 4: 16 µA 5: 32 µA 6: 64 µA 7: 128 µA

MOD1_CFGB Register (Address 0x1c)

Figure 52:
MOD1_CFGB Register

Addr: 0x1c		MOD1_CFGB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	mod1_iref_scale	0	RW	Current reference DAC IRN/IRNmax scale factor **Number**: **Value** 0: Reserved 1: Reserved 2: Reserved 3: Reserved 4: 0.625

Addr: 0x1c		MOD1_CFGB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				5 Reserved
				6 Reserved
				7 1.000
				8-15 Reserved

MOD1_CFGC Register (Address 0x1d)

Figure 53:
MOD1_CFGC Register

Addr: 0x1d		MOD1_CFGC		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5	mod1_seq1_dsm_ampl	0	RW	DSM integrator amplitude scaling
4:0	mod1_seq1_cint	0	RW	Integrator Capacitance
				Number **Value**
				0 1 pF
				1 2 pF
				… …
				15 16 pF
				16…31 Reserved

MOD1_CFGD Register (Address 0x1e)

Figure 54:
MOD1_CFGD Register

Addr: 0x1e		MOD1_CFGD		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	mod1_seq1_iref	0	RW	Current reference P-DAC value
				Number **Value**
				0 1 µA
				1 2 µA

Addr: 0x1e		MOD1_CFGD		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				… …
				31 32 µA
				32…255 Reserved

MOD1_CFGE Register (Address 0x1f)

Figure 55:
MOD1_CFGE Register

Addr: 0x1f		MOD1_CFGE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5	mod1_seq2_dsm_ampl	0	RW	DSM integrator amplitude scaling
3:0	mod1_seq2_cint	0	RW	Integrator Capacitance
				Number **Value**
				0 1 pF
				1 2 pF
				… …
				15 16 pF
				16…31 Reserved

MOD1_CFGF Register (Address 0x20)

Figure 56:
MOD1_CFGF Register

Addr: 0x20		MOD1_CFGF		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	mod1_seq2_iref	0	RW	Current reference DAC value
				Number **Value**
				0 1 µA
				1 2 µA
				… …

Addr: 0x20		MOD1_CFGF			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
				31	32 µA
				32…255	Reserved

MOD2_CFGA Register (Address 0x21)

Figure 57:
MOD2_CFGA Register

Addr: 0x21		MOD2_CFGA			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
5	mod2_ios_mux	0	RW	Multiplex IOS DAC1 to Modulator2 for calibration	
				Number	**Function**
				0	ios DAC to MOD2
				1	ios DAC to MOD1 if mod1_ios_dir=1
4	mod2_en	0	RW	Enable Modulator2	
				Number	**Function**
				0	Off
				1	On
3	mod2_ios_dir	0	RW	Offset DAC current direction	
				Number	**Function**
				0	PMOS (Ambient Light Cancellation)
				1	NMOS (Special Mode) PD Current + PD Offset Current
2:0	mod2_ios_fs	4	RW	Offset DAC value	
				Number	**Value**
				0	1 µA
				1	2 µA

Addr: 0x21		MOD2_CFGA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				2 4 µA
				3 8 µA
				4 16 µA
				5 32 µA
				6 64 µA
				7 128 µA

MOD2_CFGB Register (Address 0x22)

Figure 58:
MOD2_CFGB Register

Addr: 0x22		MOD2_CFGB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	mod2_iref_scale	0	RW	Current reference DAC IRP/IRN scale factor **Number** **Value** 0 0.125 1 0.250 2 0.375 3 0.500 4 0.625 5 0.750 6 0.875 7 1.000 8-15 Reserved

MOD2_CFGC Register (Address 0x23)

Figure 59:
MOD2_CFGC Register

Addr: 0x23		MOD2_CFGC			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
5	mod2_seq1_dsm_ampl	0	RW	DSM integrator amplitude scaling	
4:0	mod2_seq1_cint	0	RW	Integrator Capacitance	
				Number	**Value**
				0	1 pF
				1	2 pF
				…	…
				15	16 pF
				16-31	Reserved

MOD2_CFGD Register (Address 0x24)

Figure 60:
MOD2_CFGD Register

Addr: 0x24		MOD2_CFGD			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:0	mod2_seq1_iref	0	RW	Current reference DAC value	
				Number	**Value**
				0	1 µA
				1	2 µA
				…	…
				31	32 µA
				32-255	Reserved

MOD2_CFGE Register (Address 0x25)

Figure 61:
MOD2_CFGE Register

Addr: 0x25		MOD2_CFGE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5	mod2_seq2_dsm_ampl	0	RW	DSM integrator amplitude scaling
4:0	mod2_seq2_cint	0	RW	Integrator Capacitance **Number** **Value** 0 1 pF 1 2 pF … … 15 16 pF 16-31 Reserved

MOD2_CFGF Register (Address 0x26)

Figure 62:
MOD2_CFGF Register

Addr: 0x26		MOD2_CFGF		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	mod2_seq2_iref	0	RW	Current reference DAC value **Number** **Value** 0 1 µA 1 2 µA … … 31 32 µA 32-255 Reserved

7.1.6 Reference Block

The Reference Bock provides voltage and current references for all the blocks inside the analog block and LED/VCSEL drivers. It consists of a low voltage bandgap reference, which provides a set of buffers for delivering reference voltages to the PPG channels and LED/VCSEL drivers, and a current reference circuit inside the reference block.

REF_CFGA Register (Address 0x15)

Figure 63:
REF_CFGA Register

Addr: 0x15		REF_CFGA			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	en_bg	0	RW	Enable Bandgap; The bandgap is the main Voltage reference used to generate all internal voltages and currents. It must be enabled for modulator measurement and disabled in stand-by mode.	
				Number	**Function**
				0	Disabled
				1	Enabled
6	sel_ln_iled	1	RW	Select a low-noise source for the LED reference current.	
				Number	**Function**
				0	Regular source selected
				1	Low noise source selected
5	en_vcm_ppg	0	RW	Enable the VCM PPG Buffer; Voltage reference for ADC is enabled before measurement and disabled in standby.	
				Number	**Function**
				0	Disabled
				1	Enabled
4	sel_strtup	0	RW	Select Bandgap Start-UP Circuit.	
				Number	**Function**
				0	New start-up circuit
				1	Old start-up circuit

Addr: 0x15		REF_CFGA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	en_vr_led	0	RW	Enable LED Buffer; Voltage reference for the LED driver. **Number** **Function** 0 Disabled 1 Enabled
2	en_bias	0	RW	Enable IREF_DAC and IOS_DAC; Current bias reference. **Number** **Function** 0 Disabled 1 Enabled
1	en_ptat	0	RW	Select the tail current of VCM buffers. **Number** **Function** 0 2 mA 1 Reserved
0	byp_ref_lp	0	RW	Bypass of low-pass filter of bandgap voltage for faster startup **Number** **Function** 0 Not bypassed 1 Bypassed

REF_CFGB Register (Address 0x16)

Figure 64:
REF_CFGB Register

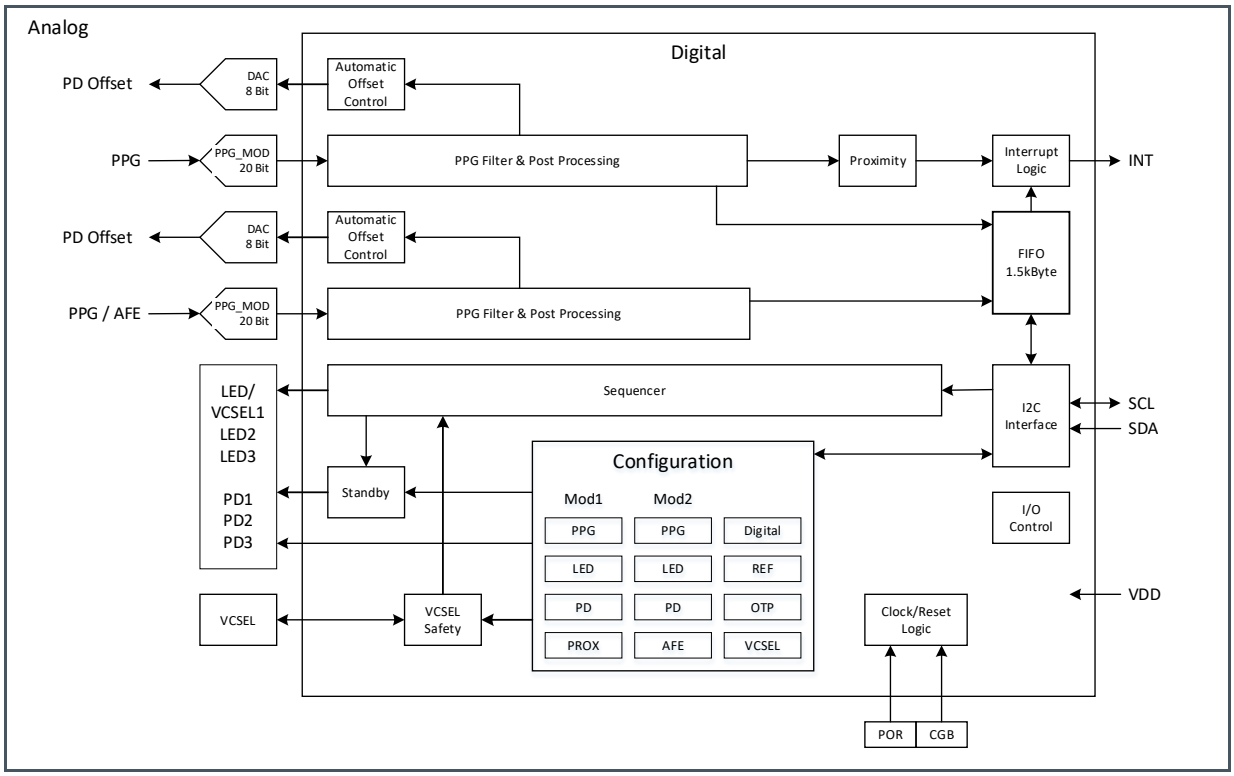
Addr: 0x16		REF_CFGB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	iled_tc	0	RW	Temperature coefficient of the LED current.

Addr: 0x16		REF_CFGB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	sel_iref_ln	1	RW	Select a low noise current reference for PPG IREF_DAC and IOS_DAC. **Number** / **Function** 0 / Regular source selected 1 / Low noise source selected
1	byp_progtc	1	RW	Bypass TC selection circuit for the LEC current. **Number** / **Function** 0 / Not bypassed 1 / Bypassed
0	sel_ref	0	RW	Select the reference voltage level for VCM; Voltage reference for ADC. All the signals are centered around this voltage. **Number** / **Function** 0 / 0.8 V 1 / 0.75 V

7.2 Digital Block

The main tasks of the digital part of the AS7056 are the AFE (Analog Frontend) configurations, host MCU communication, measurement control, signal filtering, and -balancing.

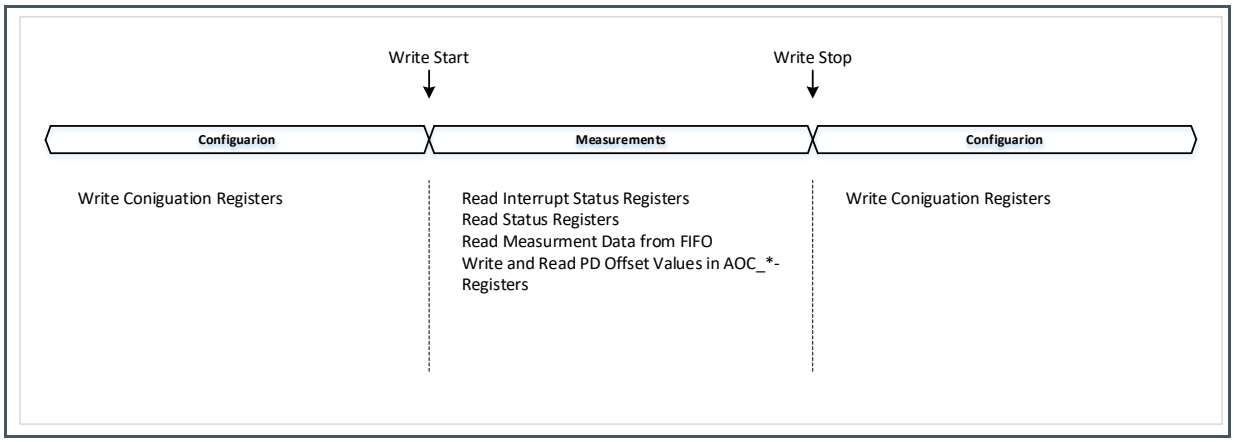
Figure 65:
Block Diagram of Digital Block



The digital block of the AS7056 includes the following main functional blocks:

- Sequencer
- PPG filters, Oversampling/Average, Post processing
- Proximity
- FIFO
- Interrupt logic
- Automatic offset control
- I^2C interface

Figure 66:
Measurement Procedure



A chip reset can be programmed via the I^2C at the system level; the SW RESET corresponds to the POR (Power-On-Reset).

7.2.1 Sequencer

A built-in sampling sequencer can be used to synchronize the LED currents, the integration time, and the ADC-sampling time. The sequencer generates the 8-bit-timings based on a 1 µs clock. The PPG acquisition channels run in parallel and operate with different sample frequencies. For this, the sampling frequency and the two frequency dividers for the partial sequences must be programmed.

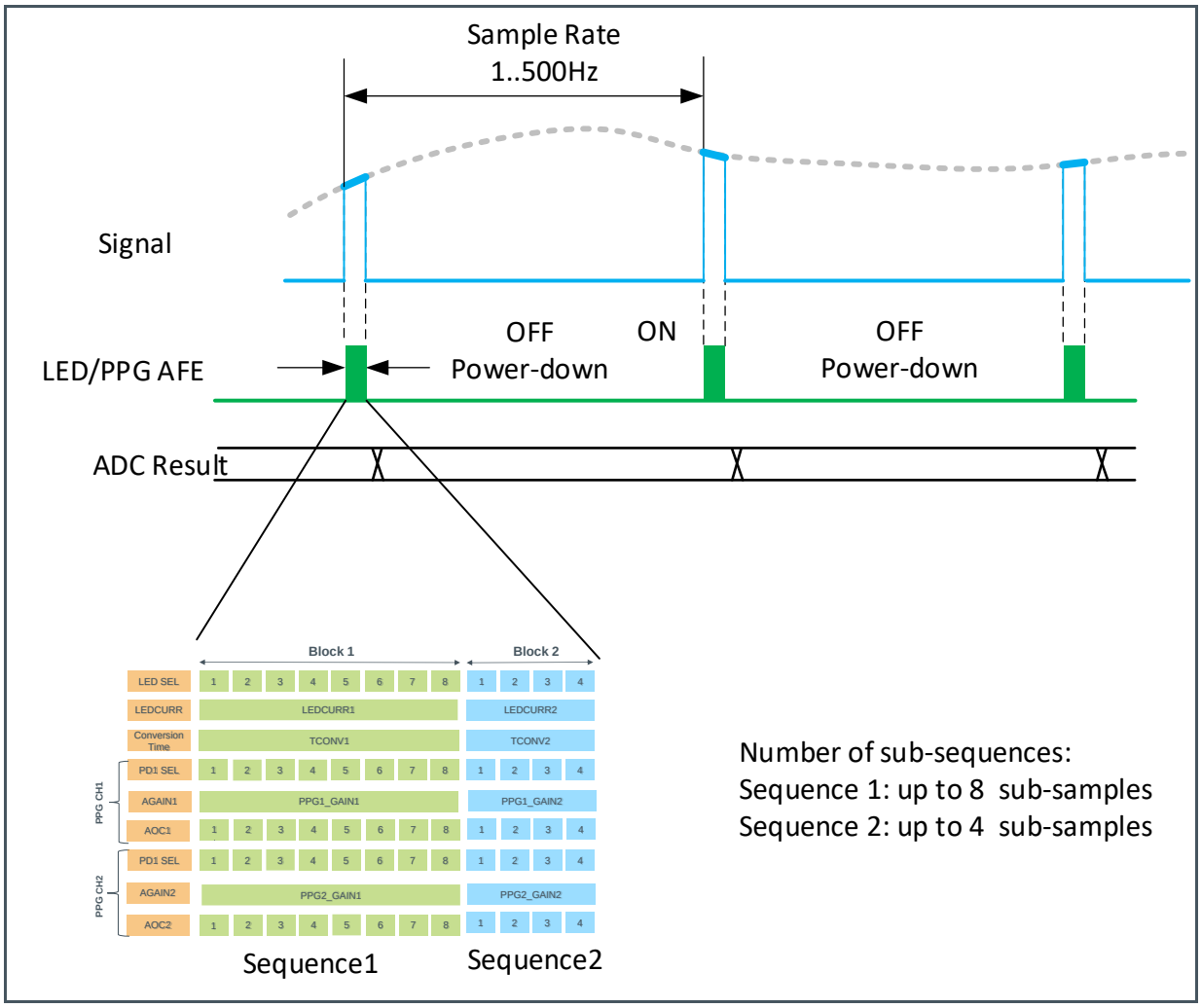
Attention

The standby mechanism is controlled by the programmable sample frequency.

The sampling rates of the PPG modulators are configurable between 1-500 Hz. Each sample channel can consist of up to twelve time-interleaved measurements with programmable configurations of the LEDs/VCSEL, photodiodes, and ambient light compensation.

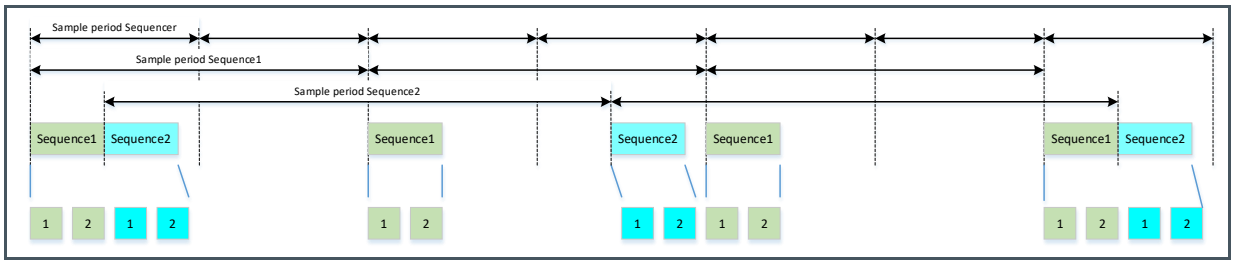
The flexible configuration, and timing control, enable users to find the optimal configuration to support heart rate monitoring, blood pressure measurement, pulse oximetry (SpO_2), and proximity detection.

Figure 67:
AS7056 Signal Acquisition



Each data sample is constructed from a set of individual measurements called sub-sequences. These sub-sequences are grouped in two sequences with separate sample rates, LED current, and PPG Gain control settings. The number of measurements can be configured from one to eight for Sequence1, and one to four for Sequence2. Each sub-sequence has its settings for operation mode, photodiode-, LED-, and AOC configurations.

Figure 68:
PPG Sample Frequencies Control



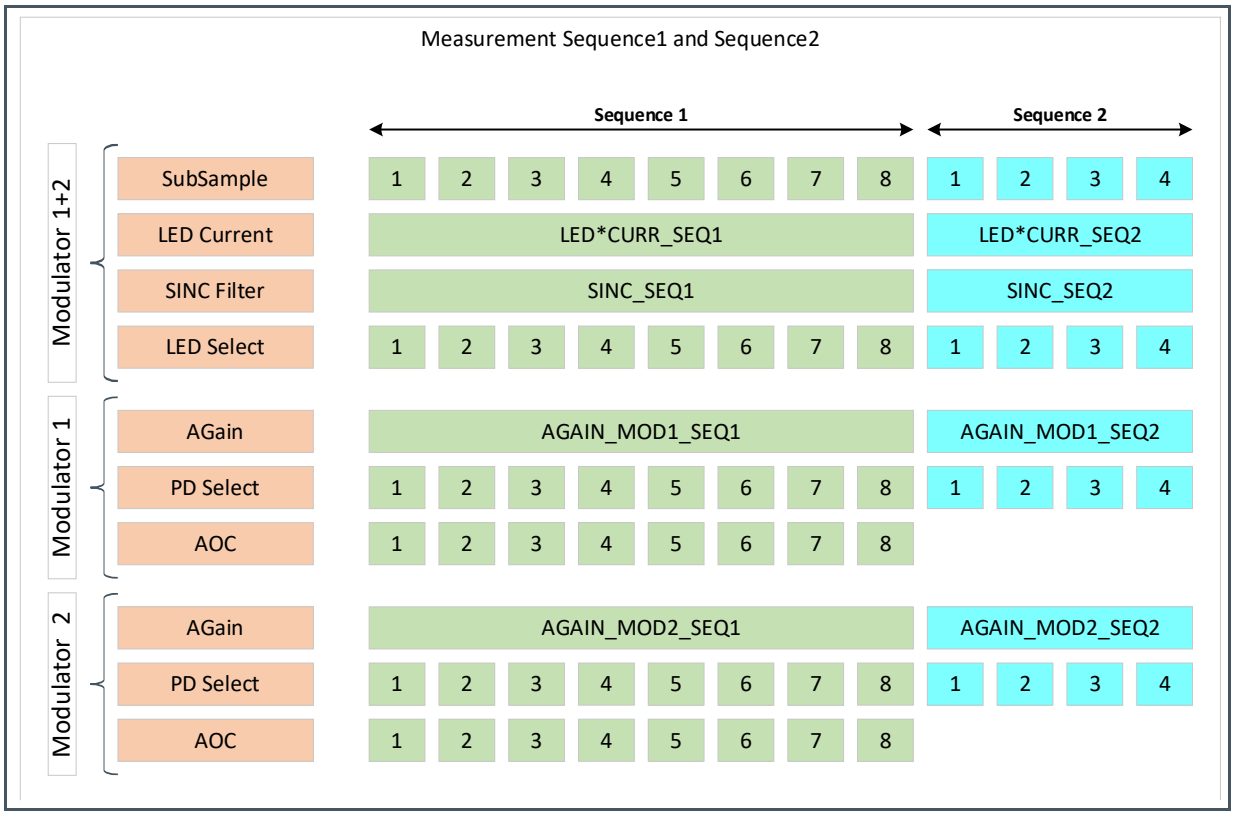
Configurations:

- A programmable sample period for the sequencer.
- A programmable sample period for sequence1 (PPG1, PPG2) by the divider.
- A programmable sample period for sequence2 (proximity, AFE) by the divider.
- The start of sampling is controlled by a clock of 32 kHz (standby).

Figure 69:
Sample Frequency Related Registers

Register Name	Description
SEQ_FREQH / SEQ_FREQL	Configuration Sequence Sample Period; (n+1) * 31.25 µs; n>0
SEQ1_FREQDIVH / SEQ1_FREQDIVL	Frequency divider for Sample Frequency Sequence1
SEQ2_FREQDIVH / SEQ2_FREQDIVL	Frequency divider for Sample Frequency Sequence2

Figure 70:
Maximum Sample Structure



Configurations:

- A programmable number of subsamples for sequencer1 = 1…8 (Conf=0…7)
- A programmable number of subsamples for sequencer2 = 1…4 (Conf=0…3)
- Enable signals for sequence1 and sequence2.

Figure 71:
Sampling Related Registers

Register Name	Description
SEQ_CONFIG	Configuration Sample Bit 7 – seq2_en; Enable Sequence2 5:4 – seq2_sub_sample, Number of Sub Samples n+1 3 – seq1_en; Enable Sequence1 2:0 – seq1_sub_sample, Number of Sub Samples n+1
MOD1_SEQ1_SUB_EN	Enable Sub Samples in Sequence1 for Modulator1.
MOD1_SEQ2_SUB_EN	Enable Sub Samples in Sequence2 for Modulator1.
MOD2_SEQ1_SUB_EN	Enable Sub Samples in Sequence1 for Modulator2.
MOD2_SEQ2_SUB_EN	Enable Sub Samples in Sequence2 for Modulator2.

Register Name	Description
PD_SEQ1_SUB1	Select PD for SubSample1 in Sequence1.
PD_SEQ1_SUB2	Select PD for SubSample2 in Sequence1.
PD_SEQ1_SUB3	Select PD for SubSample3 in Sequence1.
PD_SEQ1_SUB4	Select PD for SubSample4 in Sequence1.
PD_SEQ1_SUB5	Select PD for SubSample5 in Sequence1.
PD_SEQ1_SUB6	Select PD for SubSample6 in Sequence1.
PD_SEQ1_SUB7	Select PD for SubSample7 in Sequence1.
PD_SEQ1_SUB8	Select PD for SubSample8 in Sequence1.
PD_SEQ2_SUB1	Select PD for SubSample1 in Sequence2.
PD_SEQ2_SUB2	Select PD for SubSample2 in Sequence2.
PD_SEQ2_SUB3	Select PD for SubSample3 in Sequence2.
PD_SEQ2_SUB4	Select PD for SubSample4 in Sequence2.

Figure 72:
Example for Subsampling in Sequence1 and 2

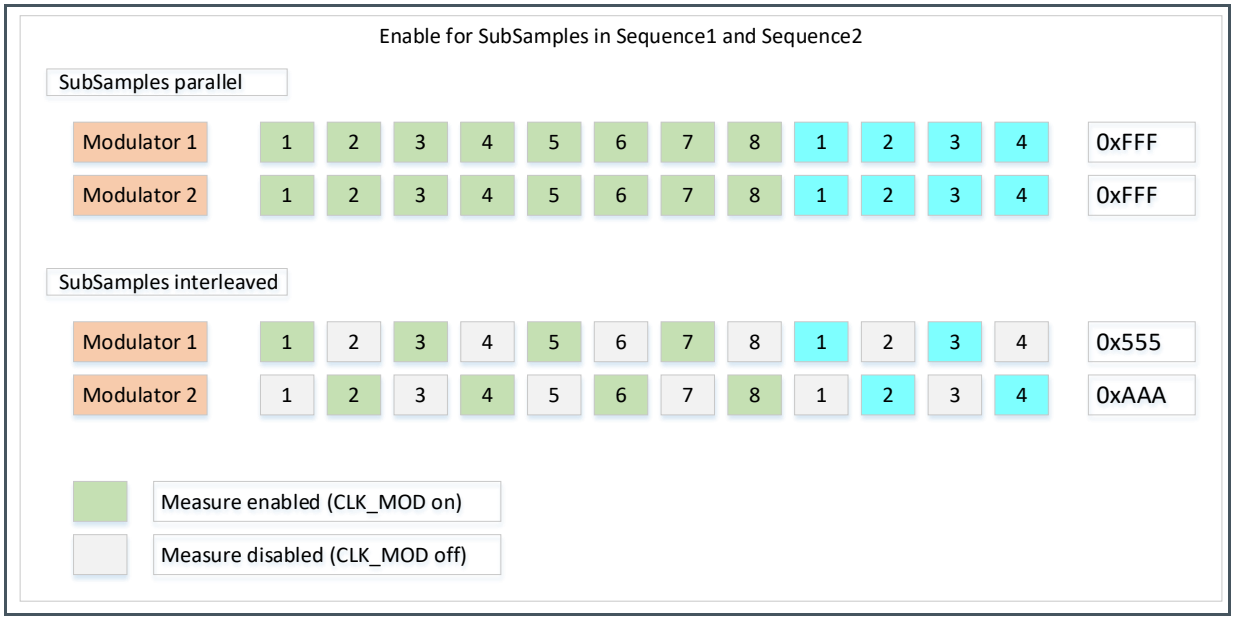
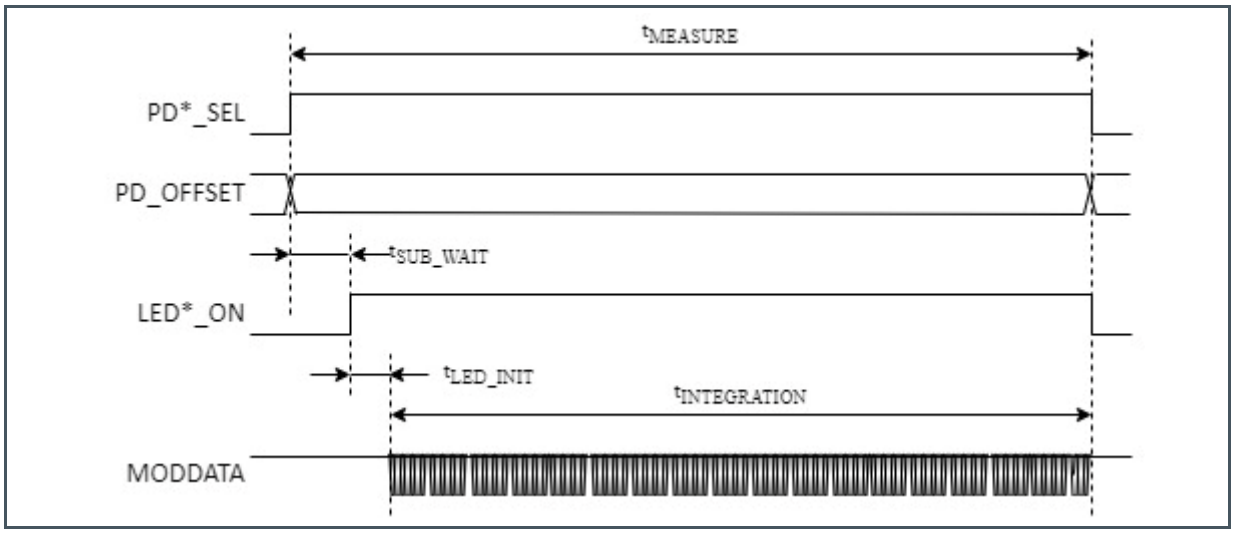


Figure 73:
Time Behavior of a Single Measurement



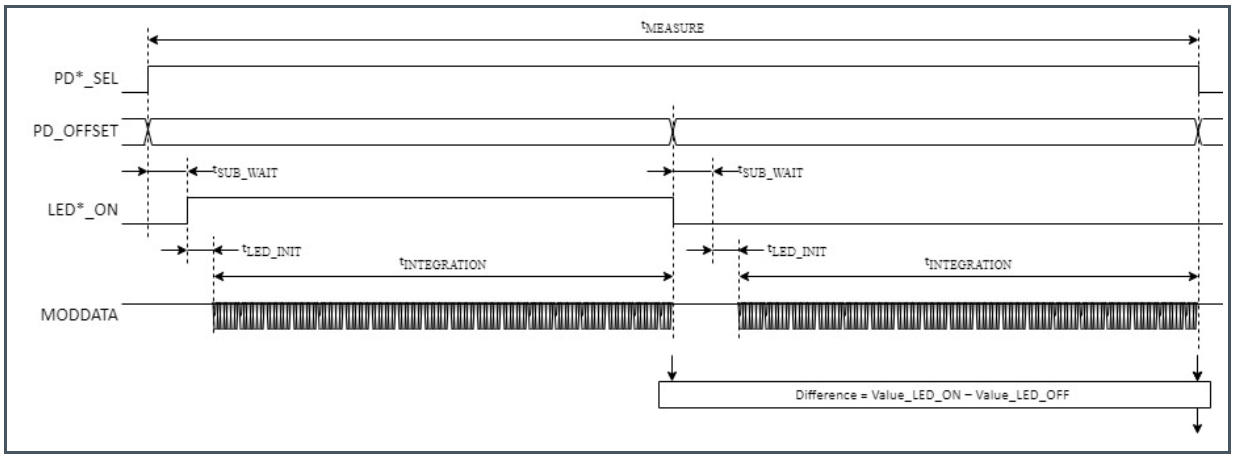
The single sampling function measures one value within a subsample.

The values for PD*_SEL, PD_OFFSET and LED*_ON must be programmed separately for each subsample.

Figure 74:
Single Measurement Timings

Time	Minimum Conditions		Maximum Conditions	
	modclk = 0	0.1 µs (10 MHz)	modclk = 3	0.8 µs (1.25 MHz)
	sinc_dec = 0		sinc_dec = 4	
t_{led_init}	led_init = 0	0 µs	led_init = 8'hff	255 µs
t_{reset_delay}	reset_delay = 0	0.4 µs	reset_delay = 3	25.6 µs
t_{start_delay}	start_delay = 0	0 µs	start_delay = 8'hff	240 µs
t_{sinc_dec}	sel_order = 0	8.5 µs	sel_order = 1	1252.8 µs
t_{os_delay}	os_delay = 0	0 µs	os_delay = 4'hf	3072 µs
t_{sinc_ovs}	sinc_ovs = 0	0 µs	sinc_ovs = 7	26009.6 µs
$t_{measure}$		8.9 µs		30.855 ms

Figure 75:
PPG Double Sampling



The double sampling function measures two values within a subsample.

The difference between the two measurements (Value_LED_ON – Value_LED_OFF) is written to the FIFO.

The programmed value for PD * _SEL is used for both measurements.

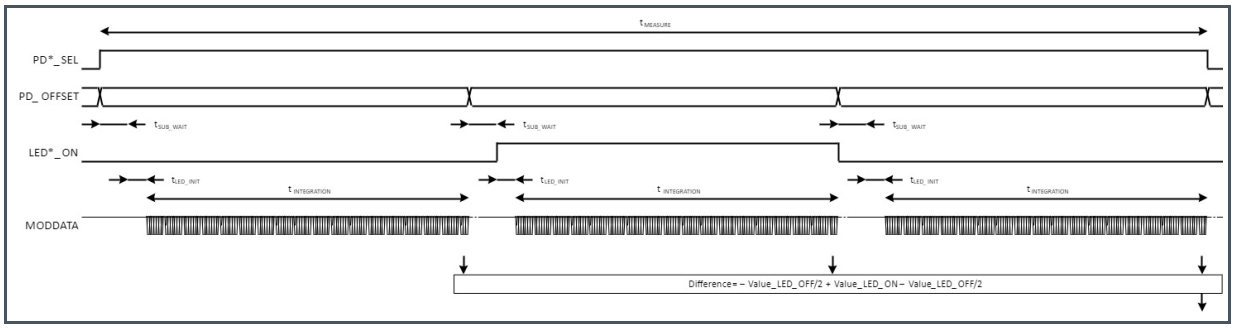
The programmed value for LED * _ON is used for the first measurement; it is switched off automatically for the second measurement.

The programmed value for the PD_OFFSET is used for the first measurement; the same value can be used for the second measurement (dis_ledoff = 1) or the programmed offset value for LED off (dis_ledoff = 0) is used.

Figure 76:
Double Measurement Timings

Time	Minimum Conditions		Maximum Conditions	
	modclk = 0	0.1 µs (10 MHz)	modclk = 3	0.8 µs (1.25 MHz)
	sinc_dec = 0		sinc_dec = 4	
$1*t_{led\_init}$	led_init = 0	0 µs	led_init = 8'hff	255 µs
$2*t_{reset\_delay}$	reset_delay = 0	0.4 µs	reset_delay = 3	25.6 µs
$2*t_{start\_delay}$	start_delay = 0	0 µs	start_delay = 8'hff	240 µs
$2*t_{sinc\_dec}$	sel_order = 0	8.5 µs	sel_order = 1	1252.8 µs
$2*t_{os\_delay}$	os_delay = 0	0 µs	os_delay = 4'hf	3072 µs
$2*t_{sinc\_ovs}$	sinc_ovs = 0	0 µs	sinc_ovs = 7	26009.6 µs
$t_{measure}$		18.7 µs		61.464 ms

Figure 77:
Time Slot for Triple Sampling



The Triple Sampling function measures three values within a subsample.

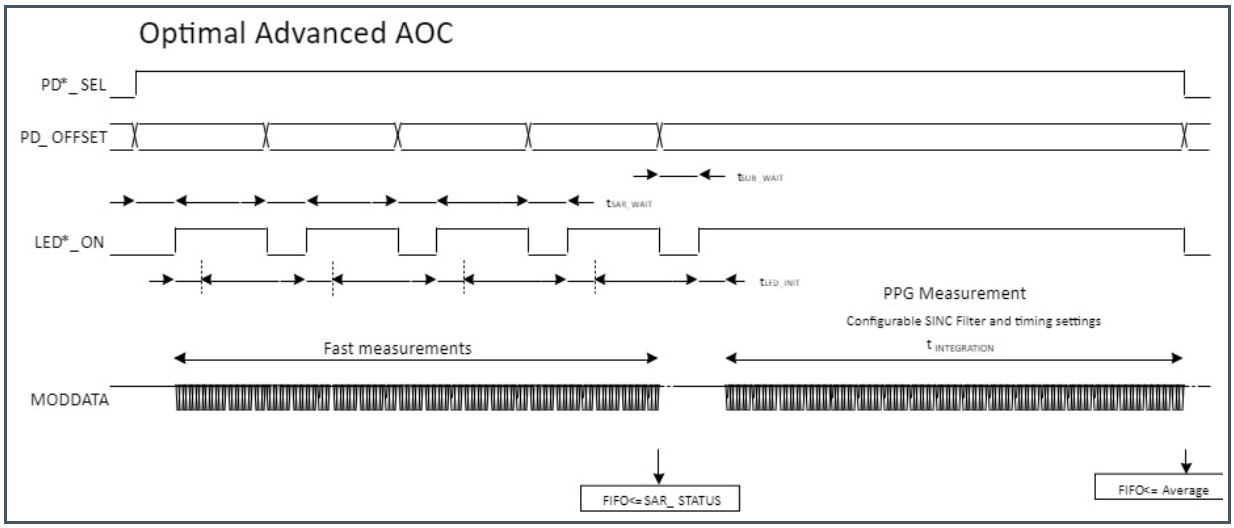
The difference between the three measurements (-Value_LED_OFF1*0.5 + Value_LED_ON - Value_LED_OFF2*0.5) is written to the FIFO.

The programmed value for PD * _SEL is used for all three measurements.

The programmed value for LED * _ON is used for the second measurement; it is switched off automatically for the first and third measurement.

The programmed value for the PD_OFFSET is used for the second measurement; the same value can be used for the first and third measurement (dis_ledoff = 1) or the programmed offset value for LED off (dis_ledoff = 0) is used.

Figure 78:
Time Behavior of an SAR Single Measurement



The SAR single sampling function measures the value within a subsampling after automatically calculating the upper 4 bits of the PD Offset. This feature targets an advanced automatic offset

control. It sets the AOC DAC immediately before the measurement. The FIFO stores the AOC data and the ADC results.

The programmed value for PD * _SEL is used for all five measurements.

The programmed value for LED * _ON is used for all five measurements.

The upper 4 bits for the PD_OFFSET are determined automatically with the first four measurements; the lower 4 bits correspond to the programmable bits. The determined PD offset is written to the FIFO as SAR status or to the lower bits of the ADC value.

PP_CFG Register (Address 0x37)

Figure 79:
PP_CFG Register

Addr: 0x37		PP_CFG			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7	asat_on	0	RW	Enable Analog Saturation; enabling the change in the measured signed value when an analog saturation is detected.	
				Number	**Function**
				0	The measured signed value has not changed.
				1	The measured signed value has changed.
3:0	asat_fil	0	RW	Digital Filter for the analog input signal for saturation; the pulse for the detection of the analog saturation must be longer than n * MOD_CLK.	

SEQ1_SUB12_PP Register (Address 0x38)

Figure 80:
SEQ1_SUB12_PP Register

Addr: 0x38		SEQ1_SUB12_PP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	mod1_seq1_sub1_pp	0	RW	Post Processing in Channel1 for SubSample1 in Sequence1. **Number** / **Value** 0 – Normal value 1 – Inverted value 2 – Value – pp_offset 3 – Write value to pp_offset
5:4	mod2_seq1_sub1_pp	0	RW	Post Processing in Channel2 for SubSample1 in Sequence1. (See the settings above at mod1_seq1_sub1_pp.)
3:2	mod1_seq1_sub2_pp	0	RW	Post Processing in Channel1 for SubSample2 in Sequence1. (See the settings above at mod1_seq1_sub1_pp.)
1:0	mod2_seq1_sub2_pp	0	RW	Post Processing in Channel2 for SubSample2 in Sequence1 (See the settings above at mod1_seq1_sub1_pp.)

SEQ1_SUB34_PP Register (Address 0x39)

Figure 81:
SEQ1_SUB34_PP Register

Addr: 0x39		SEQ1_SUB34_PP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	mod1_seq1_sub3_pp	0	RW	Post Processing in Channel1 for SubSample3 in Sequence1.

Addr: 0x39		SEQ1_SUB34_PP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				Number / **Value** 0 – Normal value 1 – Inverted value 2 – Value – pp_offset 3 – Write value to pp_offset
5:4	mod2_seq1_sub3_pp	0	RW	Post Processing in Channel2 for SubSample3 in Sequence1. (See the settings above at mod1_seq1_sub3_pp.)
3:2	mod1_seq1_sub4_pp	0	RW	Post Processing in Channel1 for SubSample4 in Sequence1. (See the settings above at mod1_seq1_sub3_pp.)
1:0	mod2_seq1_sub4_pp	0	RW	Post Processing in Channel2 for SubSample4 in Sequence1. (See the settings above at mod1_seq1_sub3_pp.)

SEQ1_SUB56_PP Register (Address 0x3a)

Figure 82:
SEQ1_SUB56_PP Register

Addr: 0x3a		SEQ1_SUB56_PP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	mod1_seq1_sub5_pp	0	RW	Post Processing in Channel1 for SubSample5 in Sequence1. **Number** / **Value** 0 – Normal value 1 – Inverted value 2 – Value – pp_offset

Addr: 0x3a		SEQ1_SUB56_PP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				3 Write value to pp_offset
5:4	mod2_seq1_sub5_pp	0	RW	Post Processing in Channel2 for SubSample5 in Sequence1. (See the settings above at mod1_seq1_sub5_pp.)
3:2	mod1_seq1_sub6_pp	0	RW	Post Processing in Channel1 for SubSample6 in Sequence1. (See the settings above at mod1_seq1_sub5_pp.)
1:0	mod2_seq1_sub6_pp	0	RW	Post Processing in Channel2 for SubSample6 in Sequence1. (See the settings above at mod1_seq1_sub5_pp.)

SEQ1_SUB78_PP Register (Address 0x3b)

Figure 83:
SEQ1_SUB78_PP Register

Addr: 0x3b		SEQ1_SUB78_PP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	mod1_seq1_sub7_pp	0	RW	Post Processing in Channel1 for SubSample7 in Sequence1. **Number** / **Value** 0 Normal value 1 Inverted value 2 Value – pp_offset 3 Write value to pp_offset
5:4	mod2_seq1_sub7_pp	0	RW	Post Processing in Channel2 for SubSample7 in Sequence1. (See the settings above at mod1_seq1_sub7_pp.)

Addr: 0x3b		SEQ1_SUB78_PP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:2	mod1_seq1_sub8_pp	0	RW	Post Processing in Channel1 for SubSample8 in Sequence1. (See the settings above at mod1_seq1_sub7_pp.)
1:0	mod2_seq1_sub8_pp	0	RW	Post Processing in Channel2 for SubSample8 in Sequence1. (See the settings above at mod1_seq1_sub7_pp.)

SEQ2_SUB12_PP Register (Address 0x3c)

Figure 84:
SEQ2_SUB12_PP Register

Addr: 0x3c		SEQ2_SUB12_PP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	mod1_seq2_sub1_pp	0	RW	Post Processing in Channel1 for SubSample1 in Sequence2. **Number** / **Value** 0 – Normal value 1 – Inverted value 2 – Value – pp_offset 3 – Write value to pp_offset
5:4	mod2_seq2_sub1_pp	0	RW	Post Processing in Channel2 for SubSample1 in Sequence2. (See the settings above at mod1_seq2_sub1_pp.)
3:2	mod1_seq2_sub2_pp	0	RW	Post Processing in Channel1 for SubSample2 in Sequence2. (See the settings above at mod1_seq2_sub1_pp.)

Addr: 0x3c		SEQ2_SUB12_PP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1:0	mod2_seq2_sub2_pp	0	RW	Post Processing in Channel2 for SubSample2 in Sequence2. (See the settings above at mod1_seq2_sub1_pp.)

SEQ2_SUB34_PP Register (Address 0x3d)

Figure 85:
SEQ2_SUB34_PP Register

Addr: 0x3d		SEQ2_SUB34_PP		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	mod1_seq2_sub3_pp	0	RW	Post Processing in Channel1 for SubSample3 in Sequence2. **Number** / **Value** 0 / Normal value 1 / Inverted value 2 / Value – pp_offset 3 / Write value to pp_offset
5:4	mod2_seq2_sub3_pp	0	RW	Post Processing in Channel2 for SubSample3 in Sequence2. (See the settings above at mod1_seq1_sub1_pp.)
3:2	mod1_seq2_sub4_pp	0	RW	Post Processing in Channel1 for SubSample4 in Sequence2. (See the settings above at mod1_seq2_sub3_pp.)
1:0	mod2_seq2_sub4_pp	0	RW	Post Processing in Channel2 for SubSample4 in Sequence2. (See the settings above at mod1_seq2_sub3_pp.)

SEQ_SAMPLE Register (Address 0x40)

Figure 86:
SEQ_SAMPLE Register

Addr: 0x40		SEQ_SAMPLE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_sample	0	RW	Number of samples for the activated channel; if seq_sample = 0 the sequencer runs continuously.

SEQ_SUB_WAIT Register (Address 0x41)

Figure 87:
SEQ_SUB_WAIT Register

Addr: 0x41		SEQ_SUB_WAIT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	sub_wait	0	RW	Distance between the SubSamples; N * 1 µs; Sequence1 and Sequence2 use the same distance.

SEQ_MODCONF Register (Address 0x42)

Figure 88:
SEQ_MODCONF Register

Addr: 0x42		SEQ_MODCONF		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4:2	mod_reset_delay	0	RW	Reset Time for all Modulators N * MOD_CLK; internal timing for the reset process.

Number	Value
0	4
1	8
2	16
3	32

Addr: 0x42		SEQ_MODCONF		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				4 64
				5 128
				>5 256
1:0	modclk	0	RW	Modulator clock frequency MOD_CLK; Sequence1 and Sequence2 use the same Modulator frequency **Number Value** 0 10 MHz 1 5 MHz 2 2.5 MHz 3 1.25 MHz

With a reduction of the Modulator clock frequency, the converting time will increase, and the signal-to-noise ratio will improve. Also, the power consumption of the AS7056 will increase.

SEQ_CONFIG Register (Address 0x43)

Figure 89:
SEQ_CONFIG Register

Addr: 0x43		SEQ_CONFIG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	seq2_en	0	RW	Enable Sequence2
5:4	seq2_sub_sample	0	RW	Number of SubSamples for Sequence2 (n+1) 0...3 - 1...4
3	seq1_en	0	RW	Enable Sequence1
2:0	seq1_sub_sample	0	RW	Number of SubSamples for Sequence1 (n+1) 0...7 - 1...8

SEQ_SAR_WAIT Register (Address 0x44)

Figure 90:
SEQ_SAR_WAIT Register

Addr: 0x44		SEQ_SAR_WAIT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	sar_wait	0	RW	Distance between the SAR measures; N * 1 µs

SEQ_LED_INIT Register (Address 0x45)

Figure 91:
SEQ_LED_INIT Register

Addr: 0x45		SEQ_LED_INIT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	led_init	0	RW	Setup time after turn on the LEDs; t_LED_INIT = N * 1 µs with N = 0 ... 255

SEQ_FREQL Register (Address 0x46)

Figure 92:
SEQ_FREQL Register

Addr: 0x46		SEQ_FREQL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_freq[7:0]	79	RW	Configuration of the Sequence Sample period T(SEQ) = (n+1) * 31.25 µs f(SEQ) = 1/((n+1) * 31.25 µs); n>0

SEQ_FREQH Register (Address 0x47)

Figure 93:
SEQ_FREQH Register

Addr: 0x47		SEQ_FREQH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq_freq[15:8]	0	RW	Configuration of the Sequence Sample period T(SEQ) = (n+1) * 31.25 µs f(SEQ) = 1/((n+1) * 31.25 µs); n>0

SEQ1_FREQDIVL Register (Address 0x48)

Figure 94:
SEQ1_FREQDIVL Register

Addr: 0x48		SEQ1_FREQDIVL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq1_freqdiv[7:0]	0	RW	Sample period Sequence1 T(SEQ1) = (n+1) * T(SEQ) f(SEQ1) = f(SEQ)/(n+1)

SEQ1_FREQDIVH Register (Address 0x49)

Figure 95:
SEQ1_FREQDIVH Register

Addr: 0x49		SEQ1_FREQDIVH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq1_freqdiv[15:8]	0	RW	Sample period Sequence1 T(SEQ1) = (n+1) * T(SEQ) f(SEQ1) = f(SEQ)/(n+1)

SEQ2_FREQDIVL Register (Address 0x4a)

Figure 96:
SEQ2_FREQDIVL Register

Addr: 0x4a		SEQ2_FREQDIVL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq2_freqdiv[7:0]	0	RW	Sample period Sequence2 T(SEQ2) = (n+1) * T(SEQ) f(SEQ2) = f(SEQ)/(n+1)

SEQ2_FREQDIVH Register (Address 0x4b)

Figure 97:
SEQ2_FREQDIVH Register

Addr: 0x4b		SEQ2_FREQDIVH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq2_freqdiv[15:8]	0	RW	Sample period Sequence2 T(SEQ2) = (n+1) * T(SEQ) f(SEQ2) = f(SEQ)/(n+1)

MOD1_SEQ1_SUB_EN Register (Address 0x4c)

Figure 98:
MOD1_SEQ1_SUB_EN Register

Addr: 0x4c		MOD1_SEQ1_SUB_EN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	mod1_seq1_sub_en	0	RW	Enable SubSamples Sequence1 in Channel1; see Figure 72.

MOD1_SEQ2_SUB_EN Register (Address 0x4d)

Figure 99:
MOD1_SEQ2_SUB_EN Register

Addr: 0x4d		MOD1_SEQ2_SUB_EN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	mod1_seq2_sub_en	0	RW	Enable SubSamples Sequence2 in Channel1.

MOD2_SEQ1_SUB_EN Register (Address 0x4e)

Figure 100:
MOD1_SEQ1_SUB_EN Register

Addr: 0x4e		MOD2_SEQ1_SUB_EN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Mod2_seq1_sub_en	0	RW	Enable SubSamples Sequence1 in Channel2.

MOD2_SEQ2_SUB_EN Register (Address 0x4f)

Figure 101:
MOD1_SEQ2_SUB_EN Register

Addr: 0x4f		MOD2_SEQ2_SUB_EN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	Mod2_seq2_sub_en	0	RW	Enable SubSamples Sequence2 in Channel2.

SEQ1_MODE_A Register (Address 0x50)

Figure 102:
SEQ1_MODE_A Register

Addr: 0x50		SEQ1_MODE_A		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	seq1_sub1_mode	0	RW	Measure the mode for SubSample1 in Sequence1. **Number** **Value** 0 Single 1 Double 2 Triple 3 SAR Single
5:4	seq1_sub2_mode	0	RW	Measure the mode for SubSample2 in Sequence1; the same settings as in seq1_sub1_mode.
3:2	seq1_sub3_mode	0	RW	Measure the mode for SubSample3 in Sequence1; the same settings as in seq1_sub1_mode.
1:0	seq1_sub4_mode	0	RW	Measure the mode for SubSample4 in Sequence1; the same settings as in seq1_sub1_mode.

SEQ1_MODE_b Register (Address 0x51)

Figure 103:
SEQ1_MODE_B Register

Addr: 0x51		SEQ1_MODE_B		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	seq1_sub5_mode	0	RW	Measure the mode for SubSample5 in Sequence1. **Number** **Value** 0 Single 1 Double 2 Triple 3 SAR Single

Addr: 0x51		SEQ1_MODE_B		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5:4	seq1_sub6_mode	0	RW	Measure the mode for SubSample6 in Sequence1; the same settings as in seq1_sub5_mode.
3:2	seq1_sub7_mode	0	RW	Measure the mode for SubSample7 in Sequence1; the same settings as in seq1_sub5_mode.
1:0	seq1_sub8_mode	0	RW	Measure the mode for SubSample8 in Sequence1; the same settings as in seq1_sub5_mode.

SEQ2_MODE Register (Address 0x52)

Figure 104:
SEQ2_MODE Register

Addr: 0x52		SEQ2_MODE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	seq2_sub1_mode	0	RW	Measure the mode for SubSample1 in Sequence2. **Number** / **Value** 0 / Single 1 / Double 2 / Triple 3 / SAR Single
5:4	seq2_sub2_mode	0	RW	Measure the mode for SubSample2 in Sequence2; the same settings as in seq2_sub1_mode.
3:2	seq2_sub3_mode	0	RW	Measure the mode for SubSample3 in Sequence2; the same settings as in seq2_sub1_mode.
1:0	seq2_sub4_mode	0	RW	Measure the mode for SubSample4 in Sequence2; the same settings as in seq2_sub1_mode.

7.2.2 Digital Filter, Averaging and Post Processing

The Digital Filter includes a CIC filter and is configurable for fast and slow measurements. The filter can also only run in an integrator mode, and it uses two's complement for math operations. Oversampling is not available in integrator mode.

Figure 105:
Digital Filter Structure

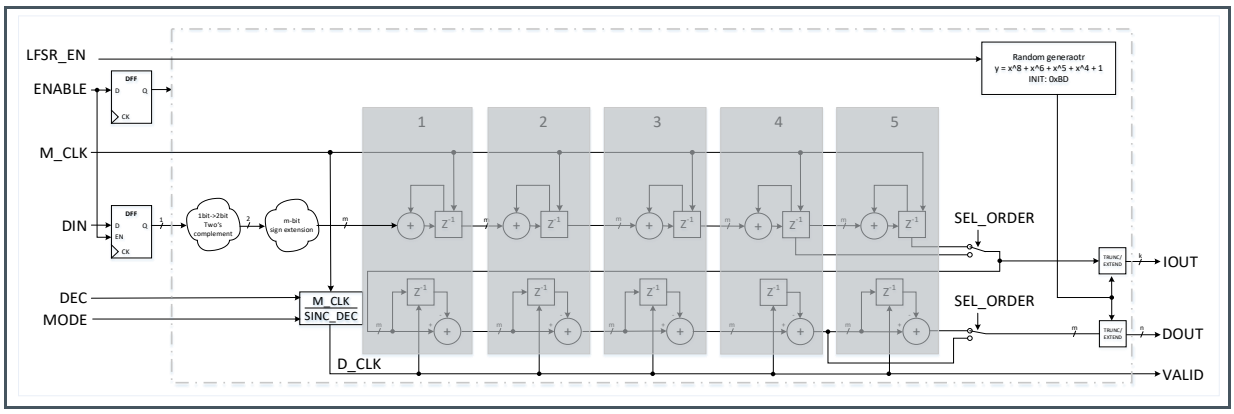
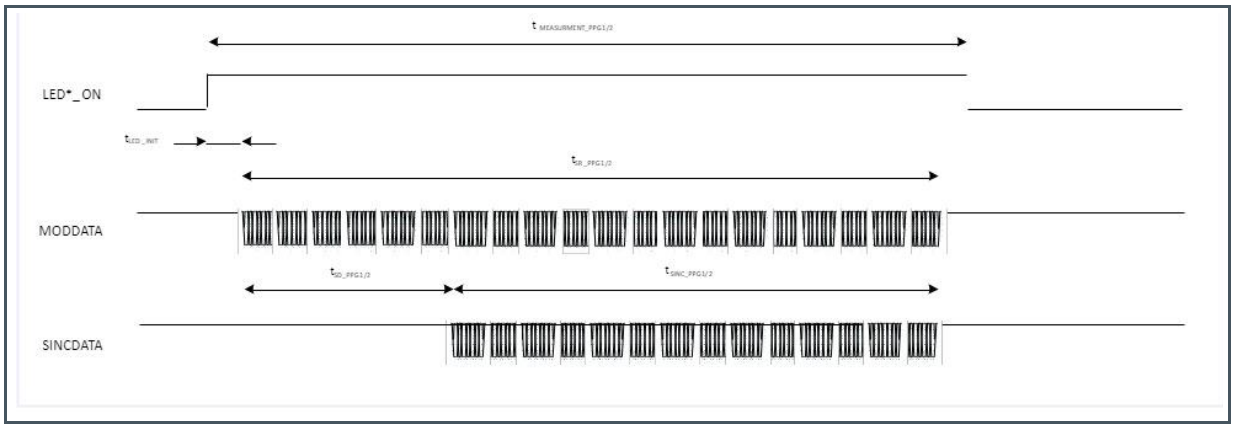


Figure 106:
Digital Filter Timing Diagram of Data Propagation (CIC mode)



CIC Mode:

$t_{SD\_PPG1/PPG2} = SEQ1/SEQ2\_START\_DELAY * T_{PPG1/PPG2\_MODCLK}$

$t_{DV\_PPG1/PPG2} = SEQ1/SEQ2\_ORDER * SEQ1/SEQ2\_SINC\_DEC * T_{PPG1/PPG2\_MODCLK}$

$t_{OS\_PPG1/PPG2} = SEQ1/SEQ2\_OS\_DELAY * SEQ1/SEQ2\_SINC\_DEC * T_{PPG1/PPG2\_MODCLK}$

$t_{OVER\_PPG1/PPG2} = 2(SEQ1/SEQ2\_SINC\_OVS - 1) * SEQ1/SEQ2\_SINC\_DEC * T_{PPG1/PPG2\_MODCLK}$

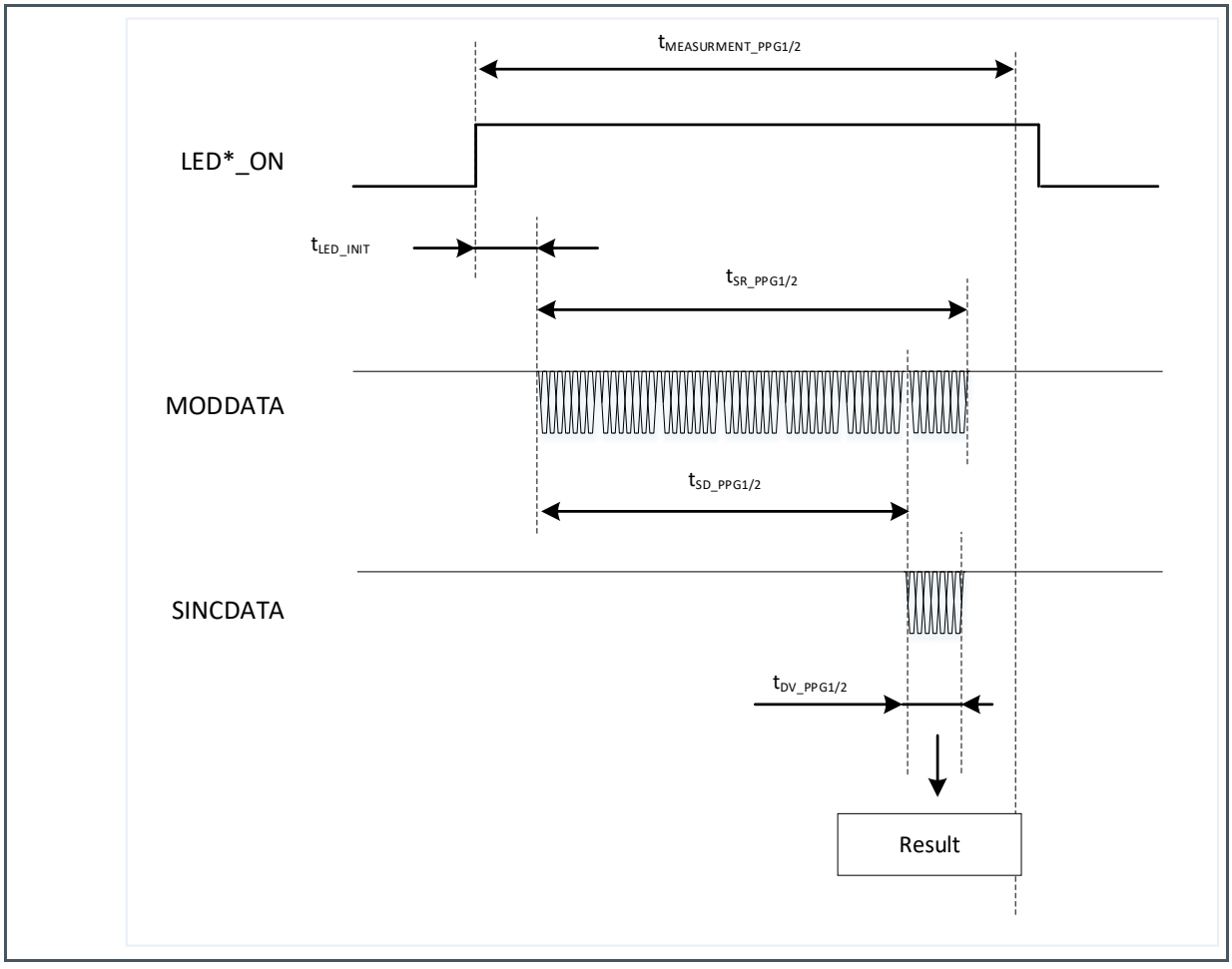
$$t_{SR\_PPG1/PPG2} = t_{SD\_PPG1/PPG2} + t_{DV\_PPG1/PPG2} + t_{OS\_PPG1/PPG2} + t_{OVER\_PPG1/PPG2}$$

$$t_{MEASURMENT\_PPG1/PPG2} = t_{LED\_INIT} + t_{SR\_PPG1/PPG2}$$

Figure 107:
CIC Mode Integration Times in µs, f_mod = 10 MHz

	Oversampling Order 4					Oversampling Order 5				
Decimation Rate	**0**	**2**	**4**	**8**	**16**	**0**	**2**	**4**	**8**	**16**
16	6.7	9.9	13.1	19.5	32.3	8.3	11.5	14.7	21.1	33.9
32	13.1	19.5	25.9	38.7	64.3	16.3	22.7	29.1	41.9	67.5
64	25.9	38.7	51.5	77.1	128.3	32.3	45.1	57.9	83.5	134.7
128	51.5	77.1	102.7	153.9	256.3	64.3	89.9	115.5	166.7	269.1
256	102.7	153.9	205.1	307.5	512.3	128.3	179.5	230.7	333.1	537.9

Figure 108:
Digital Filter Timing Diagram of Data Propagation (Integrator mode)



Integrator Mode:

$t_{SD\_PPG1/2} = SEQ1/2\_START\_DELAY * T_{PPG1/2\_MODCLK}$

$t_{DV\_PPG1/2} = SEQ1/2\_SINC\_DEC * T_{PPG1/2\_MODCLK}$

$t_{SR\_PPG1/2} = t_{SD\_PPG1/2} + t_{DV\_PPG1/2}$

$t_{MEASURMENT\_PPG1/2} = t_{LED\_INIT} + t_{SR\_PPG1/2}$

Figure 109:
Integrator Mode Integration Times in µs, f_mod = 10 MHz

	Oversampling Order 4					Oversampling Order 5				
Decimation Rate	0	2	4	8	16	0	2	4	8	16
16	2.3	N/A	N/A	N/A	N/A	2.4	N/A	N/A	N/A	N/A
32	3.9	N/A	N/A	N/A	N/A	4	N/A	N/A	N/A	N/A
64	7.1	N/A	N/A	N/A	N/A	7.2	N/A	N/A	N/A	N/A
128	13.5	N/A	N/A	N/A	N/A	13.6	N/A	N/A	N/A	N/A
256	26.3	N/A	N/A	N/A	N/A	26.4	N/A	N/A	N/A	N/A

SEQ1_SINC_CFGA Register (Address 0x61)

Figure 110:
SEQ1_SINC_CFGA Register

Addr: 0x61		SEQ1_SINC_CFGA		
Bit	Bit Name	Default	Access	Bit Description
7:5	seq1_sinc_ovs	0	RW	Value for oversampling SINC filter. Oversampling = 2^seq1_sinc_ovs
4:2	seq1_sinc_dec	0	RW	Number: Decimation 0: 16 1: 32 2: 64 3: 128 4: 256

SEQ1_SINC_CFGB Register (Address 0x62)

Figure 111:
SEQ1_SINC_CFGB Register

Addr: 0x62		SEQ1_SINC_CFGB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:3	seq1_os_delay	0	RW	Delay after which data is valid for the average calculation.
1	seq1_sel_order	0	RW	Select filter order 4/5 **Number** / **Filter Order** 0 / 4 1 / 5
0	seq1_filter_mode	1	RW	Select a mode of filter for Sequence1. **Number** / **Mode** 0 / Integrator mode 1 / CIC mode

SEQ1_SINC_CFGC Register (Address 0x63)

Figure 112:
SEQ1_SINC_CFGC Register

Addr: 0x63		SEQ1_SINC_CFGC		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq1_start_delay	0	RW	Start delay

SEQ2_SINC_CFGA Register (Address 0x64)

Figure 113:
SEQ2_SINC_CFGA Register

Addr: 0x64		SEQ2_SINC_CFGA		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	seq2_sinc_ovs	0	RW	Value for oversampling SINC filter. Oversampling = 2^seq2_sinc_ovs
4:2	seq2_sinc_dec	0	RW	**Number** / **Decimation** 0 / 16 1 / 32 2 / 64 3 / 128 4 / 256

SEQ2_SINC_CFGB Register (Address 0x65)

Figure 114:
SEQ2_SINC_CFGB Register

Addr: 0x65		SEQ2_SINC_CFGB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:3	seq2_os_delay	0	RW	Delay after which data is valid for the average calculation.
1	seq2_sel_order	0	RW	Select filter order 4/5 **Number** / **Filter Order** 0 / 4 1 / 5
0	seq2_filter_mode	1	RW	Select a mode of filter for Sequence2. **Number** / **Mode** 0 / Integrator mode 1 / CIC mode

SEQ2_SINC_CFGC Register (Address 0x66)

Figure 115:
SEQ2_SINC_CFGC Register

Addr: 0x66		SEQ2_SINC_CFGC		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	seq2_start_delay	0	RW	

Post Processing

The post-processing includes; the calculation of the measurement values, change of PPG data at an active analog saturation, and inversion of the measured values. The inversion is programmable independently of each other for each subsample as described in the sequencer register descriptions.

7.2.3 Automatic Offset Control (AOC)

The AS7056 offers an automatic offset control to balance and reduce ambient light currents automatically. Apart from the configuration before or after a measurement cycle, it is also possible to adjust the AOC registers during a measurement by an external microcontroller.

The AOC is only available in sequence1 and can be activated for subsamples 1 to 8 for PPG MOD1 and subsamples1 to 2 in sequence1 for PPG MOD2 (see Figure 116).

Subsamples 1 to 4 in Sequence2 for PPG MOD1 and subsamples 3 to 8 in Sequence1 for PPG MOD2 only work with the manual programmable PD offset value.

Subsamples 1 to 4 in sequence 2 for PPG MOD2 are intended for the Analog Frontend and do not have a programmable PD offset value.

The PD offset registers can be overwritten if the AOC is active and take effect immediately. There are no shadow registers. The control of the AOC continues as usual.

Figure 116:
AOC Example for Subsampling in Sequence1

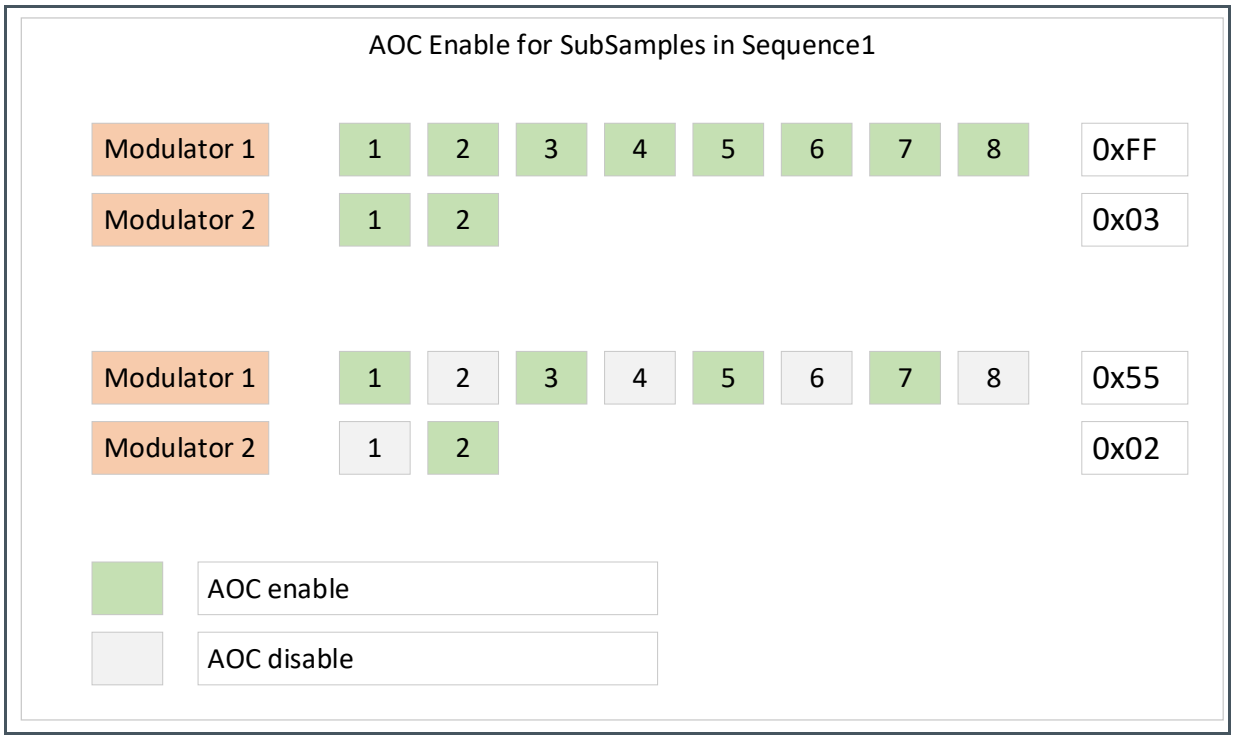
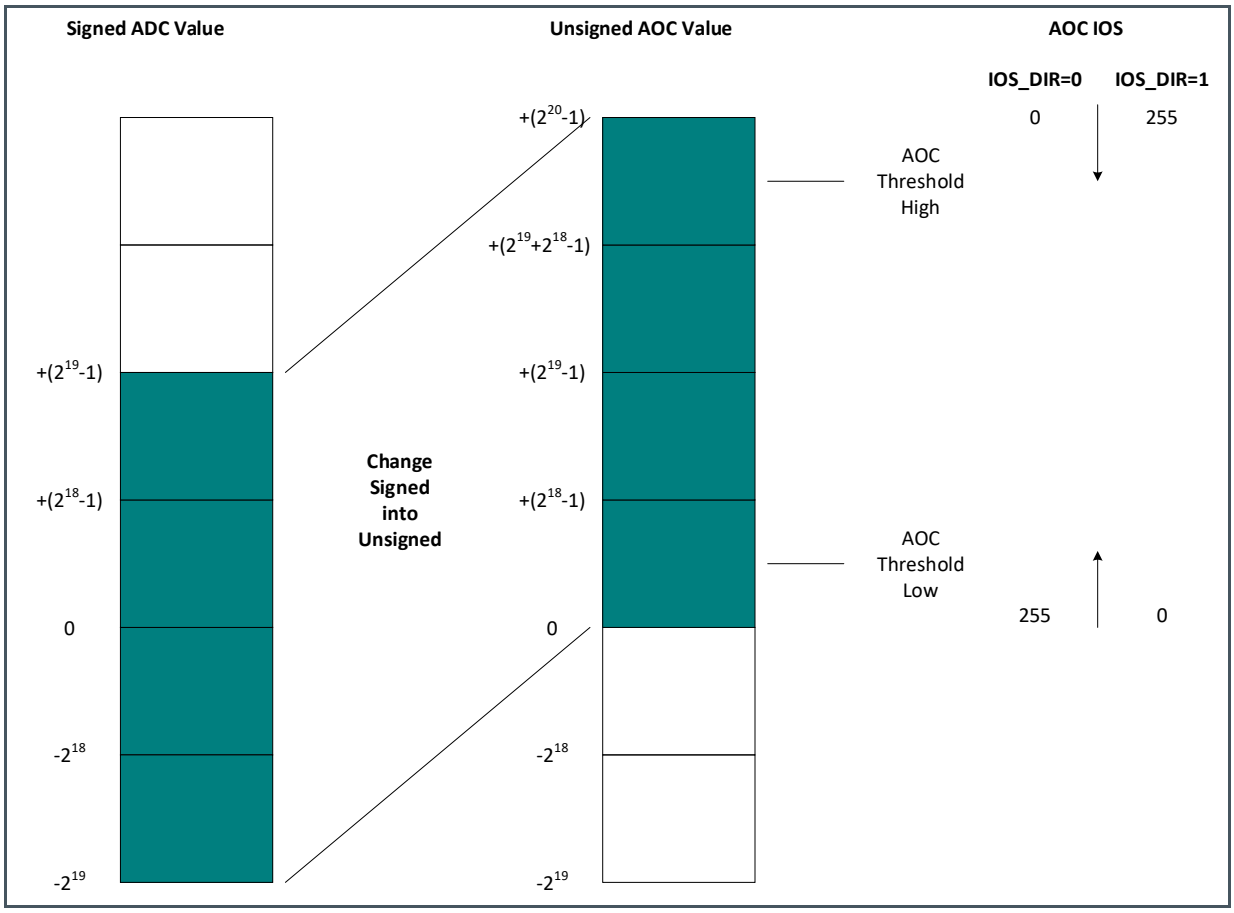


Figure 117:
AOC Function



AOC_MOD1_SEQ1_SUB1 Register (Address 0x70)

Figure 118:
AOC_MOD1_SEQ1_SUB1 Register

Addr: 0x70		AOC_MOD1_SEQ1_SUB1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod1_seq1_sub1	0	R_PUSH	PD Offset for SubSample1 Sequence1 Channel1.

AOC_MOD1_SEQ1_SUB2 Register (Address 0x71)

Figure 119:
AOC_MOD1_SEQ1_SUB2 Register

Addr: 0x71		AOC_MOD1_SEQ1_SUB2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod1_seq1_sub2	0	R_PUSH	PD Offset for SubSample2 Sequence1 Channel1.

AOC_MOD1_SEQ1_SUB3 Register (Address 0x72)

Figure 120:
AOC_MOD1_SEQ1_SUB3 Register

Addr: 0x72		AOC_MOD1_SEQ1_SUB3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod1_seq1_sub3	0	R_PUSH	PD Offset for SubSample3 Sequence1 Channel1.

AOC_MOD1_SEQ1_SUB4 Register (Address 0x73)

Figure 121:
AOC_MOD1_SEQ1_SUB4 Register

Addr: 0x73		AOC_MOD1_SEQ1_SUB4		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod1_seq1_sub4	0	R_PUSH	PD Offset for SubSample4 Sequence1 Channel1.

AOC_MOD1_SEQ1_SUB5 Register (Address 0x74)

Figure 122:
AOC_MOD1_SEQ1_SUB5 Register

Addr: 0x74		AOC_MOD1_SEQ1_SUB5		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod1_seq1_sub5	0	R_PUSH	PD Offset for SubSample5 Sequence1 Channel1.

AOC_MOD1_SEQ1_SUB6 Register (Address 0x75)

Figure 123:
AOC_MOD1_SEQ1_SUB6 Register

Addr: 0x75		AOC_MOD1_SEQ1_SUB6		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod1_seq1_sub6	0	R_PUSH	PD Offset for SubSample6 Sequence1 Channel1.

AOC_MOD1_SEQ1_SUB7 Register (Address 0x76)

Figure 124:
AOC_MOD1_SEQ1_SUB7 Register

Addr: 0x76		AOC_MOD1_SEQ1_SUB7		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod1_seq1_sub7	0	R_PUSH	PD Offset for SubSample7 Sequence1 Channel1.

AOC_MOD1_SEQ1_SUB8 Register (Address 0x77)

Figure 125:
AOC_MOD1_SEQ1_SUB8 Register

Addr: 0x77		AOC_MOD1_SEQ1_SUB8		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod1_seq1_sub8	0	R_PUSH	PD Offset for SubSample8 Sequence1 Channel1.

AOC_MOD1_SEQ2_SUB1 Register (Address 0x78)

Figure 126:
AOC_MOD1_SEQ2_SUB1 Register

Addr: 0x78		AOC_MOD1_SEQ2_SUB1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod1_seq2_sub1	0	R_PUSH	PD Offset for SubSample1 Sequence2 Channel1.

AOC_MOD1_SEQ2_SUB2 Register (Address 0x79)

Figure 127:
AOC_MOD1_SEQ2_SUB2 Register

Addr: 0x79		AOC_MOD1_SEQ2_SUB2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod1_seq2_sub2	0	R_PUSH	PD Offset for SubSample2 Sequence2 Channel1.

AOC_MOD1_SEQ2_SUB3 Register (Address 0x7a)

Figure 128:
AOC_MOD1_SEQ2_SUB3 Register

Addr: 0x7a		AOC_MOD1_SEQ2_SUB3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod1_seq2_sub3	0	R_PUSH	PD Offset for SubSample3 Sequence2 Channel1.

AOC_MOD1_SEQ2_SUB4 Register (Address 0x7b)

Figure 129:
AOC_MOD1_SEQ2_SUB4 Register

Addr: 0x7b		AOC_MOD1_SEQ2_SUB4		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod1_seq2_sub4	0	R_PUSH	PD Offset for SubSample4 Sequence2 Channel1.

AOC_MOD2_SEQ1_SUB1 Register (Address 0x7c)

Figure 130:
AOC_MOD2_SEQ1_SUB1 Register

Addr: 0x7c		AOC_MOD2_SEQ1_SUB1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod2_seq1_sub1	0	R_PUSH	PD Offset for SubSample1 Sequence1 Channel2.

AOC_MOD2_SEQ1_SUB2 Register (Address 0x7d)

Figure 131:
AOC_MOD2_SEQ1_SUB2 Register

Addr: 0x7d		AOC_MOD2_SEQ1_SUB2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod2_seq1_sub2	0	R_PUSH	PD Offset for SubSample2 Sequence1 Channel2.

AOC_MOD2_SEQ1_SUB3 Register (Address 0x7e)

Figure 132:
AOC_MOD2_SEQ1_SUB3 Register

Addr: 0x7e		AOC_MOD2_SEQ1_SUB3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod2_seq1_sub3	0	R_PUSH	PD Offset for SubSample3 Sequence1 Channel2.

AOC_MOD2_SEQ1_SUB4 Register (Address 0x7f)

Figure 133:
AOC_MOD2_SEQ1_SUB4 Register

Addr: 0x7f		AOC_MOD2_SEQ1_SUB4		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod2_seq1_sub4	0	R_PUSH	PD Offset for SubSample4 Sequence1 Channel2.

AOC_MOD2_SEQ1_SUB5 Register (Address 0x80)

Figure 134:
AOC_MOD2_SEQ1_SUB5 Register

Addr: 0x80		AOC_MOD2_SEQ1_SUB5		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod2_seq1_sub5	0	R_PUSH	PD Offset for SubSample5 Sequence1 Channel2.

AOC_MOD2_SEQ1_SUB6 Register (Address 0x81)

Figure 135:
AOC_MOD2_SEQ1_SUB6 Register

Addr: 0x81		AOC_MOD2_SEQ1_SUB6		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod2_seq1_sub6	0	R_PUSH	PD Offset for SubSample6 Sequence1 Channel2.

AOC_MOD2_SEQ1_SUB7 Register (Address 0x82)

Figure 136:
AOC_MOD2_SEQ1_SUB7 Register

Addr: 0x82		AOC_MOD2_SEQ1_SUB7		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod2_seq1_sub7	0	R_PUSH	PD Offset for SubSample7 Sequence1 Channel2.

AOC_MOD2_SEQ1_SUB8 Register (Address 0x83)

Figure 137:
AOC_MOD2_SEQ1_SUB8 Register

Addr: 0x83		AOC_MOD2_SEQ1_SUB8		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod2_seq1_sub8	0	R_PUSH	PD Offset for SubSample8 Sequence1 Channel2.

AOC_LEDOFF Register (Address 0x84)

Figure 138:
AOC_LEDOFF Register

Addr: 0x84		AOC_LEDOFF		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_ledoff	0	RW	PD Offset for LED off (Double and Triple Sampling).

AOC_CFG Register (Address 0x85)

Figure 139:
AOC_CFG Register

Addr: 0x85		AOC_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	dis_ledoff	0	RW	Disable PD Offset for LED off (Double and Triple Sampling). Use PD Offset for SubSample.
2:0	aoc_ovs	0	RW	Value for oversampling AOC Oversampling = 2^(aoc_ovs+3)

AOC_MOD1_THH Register (Address 0x86)

Figure 140:
AOC_MOD1_THH Register

Addr: 0x86		AOC_MOD1_THH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod1_thh	255	RW	Threshold for decreasing the PD_OFFSET for all SubSamples for Modulator1.

AOC_MOD1_THL Register (Address 0x87)

Figure 141:
AOC_MOD1_THL Register

Addr: 0x87		AOC_MOD1_THL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod1_thl	0	RW	Threshold for increasing the PD_OFFSET for all SubSamples for Modulator1.

AOC_MOD2_THH Register (Address 0x88)

Figure 142:
AOC_MOD2_THH Register

Addr: 0x88		AOC_MOD2_THH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod2_thh	255	RW	Threshold for decreasing the PD_OFFSET for all SubSamples for Modulator2.

AOC_MOD2_THL Register (Address 0x89)

Figure 143:
AOC_MOD2_THL Register

Addr: 0x89		AOC_MOD2_THL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	aoc_mod2_thl	0	RW	Threshold for increasing the PD_OFFSET for all SubSamples for Modulator2.

AOC_SAR_TRES Register (Address 0x8a)

Figure 144:
AOC_SAR_TRES Register

Addr: 0x8a		AOC_SAR_TRES		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	sar_thres	128	RW	Threshold for SAR for all SubSamples.

MOD1_SEQ1_AOC_EN Register (Address 0x8b)

Figure 145:
MOD1_SEQ1_AOC_EN Register

Addr: 0x8b		MOD1_SEQ1_AOC_EN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	mod1_seq1_aoc_en	0	RW	Enable AOC for Subsamples 1 to 8 in Sequence1 for Modulator1.

Bit	Subsample
7	8
6	7
5	6
4	5
3	4
2	3

Addr: 0x8b		MOD1_SEQ1_AOC_EN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				1 2
				0 1

MOD2_SEQ1_AOC_EN Register (Address 0x8c)

Figure 146:
MOD2_SEQ1_AOC_EN Register

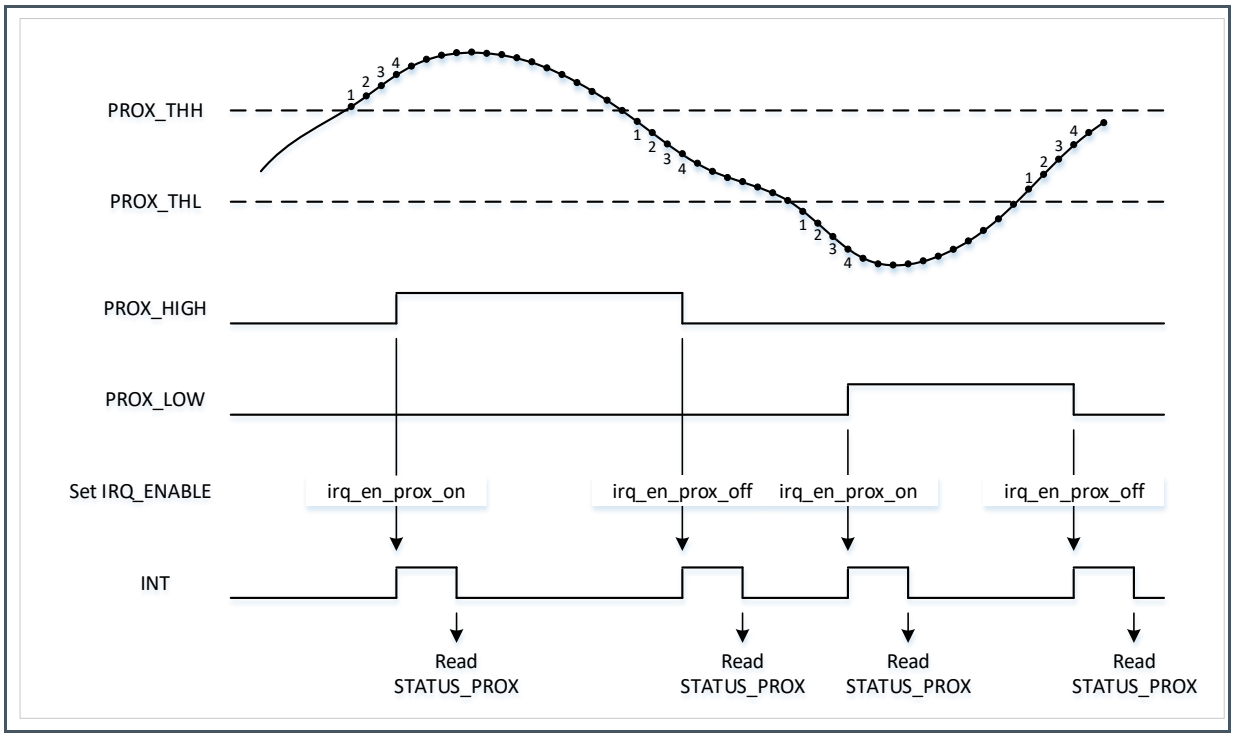
Addr: 0x8c		MOD2_SEQ1_AOC_EN		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1:0	Mod2_seq1_aoc_en	0	RW	Enable AOC for Subsamples 1 to 2 in Sequence1 for Modulator2.

7.2.4 Proximity Detection

The AS7056 has an integrated proximity detection, with separate programmable high and low threshold values, such that a high threshold is more than a low threshold. The proximity output is low, in case the measured proximity signal value is between the threshold values, else it is high. The Proximity output is an additional signal to the two PPG signal outputs.

The Proximity threshold sample sequence is programmable from one up to eight samples to trigger the Interrupt. It means if the complete programmed Proximity threshold sample sequence (1-8) is above or below the threshold, an Interrupt will be triggered.

Figure 147:
AS7056 Proximity Detection



PROX_CFG Register (Address 0x98)

Figure 148:
PROX_CFG Register

Addr: 0x98		PROX_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	prox_en	0	RW	Enable Proximity
1:0	prox_sub	0	RW	Select SubSample for Proximity; MOD1_SEQ2: 0-3: SUB1-SUB4

PROX_OVS Register (Address 0x99)

Figure 149:
PROX_OVS Register

Addr: 0x99		PROX_OVS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:4	prox_on_ovs	0	RW	Oversampling for Proximity up.
2:0	prox_off_ovs	0	RW	Oversampling for Proximity down.

PROX_THH_L Register (Address 0x9a)

Figure 150:
PROX_THH_L Register

Addr: 0x9a		PROX_THH_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	prox_thh[7:0]	0	RW	Threshold High for Proximity.

PROX_THH_H Register (Address 0x9b)

Figure 151:
PROX_THH_H Register

Addr: 0x9b		PROX_THH_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	prox_thh[15:8]	0	RW	Threshold High for Proximity.

PROX_THL_L Register (Address 0x9c)

Figure 152:
PROX_THL_L Register

Addr: 0x9c		PROX_THL_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	prox_thl[7:0]	0	RW	Threshold Low for Proximity.

PROX_THL_H Register (Address 0x9d)

Figure 153:
PROX_THL_H Register

Addr: 0x9d		PROX_THL_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	prox_thl[15:8]	0	RW	Threshold Low for Proximity.

7.2.5 FIFO Register

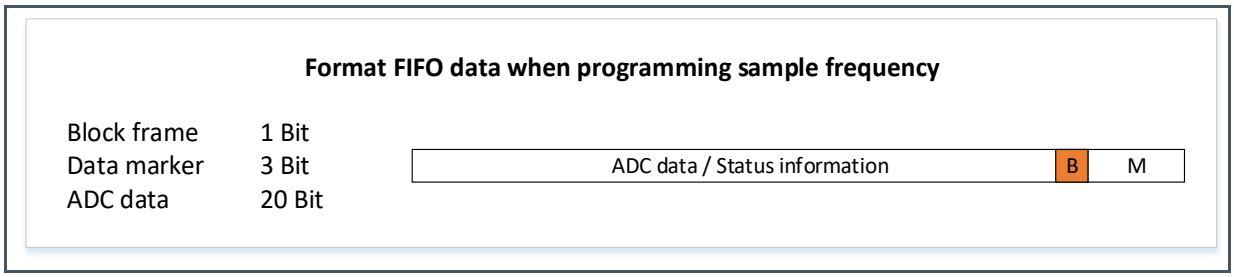
The AS7056 provides a 1.5 kB FIFO register for buffering the measurement data output to an external microcontroller via the I^2C interface. The FIFO buffering allows the external MCU to stay in idle mode during energy-saving measurements.

The measurement data of the two channels after oversampling and possible status information from the AOC will be collected in a common data stream and written to the FIFO.

The coding of the data stream is described below in Figure 154.

The data stream is divided into blocks of 100 data of 24 bits each. The first five data have the block frame = "11100". Another block frame = "00", is no longer available within the block.

Figure 154:
FIFO Data Format



Data Marker (3 Bits)

- 000 – first ADC data Sequence1 Modulator1
- 001 – first ADC data Sequence2 Modulator1
- 010 – other ADC data Modulator1
- 011 – first ADC data Sequence1 Modulator2
- 100 – first ADC data Sequence2 Modulator2
- 101 – other ADC data Modulator2
- 110 – SAR Status
- 111 – AOC Status

Figure 155:
Description AOC Status

AOC Status 20Bit

MOD1=4'h0	SUB8	SUB7	SUB6	SUB5	SUB4	SUB3	SUB2	SUB1
MOD2=4'h2	00	00	00	00	00	00	SUB2	SUB1

Change AOC value per SubSample = 2 Bit
Bit 0 = 1 – Input current from PD on the modulator is decreased
Bit 1 = 1 – Input current from PD on the modulator is increased

The following ADC values will be measured with a new AOC Value.

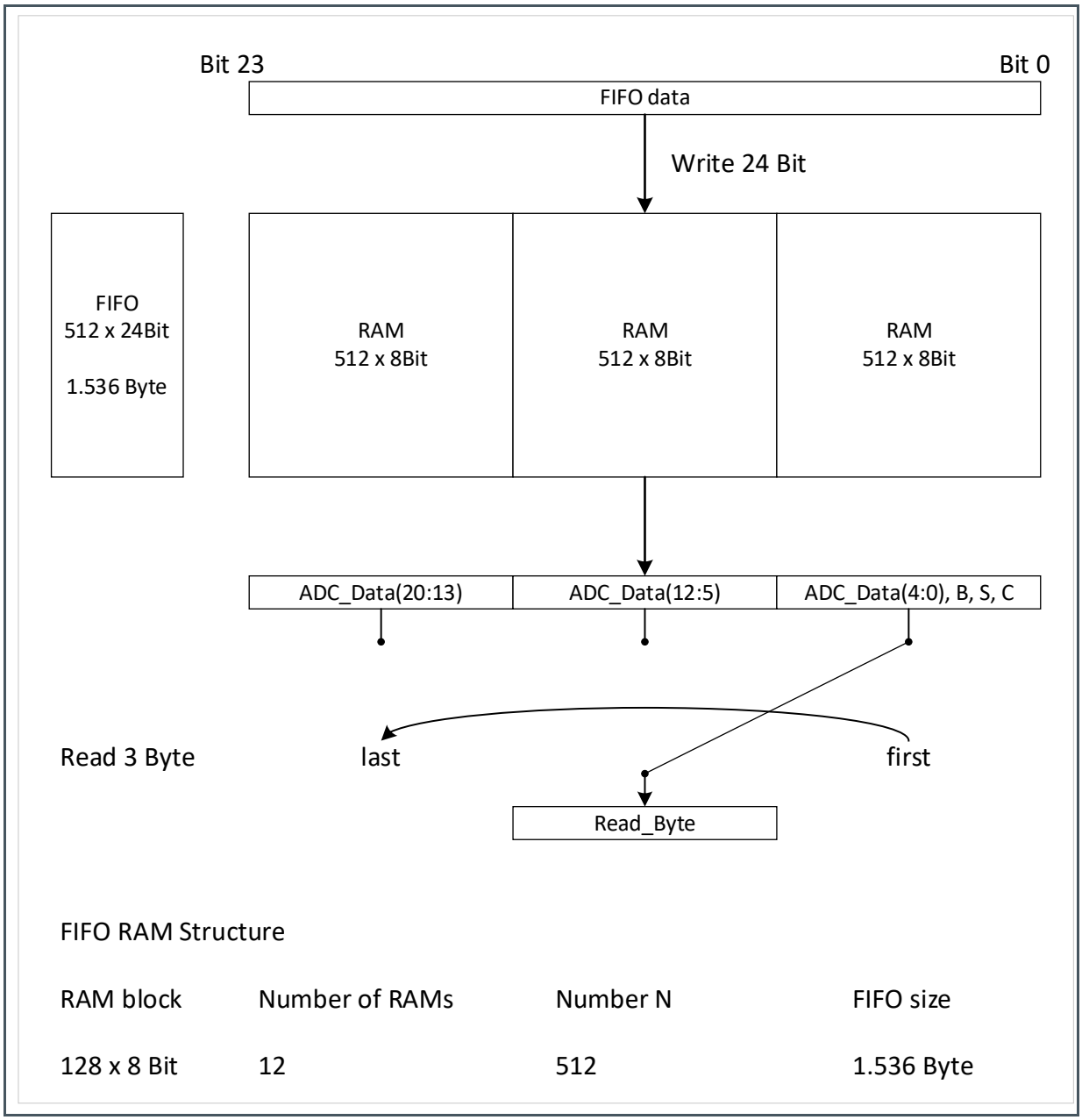
Figure 156:
Description SAR Status

SAR Status 20Bit

6Bit	1Bit	1Bit	4Bit	8Bit
6'h00	MOD	SEQ	SUB	PD Offset

MOD: 0 – Modulator 1, 1 – Modulator 2
SEQ: 0 – Sequence 1, 1 – Sequence 2
SUB: 0...7 (Seq1) – SUB Sample 1...8
0...3 (Seq2) – SUB Sample 1...4

Figure 157:
FIFO Data Structure and Organization



FIFO_THRESHOLD Register (Address 0xd0)

Figure 158:
FIFO_THRESHOLD Register

Addr: 0xd0		FIFO_THRESHOLD		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	fifo_threshold[7:0]	64	RW	FIFO threshold bit 7:0

FIFO_CTRL Register (Address 0xd1)

Figure 159:
FIFO_CTRL Register

Addr: 0xd1		FIFO_CTRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	fifo_clear	0	PUSH	Write 1 here to clear the FIFO.
3	sar_data_en	0	RW	Write 4 bit SAR into SINC data bit (3:0).
0	fifo_threshold[8]	0	RW	FIFO threshold bit 8.

7.2.6 Interrupt Logic

The interrupt manager processes the interrupt events. These interrupt events must be released for processing via an interrupt enable register. The interrupt status is automatically reset when the STATUS register is read (auto-zero register). In this way, no interrupt events may be lost.

IRQ_ENABLE Register (Address 0x3f)

Figure 160:
IRQ_ENABLE Register

Addr: 0x3f		IRQ_ENABLE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	irq_en_prox_on	0	RW	Rising Edge PROX_HIGH or PROX_LOW.
6	irq_en_prox_off	0	RW	Falling Edge PROX_HIGH or PROX_LOW.

Addr: 0x3f		IRQ_ENABLE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5	irq_en_vcsel	0	RW	VCSEL Safety control interrupt
4	irq_en_asat	0	RW	Analog Saturation Interrupt.
3	irq_en_led_lowvds	0	RW	LED lowvds Interrupt.
2	irq_en_fifooverflow	0	RW	FIFO overflow occurred. ERROR: "new sample is lost"
1	irq_en_fifothreshold	0	RW	FIFO is almost full, FIFO_LEVEL > FIFO_THRESHOLD
0	irq_en_sequencer	0	RW	

7.2.7 I/O Control

CONTROL Register (Address 0x10)

Figure 161:
CONTROL Register

Addr: 0x10		CONTROL			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
0	i2c_fm_plus	0	RW	I^2C fastmode plus with 1 MHz 0-off, 1-on	
				Number	**Function**
				0	Off
				1	On

CGB_CFG Register (Address 0x11)

Figure 162:
CGB_CFG Register

Addr: 0x11		CGB_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	bgcal_done_sel	0	RW	Select which signal is used to stop the calibration.

Addr: 0x11		CGB_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
				Number **Function** 0 Run only one calibration cycle. 1 Run calibration until LF oscillator is close to 32 kHz.
6	bgcal_en	0	PUSH1	Start calibration of the LF oscillator.
2	pll_on	0	RW	Turn the pll to 20 MHz; needs to be enabled after hf_osc_en (min. 30 µs). **Number** **Function** 0 Off 1 On
1	hf_osc_on	0	RW	Turn the hf oscillator to 2 MHz; needs to be enabled after lf_osc_en (min. 100 µs). **Number** **Function** 0 Off 1 On
0	lf_osc_on	0	RW	Turn the lf oscillator to 32 KHz. **Number** **Function** 0 Off 1 On

INT_CFG Register (Address 0x12)

Figure 163:
INT_CFG Register

Addr: 0x12		INT_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6	int_e2	0	RW	Set the output driver strength high with 1.
5	int_e4	0	RW	Set the output driver strength high again with 1.

Addr: 0x12		INT_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	int_sr	0	RW	Set the slew rate to another value with 1.
3	int_pu	0	RW	PU=1 then pull-up if IO is activated.
2	int_pd	0	RW	PD=1 then pull-down if IO is activated.
0	int_inv	0	RW	Inverting interrupt.

CSXN_CFG Register (Address 0x13)

Figure 164:
CSXN_CFG Register

Addr: 0x13		CSXN_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6	csxn_e2	0	RW	Set the output driver strength high with 1.
5	csxn_e4	1	RW	Set the output driver strength high again with 1.
4	csxn_sr	0	RW	Set the slew rate to another value with 1.
3	csxn_pu	0	RW	PU=1 -> pull-up @ IO activated.
2	csxn_pd	0	RW	PD=1 -> pull-down @ IO activated.

IO_CFG Register (Address 0x14)

Figure 165:
IO_CFG Register

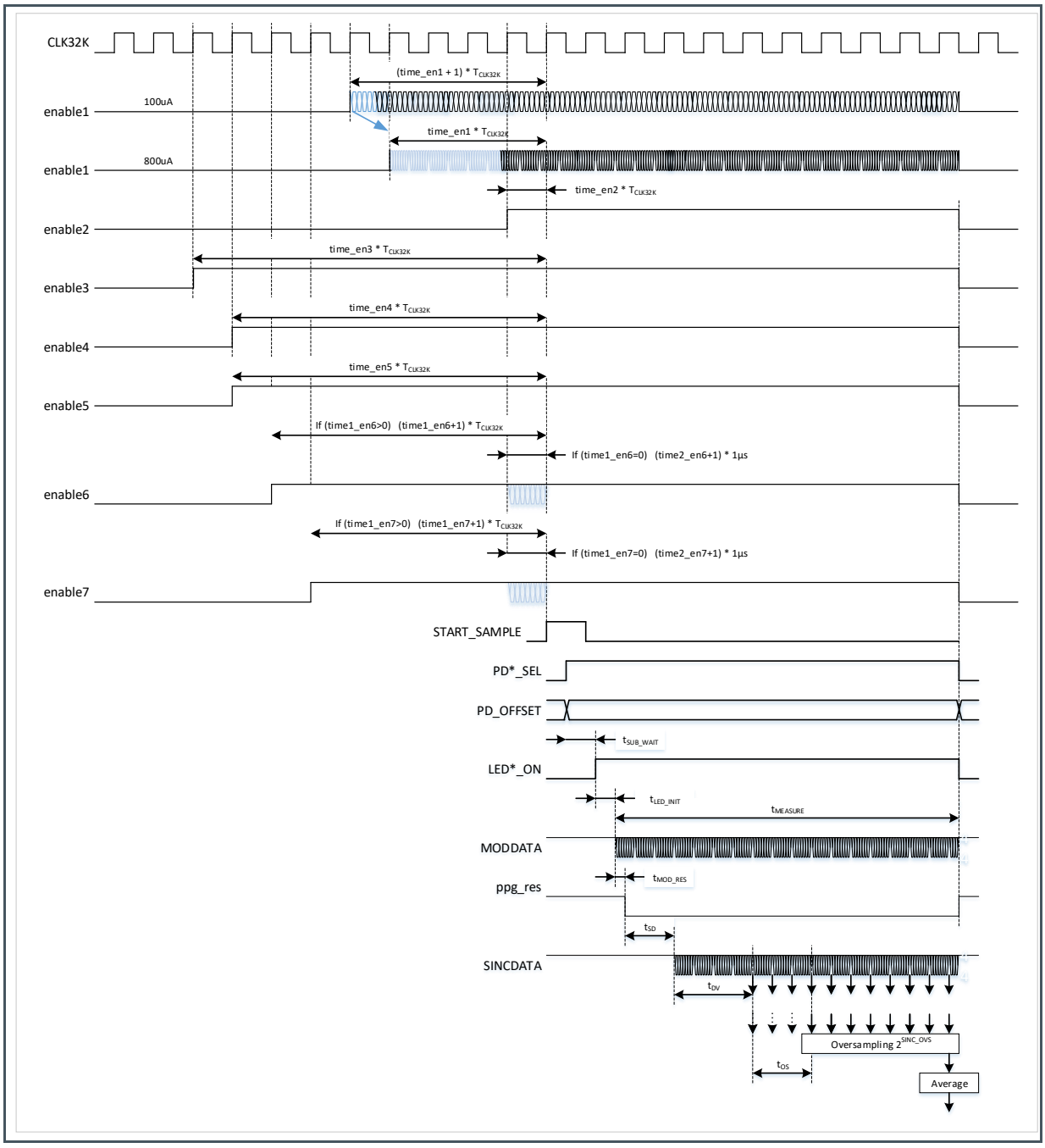
Addr: 0x14		IO_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6	sda_e2	0	RW	Set the output driver strength high with 1.
5	sda_e4	1	RW	Set the output driver strength high again with 1.

Addr: 0x14		IO_CFG		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	sda_sr	0	RW	Set the slew rate to another value with 1.

7.2.8 Standby

The standby registers are part of the AS7056 power management to reduce the power consumption of the AS7056 and the measurement system itself. In addition, during continuous measurements, blocks such as ADCs, clock generation, or reference block, can switch in standby mode between several PPG sample slots if it is inactive. For usage of the standby functionality, the dedicated registers have to be activated. In the standard default setting, the automatic standby is disabled. That means all blocks are always active as long as no standby is activated. Depending on the programmed sequences, the blocks automatically switch to standby.

Figure 166:
Standby Time Behavior



Depending on the time setting, the activated enable signal is switched on before starting sample measurements (level = 1) and switched off again, as soon as possible, after the measurement finishes (level = 0).

When the enable signal is switched on, all assigned signals receive the state programmed in the configuration.

When the enable signal is switched off, all assigned signals are switched to the inactive level (see Figure 167).

Automatic Standby Enabled (dynamic enable)

When the STANDBY_ON is set to 0x7F i.e. all to one, all the enabled signals are reset to zero except for byp_ref_lp, which is set to 1 and can be sequentially turned on, but not all at once. These enabled signals will be turned on with the configured stby_en time. In this case, STANDBY_ENx registers turn on the corresponding enable signal after a configured amount of time. This time is given as the STANDBY_ENx register value times 31.25 µs (period of the low-frequency clock .i.e. 32 kHz). However, to enable STANDBY_EN6 and STANDBY_EN7, 32 kHz or the 1 MHz clock dictates the delay time before the enable signal is turned on. Bit 7:5 for these two registers allows the delay to be set by the 32 kHz clock, while bit 4:0 allows the delay to be set by the 1 MHz clock. The pattern in which the delay is set is the same as described above for the other registers, i.e. the decimal value of bits 7:5 times 31.25 µs, or the decimal value of bits 4:0 times 1 µs. The default values of STANDBY_ENx registers are shown in Figure 167 below.

Figure 167:
Dynamic-Enabled Standby

				Standby	MOD1 Enabled	MOD2 Enabled	MOD1/2 Enabled
Register	**Address**	**Bit**	**Bit Name**	**0**	**1**	**2**	**3**
CGB_CFG	0x11	2	pll_on	Automatic	1	1	1
		1	hf_osc_on		1	1	1
		0	lf_osc_on		1	1	1
REF_CFGA	0x15	7	en_bg		1	1	1
		5	en_vcm_ppg		1	1	1
		3	en_vr_led		1	1	1
		2	en_bias		1	1	1
		0	byp_ref_lp		0	0	0
MOD1_CFGA	0x1b	4	mod1_en		1	0	1
MOD2_CFGA	0x21	4	mod2_en		0	1	1
STANDBY_ON	0x21	6:0	stby_en_on		0x7f	0x7f	0x7f
STANDBY_EN1	0xa1	7:0	stby_en1_time		4	4	4
STANDBY_EN2	0xa2	7:0	stby_en2_time		2	2	2
STANDBY_EN3	0xa3	7:0	stby_en3_time		4	4	4
STANDBY_EN4	0xa4	7:0	stby_en4_time		0	0	0
STANDBY_EN5	0xa5	7:0	stby_en5_time		3	3	3
STANDBY_EN6	0xa6	7:5	stby_en6_time1		0	0	0
STANDBY_EN6	0xa6	4:0	stby_en6_time2		16	16	16
STANDBY_EN7	0xa6	7:5	stby_en7_time1		0	0	0
STANDBY_EN7	0xa6	4:0	stby_en7_time2		16	16	16

Automatic Standby Disabled (static enable)

Enable signals for PLL, Oscillators, bandgap reference, LED drivers, IOS DAC, IREF DAC, MOD1, and MOD2, are contained in the configuration registers shown in Figure 168. There is a special register, which allows you to turn on all the enabled signals at once, or one-by-one in a sequential fashion. When the value of this 7-bit register, STANDBY_ON, is set to 0x00, i.e. all zeros, all the enable signals follow the values specified in the registers below. The values in the registers STANDBY_ENx should be set to 0x00. Figure 168 describes the power-down mode and other operational modes where only MOD1 or MOD2, or both of them are enabled.

Figure 168:
Static Enabled Standby

				Power Down	MOD1 Enabled	MOD2 Enabled	MOD1/2 Enabled
Register	**Address**	**Bit**	**Bit Name**	**0**	**1**	**2**	**3**
CGB_CFG	0x11	2	pll_on	0	1	1	1
		1	hf_osc_on	0	1	1	1
		0	lf_osc_on	0	1	1	1
REF_CFGA	0x15	7	en_bg	0	1	1	1
		5	en_vcm_ppg	0	1	1	1
		3	en_vr_led	0	1	1	1
		2	en_bias	0	1	1	1
		0	byp_ref_lp	0	0	0	0
MOD1_CFGA	0x1b	4	mod1_en	0	1	0	1
MOD2_CFGA	0x21	4	mod2_en	0	0	1	1
STANDBY_ON	0x21	6:0	stby_en_on	0	0	0	0

Extended Power-Saving Options

Besides using sequential enabling of the circuit blocks as described above, bias currents, through certain circuit blocks, can also be minimized for enhanced power saving.

- **MOD Bias:** The MOD_CFGA register controls the bias current for MOD1 and MOD2 circuit blocks. This 2-bit register can be set to one, which enables a reduction of the bias current by 50%.
- **Reference Bias:** Similar to configuring the bias current of MOD1 and MOD2, the bias current of VCM buffers inside the reference block can also be controlled. The control bit is bit 1 of the register REF_CFGA. Setting this bit to 1 enables a 50% reduction in the bias current.

The standby delay times of enable signals can be independently optimized by sweeping the STANDBY_ENx registers. For instance, if we set STANDBY_ON as 1000000, enable 2-7 signals will be set according to their values inside the configuration register. However, enable signal 1, which turns on the clock generator block, will be switched on after a delay defined by the register STANDBY_EN1. We can sweep the value of STANDBY_EN1, say from 0-7, and optimize the standby delay time for the clock generator block. The same optimization can also be performed for other

enable signals independently. For instance, to optimize standby time for the bandgap circuit, we set STANDBY_ON to 0010000 and sweep STANDBY_EN3 from 0 to 7, as shown in Figure 169 below.

Figure 169:
STANDBY Timing Optimization

Standby					CGB	VRLED	Bandgap	byp_ref_lp	IREF	VCM-time2	VCM- time1	MOD-time2	MOD-time1
Register	Address	Bit	en	Bit Name	en1 31u	en2 31u	en3 31u	en4 31u	en5 31u	en6 1u	en6 31u	en7 1u	en7 31u
CGB_CFG	0x11	2	en1	pll_on	1								
		1	en1	Hf_osc_on	1								
		0	-	Lf_osc_on	1								
REF_CFGA	0x15	7	en3	en_bg	1								
		5	en6	en_vcm_ppg	1								
		3	en2	en_vr_led	1								
		2	en5	en_bias	1								
		0	en4	byp_ref_lp	0								
MOD1_CFGA	0x1b	4	en7	mod1_en	1								
MOD2_CFGA	0x21	4	en7	mod2_en	1								
STANDBY_ON	0x21	6:0		stby_en_on	1	2	4	8	16	32	32	64	64
STANDBY_EN1	0xa1	7:0		stby_en1_time	0..7	x	x	x	x	x	x	x	x
STANDBY_EN2	0xa2	7:0		stby_en2_time	x	0..7	x	x	x	x	x	x	x
STANDBY_EN3	0xa3	7:0		stby_en3_time	x	x	0..7	x	x	x	x	x	x
STANDBY_EN4	0xa4	7:0		stby_en4_time	x	x	x	0..7	x	x	x	x	x
STANDBY_EN5	0xa5	7:0		stby_en5_time	x	x	x	x	0..7	x	x	x	x
STANDBY_EN6	0xa6	7:5		stby_en6_time1	x	x	x	x	x	0(1)	1..7	x	x
STANDBY_EN6	0xa6	4:0		stby_en6_time2	x	x	x	x	x	31..0	x	x	x
STANDBY_EN7	0xa7	7:5		stby_en7_time1	x	x	x	x	x	x	x	0(1)	1..7
STANDBY_EN7	0xa7	4:0		stby_en7_time2	x	x	x	x	x	x	x	31..0	x

(1) stby_en6/7_time2 is enabled by setting stby_en6/7_time1 to 0

STANDBY_ON Register (Address 0xa0)

Figure 170:
STANDBY_ON Register

Addr: 0xa0		STANDBY_ON		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:0	stby_en_on	0	RW	Set on Standby Enable 1...7

STANDBY_EN1 Register (Address 0xa1)

Figure 171:
STANDBY_EN1 Register

Addr: 0xa1		STANDBY_EN1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	stby_en1_time	4	RW	Time for Enable1 N * TCLK_32 KHz

STANDBY_EN2 Register (Address 0xa2)

Figure 172:
STANDBY_EN2 Register

Addr: 0xa2		STANDBY_EN2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	stby_en2_time	2	RW	Time for Enable2 N * TCLK_32 KHz

STANDBY_EN3 Register (Address 0xa3)

Figure 173:
STANDBY_EN3 Register

Addr: 0xa3		STANDBY_EN3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	stby_en3_time	4	RW	Time for Enable3 N * TCLK_32 KHz

STANDBY_EN4 Register (Address 0xa4)

Figure 174:
STANDBY_EN4 Register

Addr: 0xa4		STANDBY_EN4		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	stby_en4_time	0	RW	Time for Enable4 N * TCLK_32 KHz

STANDBY_EN5 Register (Address 0xa5)

Figure 175:
STANDBY_EN5 Register

Addr: 0xa5		STANDBY_EN5		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	stby_en5_time	3	RW	Time for Enable5 N * TCLK_32 KHz

STANDBY_EN6 Register (Address 0xa6)

Figure 176:
STANDBY_EN6 Register

Addr: 0xa6		STANDBY_EN6			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:5	stby_en6_time1	0	RW	Time1 for Enable6 N * TCLK_32 KHz	
				Number	**Value**
				0	time2_en5 is active
				others	(N+1) * TCLK_32 KHz
4:0	stby_en6_time2	16	RW	Time2 for Enable6 N * TCLK_2 MHz	

STANDBY_EN7 Register (Address 0xa7)

Figure 177:
STANDBY_EN7 Register

Addr: 0xa7		STANDBY_EN7			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:5	stby_en7_time1	0	RW	Time1 for Enable7 N * TCLK_32 KHz	
				Number	**Value**
				0	time2_en5 is active
				others	(N+1) * TCLK_32 KHz
4:0	stby_en7_time2	16	RW	Time2 for Enable7 N * TCLK_2 MHz	

7.2.9 Status Registers

PRODUCT_ID Register (Address 0xec)

Figure 178:
PRODUCT_ID Register

Addr: 0xec		PRODUCT_ID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	otp_part_id	0	RO	Image of the OTP bit for part_id in P2RAM.

SILICON_ID Register (Address 0xed)

Figure 179:
SILICON_ID Register

Addr: 0xed		SILICON_ID		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	silicon_id	0	RO	Silicon Identification

REVISION Register (Address 0xee)

Figure 180:
REVISION Register

Addr: 0xee		REVISION		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	revision	0	RO	Revision Number Identification

CHIP_CTRL Register (Address 0xef)

Figure 181:
CHIP_CTRL Register

Addr: 0xef		CHIP_CTRL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	chip_reset	0	PUSHPOP	Chip Reset Effect like Power On Reset

SEQ_START Register (Address 0xf0)

Figure 182:
SEQ_START Register

Addr: 0xf0		SEQ_START		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	start_seq	0	R_PUSH	Start and stop of the measurements. **Number** / **Function** 0 – Stop 1 – Start the number of measurements as specified in the SEQ_SAMPLE register.

STATUS_CGBB Register (Address 0xf4)

Figure 183:
STATUS_CGBB Register

Addr: 0xf4		STATUS_CGBB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	pll_lock	0	RO	PLL locked state indicator PLL_LOCK=1 then PLL is in the locked state_OK
2	clk_pll_ok	0	RO	Status indicator of CLK20M CLK_PLL_OK =1 then CLK20M clock is running

Addr: 0xf4		STATUS_CGBB		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1	lf_bgcal_ok	0	RO	LF_OSC last frequency calibration cycle done and frequency is ok
0	lf_bgcal_ready	0	RO	LF_OSC last frequency calibration cycle done

STATUS_SEQ Register (Address 0xf5)

Figure 184:
STATUS_SEQ Register

Addr: 0xf5		STATUS_SEQ		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1	seq_end	0	RO	Measurement was stopped.
0	seq_error	0	RO	Measurement of a Sample was not started. Sample frequency is too high.

STATUS_LED Register (Address 0xf6)

Figure 185:
STATUS_LED Register

Addr: 0xf6		STATUS_LED			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
2:0	led_lowvds	0	RO	Low_vds signal if active, the LED current does not reach the expected value.	
				Bit	**LED Driver**
				2	LED driver 3
				1	LED driver 2
				0	LED/VCSEL driver 1

STATUS_ASAT Register (Address 0xf7)

Figure 186:
STATUS_ASAT Register

Addr: 0xf7		STATUS_ASAT		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	mod1_asat	0	RO	Analog Saturation Modulator1.
3:0	mod2_asat	0	RO	Analog Saturation Modulator2.

As long as the input signals of each modulator are in range, all bits of the mod1_asat and mod2_asat registers are in status 0.

STATUS_VCSEL Register (Address 0xf8)

Figure 187:
STATUS_VCSEL Register

Addr: 0xf8		STATUS_VCSEL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	vcsel_short_vss	0	RO	VCSEL Safety CTRL; short to GND detected.
1	vcsel_short_vdd	0	RO	VCSEL Safety CTRL; short to VCSELS detected.
0	vcsel_wd	0	RO	VCSEL Safety CTRL; LED on time longer than maximal on time detected.

STATUS_PROX Register (Address 0xf9)

Figure 188:
STATUS_PROX Register

Addr: 0xf9		STATUS_PROX		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description(1)**
6	prox_high	0	RO	
5	prox_high_on	0	RO	
4	prox_high_off	0	RO	

Addr: 0xf9		STATUS_PROX		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description(1)**
2	prox_low	0	RO	
1	prox_low_on	0	RO	
0	prox_low_off	0	RO	

(1) See Figure 147.

STATUS Register (Address 0xfa)

The STATUS register shows the current status of the interface. When released via IRQ_ENABLE, all bits can trigger an interrupt. Reading the STATUS registers only deletes irq_iir_overflow, irq_fifooverflow and irq_sequencer.

To delete irq_prox, the STATUS_PROX register must be read.
To delete irq_vcsel, the STATUS_VCSEL register must be read.
To delete irq_asat, the STATUS_ASAT register must be read.
To delete irq_lowvds, the STATUS_LED register must be read.
To delete irq_sequencer, the STATUS_SEQ register must be read.
The interrupt for the fill level of the FIFO irq_fifothreshold cannot be deleted directly, but only by lowering the FIFO level.

Figure 189:
STATUS Register

Addr: 0xfa		STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	irq_prox	0	RO	Proximity Interrupt check Register STATUS_PROX
6	irq_vcsel	0	RO	VCSEL short to VDD/VSS or VCSEL watchdog detection check Register STATUS_VCSEL
5	irq_asat	0	RO	Analog Saturation Interrupt check Register STATUS_ASAT
4	irq_led_lowvds	0	RO	LED lowvds Interrupt check Register STATUS_LED
3	irq_fifooverflow	0	RO	FIFO overflow occurred. ERROR: "new sample is lost"

Addr: 0xfa		STATUS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	irq_fifothreshold	0	RO	FIFO is almost full, FIFO_LEVEL > FIFO_THRESHOLD
0	irq_sequencer	0	RO	

FIFO_LEVEL0 Register (Address 0xfb)

Figure 190:
FIFO_LEVEL0 Register

Addr: 0xfb		FIFO_LEVEL0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	fifo_level[7:0]	0	RO	FIFO level bit 7:0 of the 24-bit samples

FIFO_LEVEL1 Register (Address 0xfc)

Figure 191:
FIFO_LEVEL1 Register

Addr: 0xfc		FIFO_LEVEL1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	fifo_overflow	0	RO	FIFO overflow
1:0	fifo_level[9:8]	0	RO	FIFO level Bit 9:8 of the 24-bit samples

FIFOL Register (Address 0xfd)

The FIFO can be read with individual read accesses (three consecutive I^2C addresses for a FIFO entry) or with burst read accesses (n * 3 bytes for n FIFO entry). By reading FIFOL, a FIFO entry is read from the FIFO and the FIFO level is reduced. If you read beyond the end of the FIFO, the last FIFO entry will be repeated. There is no underflow flag; this is not an error condition. The FIFO level is 512 entries.

Figure 192:
FIFOL Register

Addr: 0xfd		FIFOL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	fifol	0	PUSHPOP	Low byte of the FIFO. Start address for FIFO burst. **Bit** / **Function** 7:4 – Bits 3:0 of ADC 3 – Block frame 2:0 – Data marker

FIFOM Register (Address 0xfe)

Figure 193:
FIFOM Register

Addr: 0xfe		FIFOM		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	fifom	0	PUSHPOP	Middle byte of the FIFO: bits 11..4 of ADC; on burst read the address jumps back to FIFOL.

FIFOH Register (Address 0xff)

Figure 194:
FIFOH Register

Addr: 0xff		FIFOH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	fifoh	0	PUSHPOP	High byte of the FIFO: bits 19..12 of ADC.

7.2.10 I²C Interface

The AS7056 Biosignal AFE provides a digital I²C slave interface used for the external control of the measurement setup and the control of all functions for the internal features. The AS7056 supports single and burst access via the I²C. Single access requires about 50% more time compared to burst access, for the transmission of the same amount of data.

The AS7056 I²C slave uses an I²C address of 0x55, 0x53, 0x51, and 0x52 (7-bit format; 1-bit R/W bit has to be added) respectively 60 h and 61 h. It expects external pull-up resistors.

I²C Feature List

- Fast mode (400 kHz) and standard mode (100 kHz) support.
- 7+1-bit addressing mode.
- Write formats: Single-Byte-Write, Burst-Write.
- Read formats: Current-Address-Read, Random-Read, Sequential-Read.
- SDA input delay and SCL spike filtering by integrated RC-components.

I²C Protocol

Figure 195:
I²C Symbol Definition

Symbol	Definition	RW	Note
S	Start condition after stop	R	1-bit
Sr	Repeated start	R	1-bit
DW	Device address for write	R	0110 0000b (60 h)
DR	Device address for read	R	0110 0001b (61 h)
WA	Word address	R	8-bit
A	Acknowledge	W	1-bit
N	No Acknowledge	R	1-bit
reg_data	Register data/write	R	8-bit
data (n)	Register data/read	W	8-bit
P	Stop condition	R	1-bit
WA++	Increment word address internally	R	During acknowledge

I²C Write Access

Byte Write and Burst Write formats are used to write data to the slave.

Figure 196:
I²C Byte Write Format

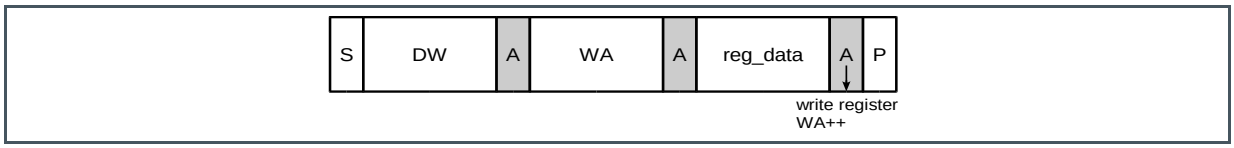
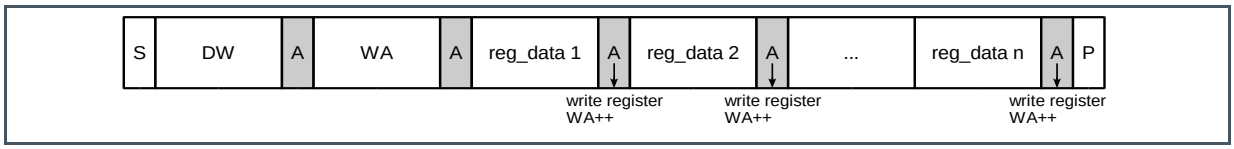


Figure 197:
I²C Burst Write Format



The transmission begins with the START condition, which is generated by the master when the bus is in an IDLE state (the bus is free). The device-write address is followed by the word address. After the word address, any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

Example of a Burst Write Access:

```
i2c_burstwrite(i2c_address, byte[0:7]);- Write 8 Byte, LSB first
```

Realization of the burst write access via single accesses:

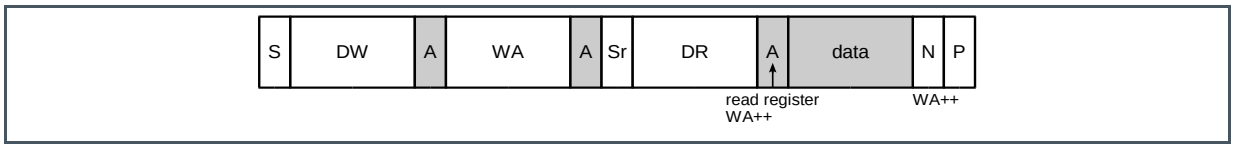
```
i2c_write(i2c_address, byte[0]);          - Write Byte 0
i2c_write(i2c_address+1, byte[1]);        - Write Byte 1
i2c_write(i2c_address+2, byte[2]);        - Write Byte 2
i2c_write(i2c_address+3, byte[3]);        - Write Byte 3
i2c_write(i2c_address+4, byte[4]);        - Write Byte 4
i2c_write(i2c_address+5, byte[5]);        - Write Byte 5
i2c_write(i2c_address+6, byte[6]);        - Write Byte 6
i2c_write(i2c_address+7, byte[7]);        - Write Byte 7
```

I²C Read

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address or, with a new transmission START followed by the device-read address - when the bus is in an IDLE state. The device-read address is always followed by the first register byte transmitted from the slave. In Read

mode, any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 198:
I²C Random Read Format



Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

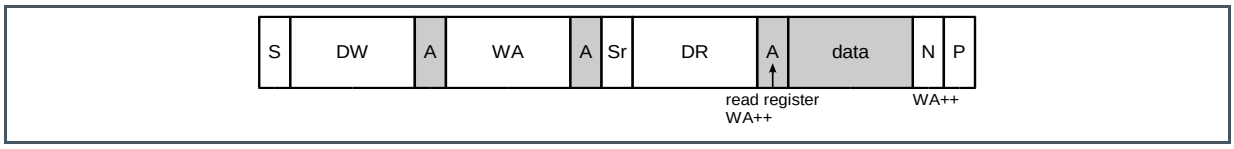
The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

To change the data direction, a repeated START condition is issued on the first SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state, the slave transmits register data, located by the previously received word address vector. The master responds to the data byte with a “not-acknowledge” and issues a STOP condition on the bus

Figure 199:
I²C Sequential Read Format

Sequential Read is the extended form of Random Read, as more than one register-data byte is subsequently transferred. In contrast to the Random Read, for a sequential read, the transferred register-data bytes are responded to with an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission, the master has to send a “not-acknowledge” following the last data byte and subsequently generate the STOP condition.

Figure 200:
I²C Current Address Read Format



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle, and the master issues a START condition, followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a “not-acknowledge” after the first register byte. Analogous to Sequential Read, an unlimited number of data bytes can be transferred - where the data bytes have to be responded to with an acknowledge from the master. For termination of the transmission, the master sends a “not-acknowledge” following the last data byte and a subsequent STOP condition.

Example of a Burst Read Access:

```
i2c_burstread(i2c_address, byte[0:7]);  - Read 8 Byte, LSB first
```

Realization of the burst read access via single accesses:

```
i2c_read(i2c_address, byte[0]);         - Read Byte 0

i2c_read(i2c_address+1, byte[1]);       - Read Byte 1

i2c_read(i2c_address+2, byte[2]);       - Read Byte 2

i2c_read(i2c_address+3, byte[3]);       - Read Byte 3

i2c_read(i2c_address+4, byte[4]);       - Read Byte 4

i2c_read(i2c_address+5, byte[5]);       - Read Byte 5

i2c_read(i2c_address+6, byte[6]);       - Read Byte 6

i2c_read(i2c_address+7, byte[7]);       - Read Byte 7
```

8 Application Information

The following figure shows the complete integration of the AS7056 in an optical measurement system for HRM, HRV, BP, and SpO_2.

8.1 Schematic

Figure 201:
AS7056 Schematics

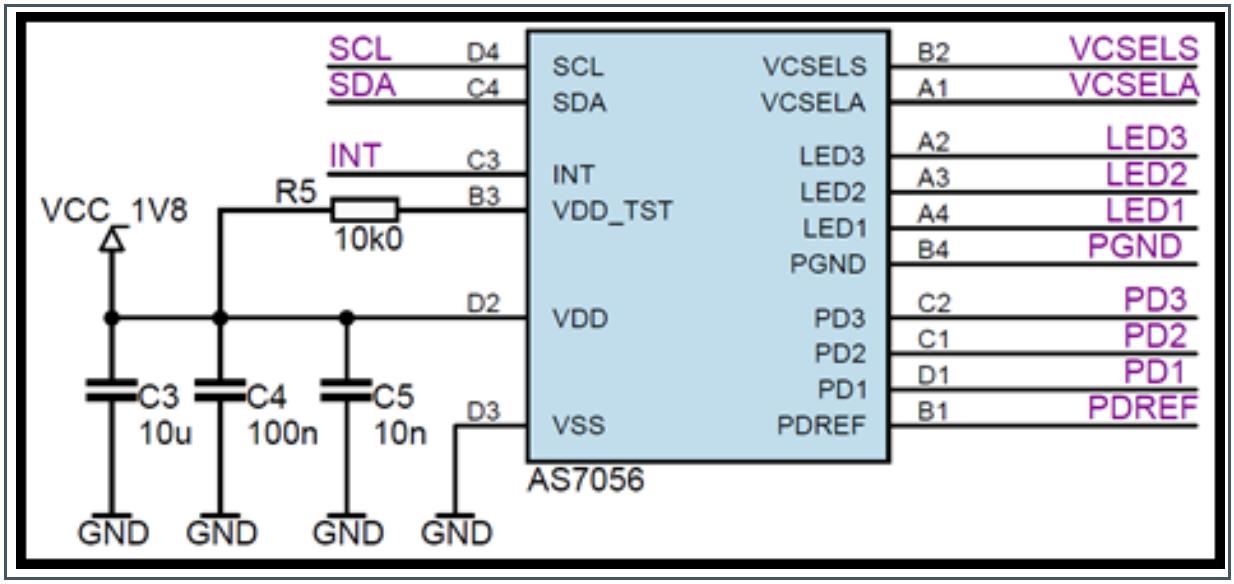


Figure 202:
LED/PD Module

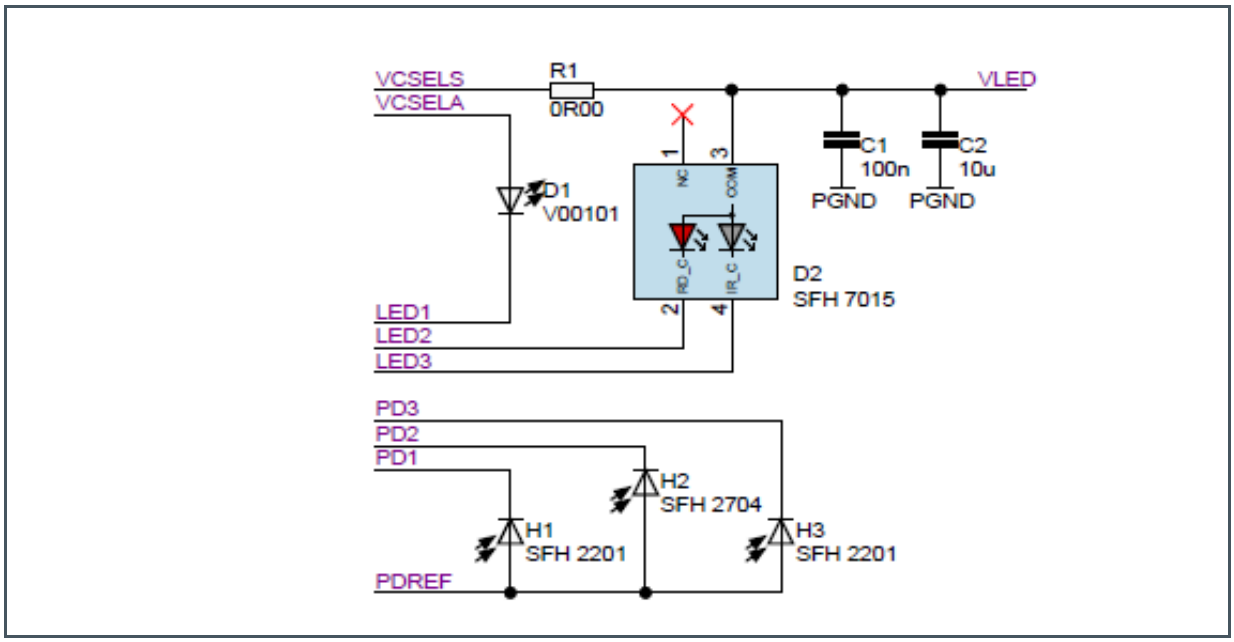


Figure 203:
Schematics MEMS Accelerometer

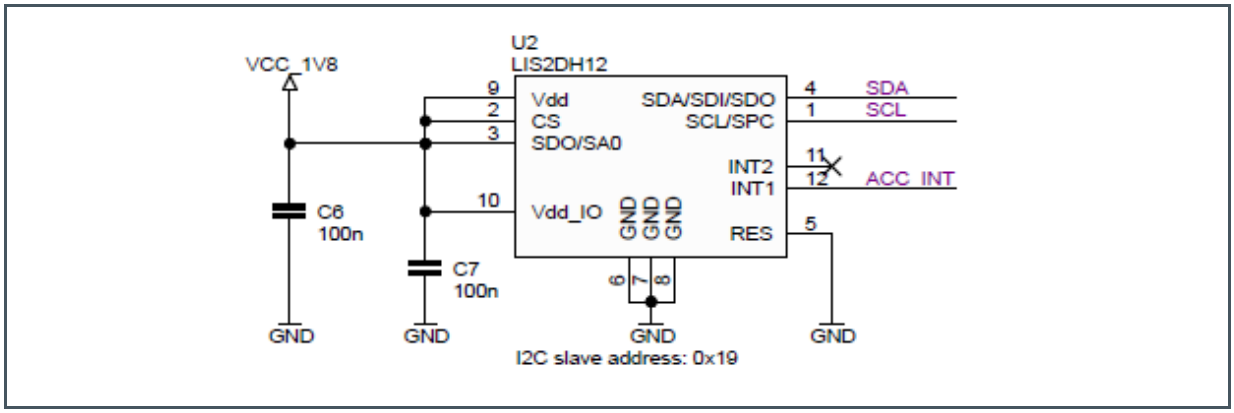


Figure 204:
Connection to MCU

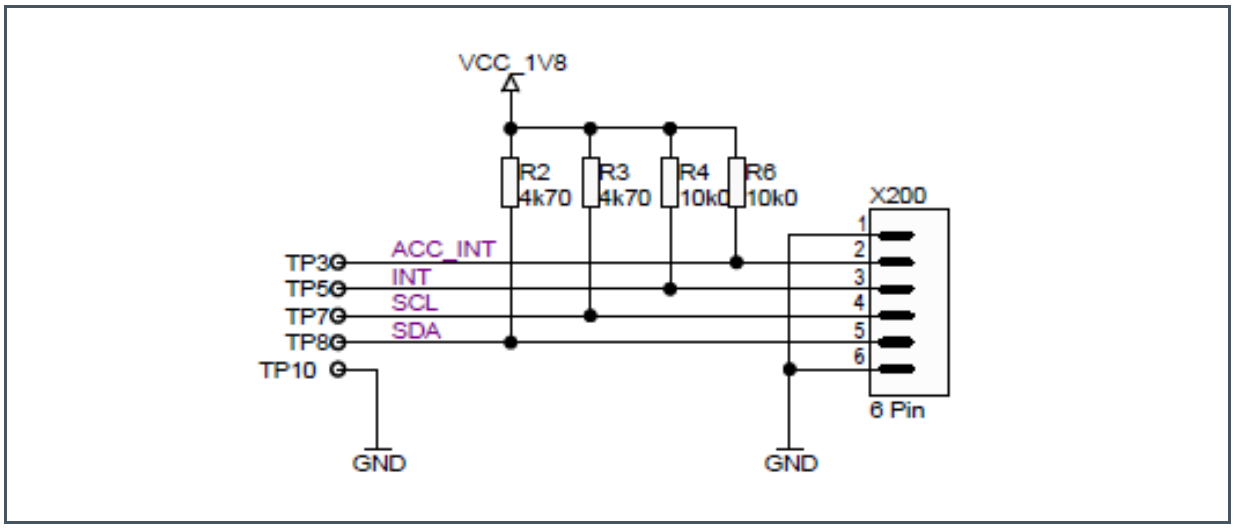
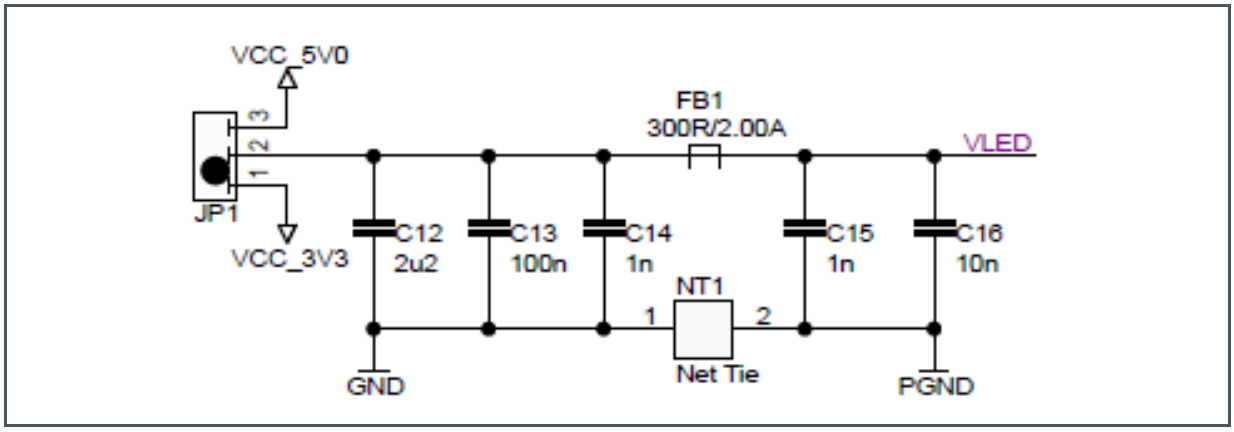
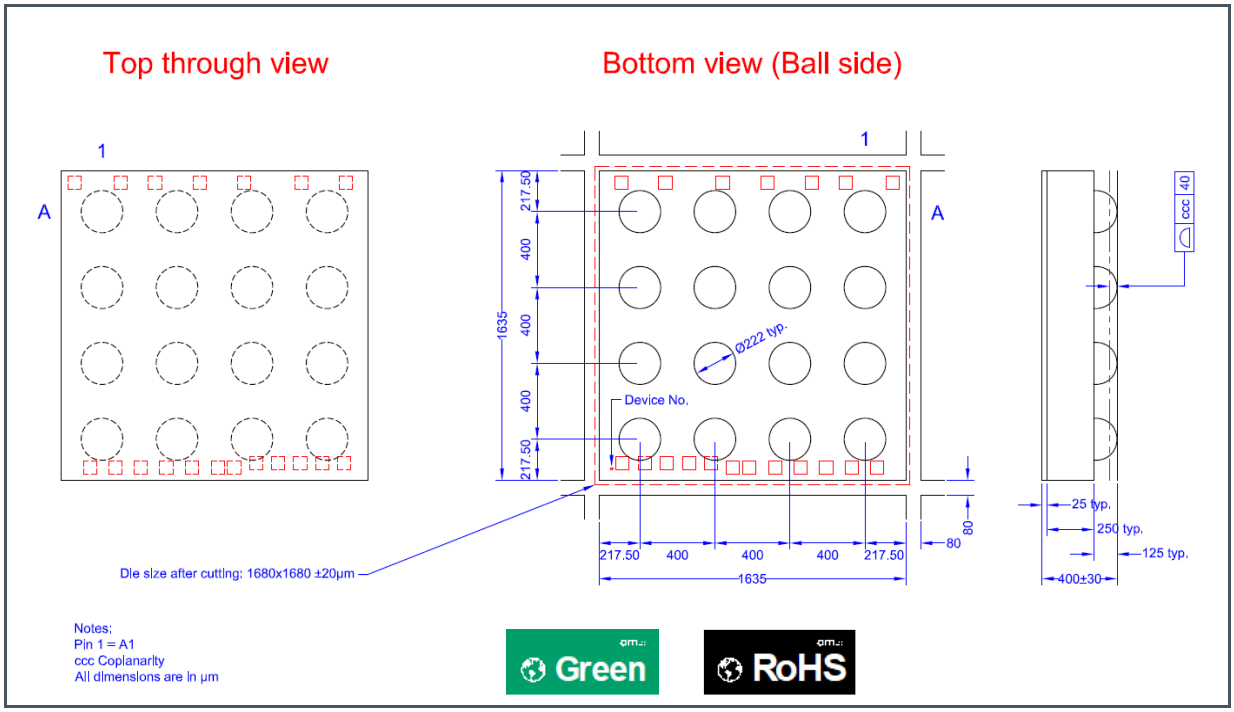


Figure 205:
Voltage Supply



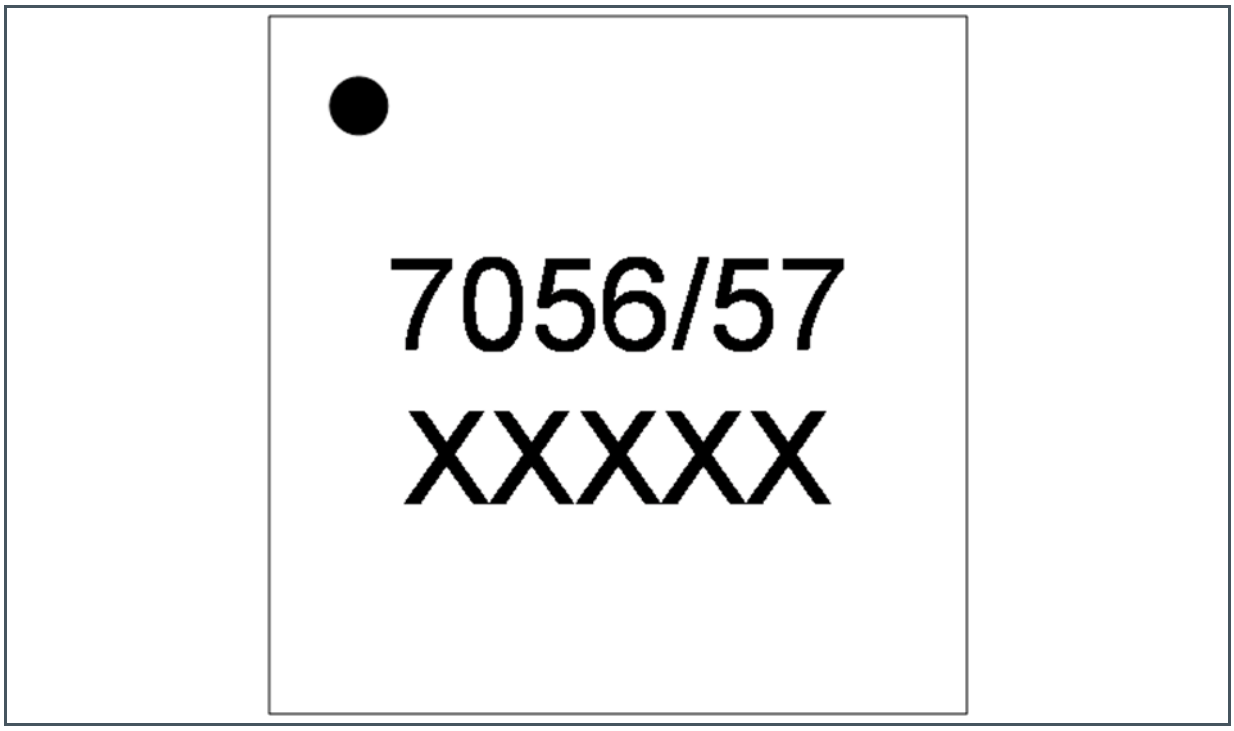
9 Package Drawings & Markings

Figure 206:
WLCSP Package Outline Drawing



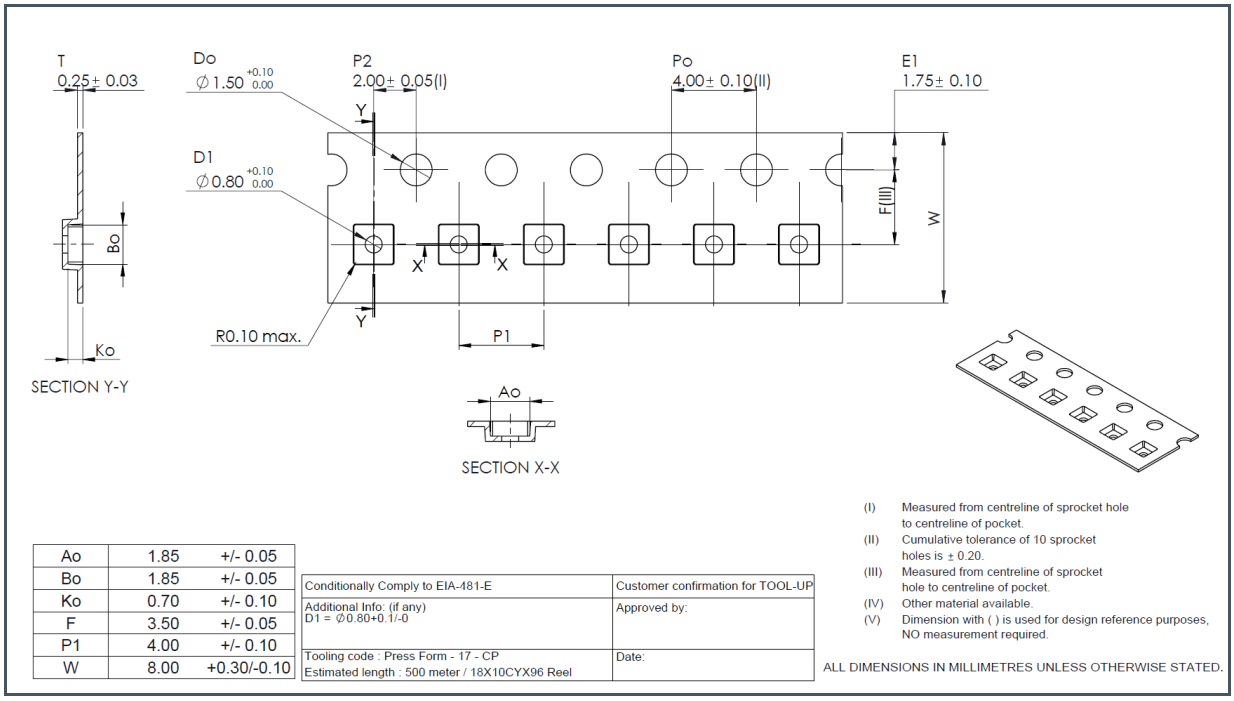
(1) All dimensions are in micrometers, angles in degrees.
(2) Dimensioning and tolerances conform to ASME Y14.5M-1994.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

Figure 207:
AS7056/57 Product Marking



10 Tape & Reel Information

Figure 208:
Tape Dimensions



Ao	1.85	+/- 0.05
Bo	1.85	+/- 0.05
Ko	0.70	+/- 0.10
F	3.50	+/- 0.05
P1	4.00	+/- 0.10
W	8.00	+0.30/-0.10

Conditionally Comply to EIA-481-E	Customer confirmation for TOOL-UP
Additional Info: (if any) D1 = ∅0.80+0.1/-0	Approved by:
Tooling code : Press Form - 17 - CP Estimated length : 500 meter / 18X10CYX96 Reel	Date:

11 Soldering & Storage Information

Figure 209:
Solder Reflow Profile Graph

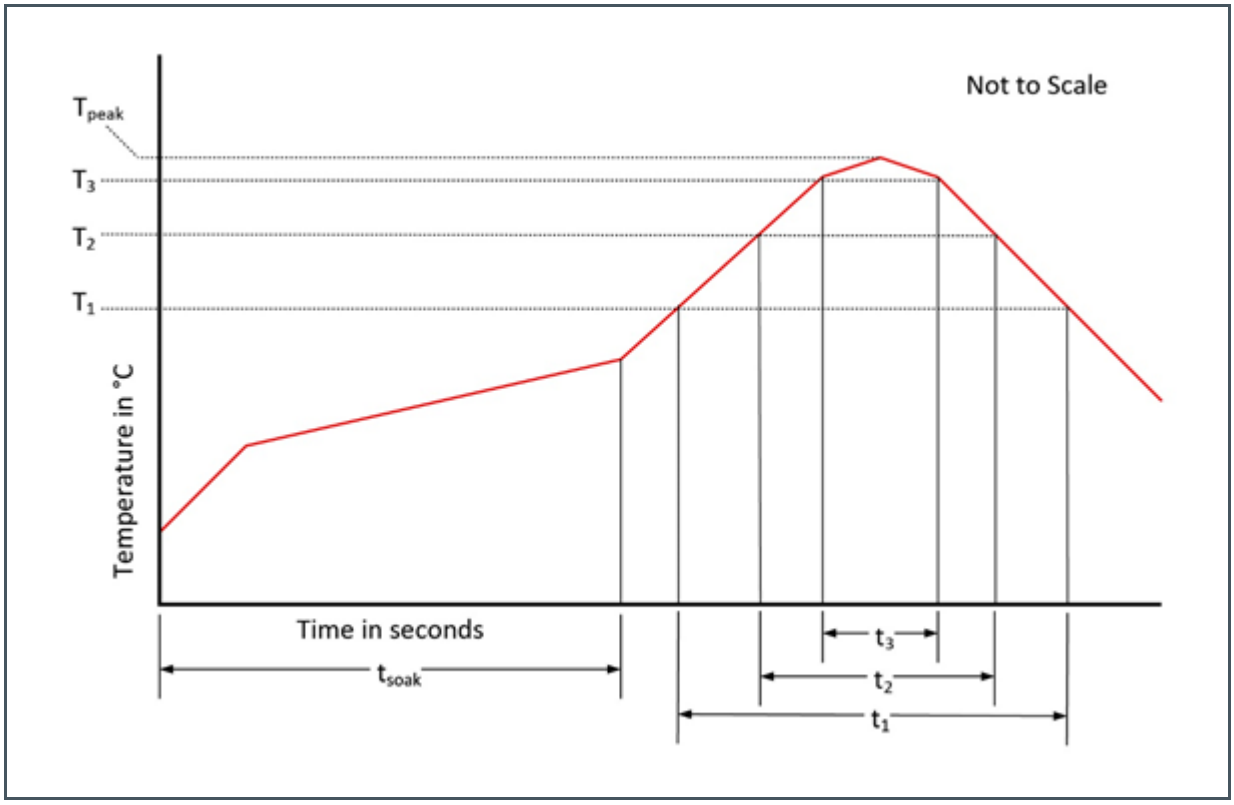


Figure 210:
Solder Reflow Profile

Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/s
Soak time	t_{soak}	2 to 3 minutes
Time above 217 °C (T1)	t_1	Max 60 s
Time above 230 °C (T2)	t_2	Max 50 s
Time above T_{peak} – 10 °C (T3)	t_3	Max 10 s
Peak temperature in reflow	T_{peak}	260 °C
Temperature gradient in cooling		Max −5 °C/s

12 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

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Changes to Figure 77	70
Changes to Figure 78	70
Changes to Figure 106	85
Addition of Figure 207	135

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

13 Legal Information

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