Power LDMOS transistor

Rev. 2 — 10 December 2020

AMPLEON Product data sheet

### 1. Product profile

### **1.1 General description**

A 10 W LDMOS driver transistor for broadcast and industrial applications. The excellent ruggedness of this device makes it ideal for digital and analog transmitter applications in the frequency range from HF to 2 GHz.

### Table 1.Typical performance

Test signal	f	V <sub>DS</sub>	PL	Gp	η <b>D</b>
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	1400	50	10	21	65
	1030 to 1090	50	11	22	63
CW	360 to 450	50	10	18	60

### **1.2 Features and benefits**

- Designed for broadband operation
- High efficiency
- Integrated dual sided ESD protection
- Excellent ruggedness
- High power gain
- Excellent reliability
- Easy power control
- Excellent stability
- For RoHS compliance see the product details on the Ampleon website

### **1.3 Applications**

- Broadcast transmitter applications
- Industrial, scientific and medical applications
- Applicable at frequencies from HF to 2 GHz

**Power LDMOS transistor** 

## 2. Pinning information

Pin	Description	Simplified outline	Graphic symbol
BLP15H9	S10 (SOT1482-1)		
1	drain		
2	gate		۲ لــــا
3	source		2 – – – – – 3 sym112
BLP15H9	S10G (SOT1483-1)		
1	drain	2	
2	gate		1 لـــا
3	source		2 – – – – – – – – – – – – – – – – – – –

[1] Connected to flange.

## 3. Ordering information

### Table 3.Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT1482-1	BLP15H9S10Z	9349 602 49515	TR13; 500-fold; 24 mm; dry pack	500
SOT1483-1	BLP15H9S10GZ	9349 603 08515	TR13; 500-fold; 24 mm; dry pack	500

### 4. Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage		-	106	V
V <sub>GS</sub>	gate-source voltage		-6	+11	V
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

### 5. Thermal characteristics

### Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
R <sub>th(j-c)</sub>	thermal resistance from junction to case	$T_{case} = 80 \text{ °C}; V_{DS} = 50 \text{ V};$ $P_{L} = 10 \text{ W}$	6.0	K/W

## 6. Characteristics

#### Table 6.DC characteristics

 $T_i = 25 \ ^{\circ}C$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; \text{ I}_{D} = 0.06 \text{ mA}$	106	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 6.4 mA	1.5	2.0	2.5	V
V <sub>GSq</sub>	gate-source quiescent voltage	V <sub>DS</sub> = 50 V; I <sub>D</sub> = 10 mA	1.5	2.0	2.5	V
I <sub>DSS</sub>	drain leakage current	$V_{GS} = 0 V; V_{DS} = 50 V$	-	-	1.4	μΑ
I <sub>DSX</sub>	drain cut-off current	$\label{eq:VGS} \begin{array}{l} V_{\mathrm{GS}} = V_{\mathrm{GS}(\mathrm{th})} + 3.75 \; V; \\ V_{\mathrm{DS}} = 10 \; V \end{array}$	-	1.1	-	A
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 11 V; V <sub>DS</sub> = 0 V	-	-	140	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 V;$ I <sub>D</sub> = 0.22 A	-	3.2	-	Ω

#### Table 7. RF characteristics

Test signal: pulsed RF;  $t_p = 100 \ \mu$ s;  $\delta = 20 \ \%$ ;  $f = 1400 \ MHz$ ; RF performance at  $V_{DS} = 50 \ V$ ;  $I_{Dq} = 10 \ mA$ ;  $T_{case} = 25 \ ^{\circ}C$ ; unless otherwise specified; in a class-AB production test circuit with Johnstech socket.

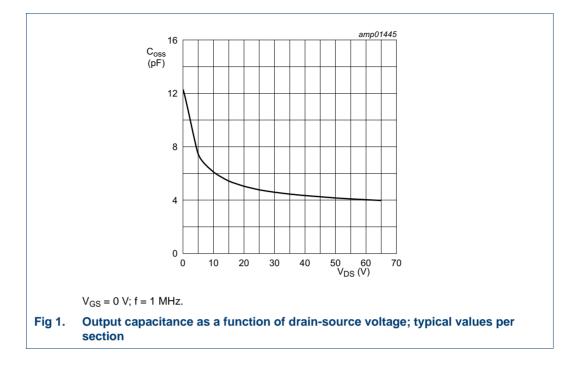
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
G <sub>p</sub>	power gain	P <sub>L</sub> = 10 W	19	21	-	dB
RL <sub>in</sub>	input return loss	P <sub>L</sub> = 10 W	-	-7	-3	dB
η <sub>D</sub>	drain efficiency	P <sub>L</sub> = 10 W	60	65	-	%

#### Table 8.AC characteristics

 $T_i = 25 \ ^{\circ}C$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C <sub>iss</sub>	input capacitance	$V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz$	-	9.8	-	pF
C <sub>oss</sub>	output capacitance	$V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz$	-	4.2	-	pF
C <sub>rss</sub>	reverse transfer capacitance	$V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz$	-	0.10	-	pF

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## 7. Test information

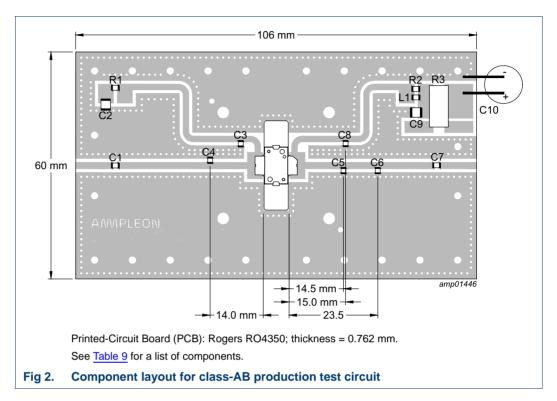
### 7.1 Ruggedness in class-AB operation

The BLP15H9S10 and BLP15H9S10G are capable of withstanding a load mismatch corresponding to VSWR = 30 : 1 through all phases under the following conditions: V<sub>DS</sub> = 55 V; I<sub>Dq</sub> = 5 mA; P<sub>L</sub> = 13 W; f = 1400 MHz; pulsed CW (t<sub>p</sub> = 100  $\mu$ s;  $\delta$  = 20 %).

BLP15H9S10\_BLP15H9S10G

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### 7.2 Test circuit

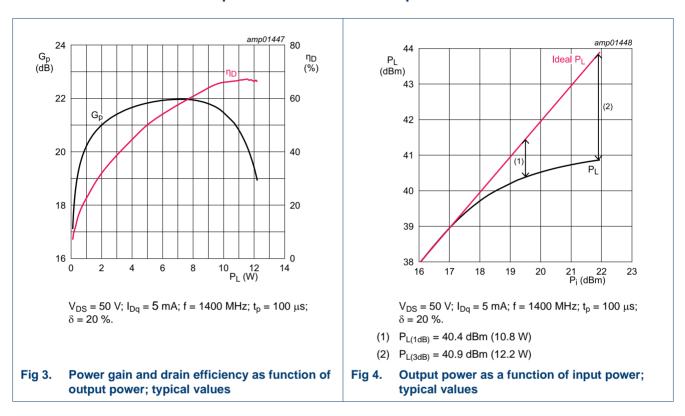


## Table 9.List of componentsFor test circuit see Figure 2.

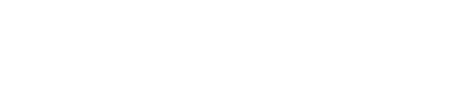
			Barriela
Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	12 pF [1]	
C2, C9	multilayer ceramic chip capacitor	4.7 μF, 100 V	
C3, C7, C8	multilayer ceramic chip capacitor	30 pF [1]	
C4	multilayer ceramic chip capacitor	5.1 pF [1]	
C5	multilayer ceramic chip capacitor	7.5 pF [1]	
C6	multilayer ceramic chip capacitor	4.3 pF [1]	
C10	electrolytic capacitor	470 μF, 64 V	
R1	chip resistor	4.7 Ω	SMD 1206
R2	chip resistor	10 Ω	SMD 1206
R3	shunt resistor	0.01 Ω	
L1	inductor	9 nH	Coilcraft: 1508-9N0GLB

[1] American Technical Ceramics type 800A or capacitor of same quality.

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### 7.3 Graphical data



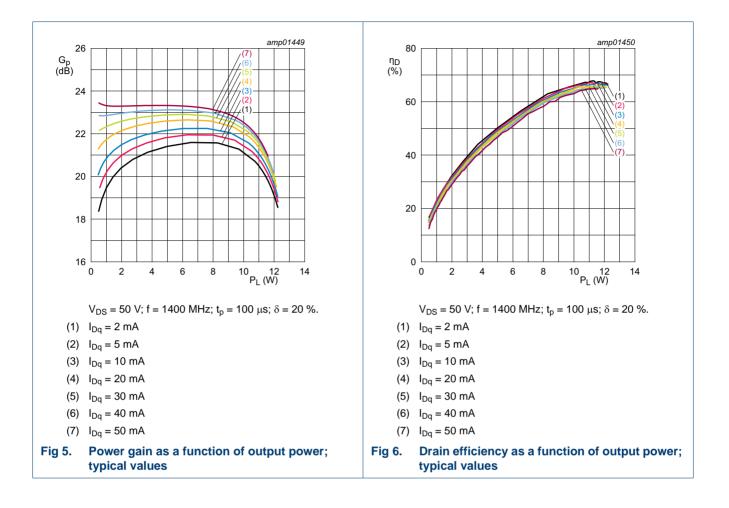
### 7.3.1 Pulsed CW performance measured in production RF test circuit

BLP15H9S10\_BLP15H9S10G

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## **BLP15H9S10; BLP15H9S10G**

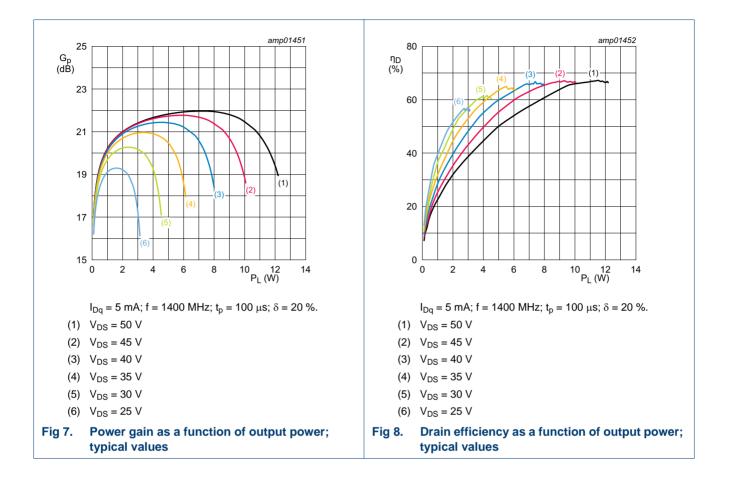
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## **BLP15H9S10; BLP15H9S10G**

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## 8. Package outline

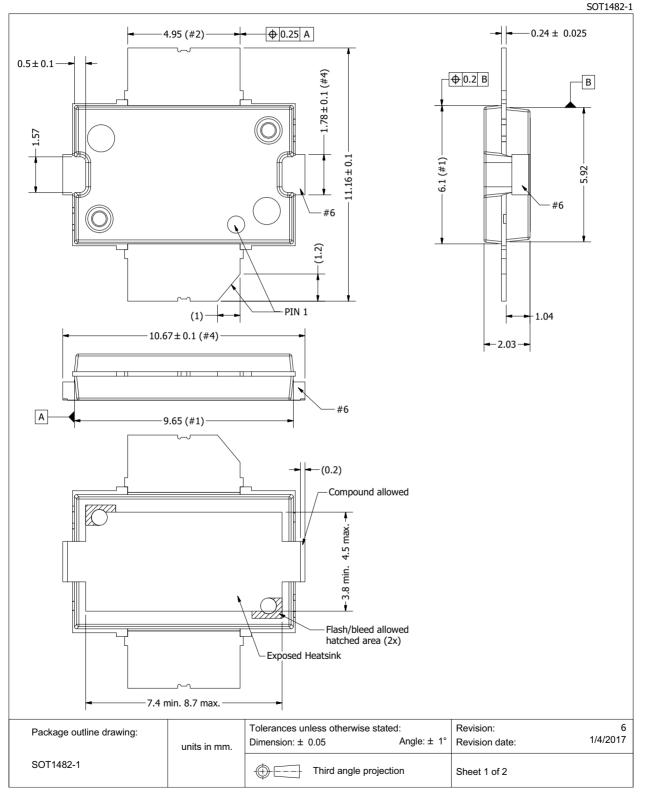


Fig 9. Package outline SOT1482-1 (sheet 1 of 2)

BLP15H9S10\_BLP15H9S10G

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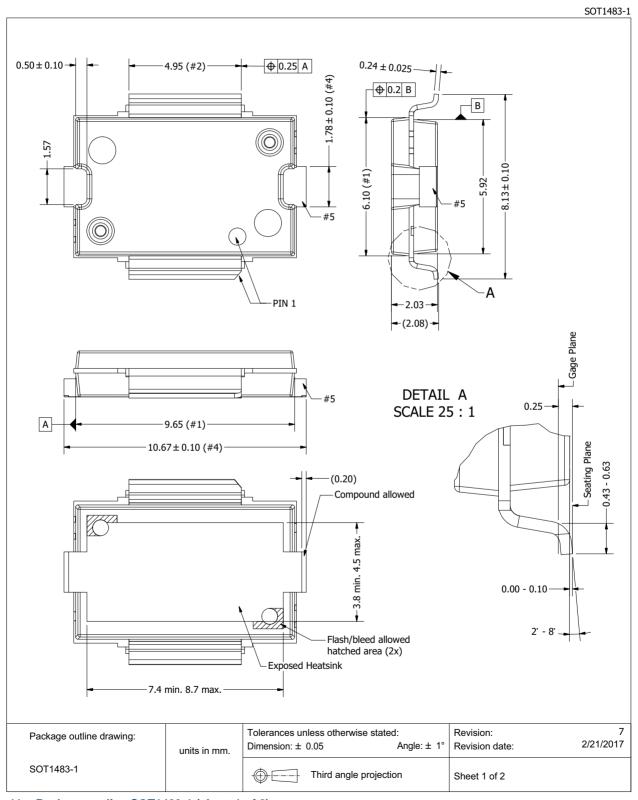
SOT1482-1

			Drawing Notes	
Items			Description	
(4)	Dimensions are exe	cluding mold protru	ision. The mold protrusion is maximum 0.15 mm p	per side. See also detail B.
(1)	In the dambar area	max. protrusion is	0.55 mm. max. in length and 0.3 mm. max. in wid	dth (4x). See also detail B.
(2)	The lead dambar (r	netal) protrusions a	are not included. Add 0.14 mm max to the total lea	ad dimension at the dambar location.
(3)	The leads and expo	osed heatsink are p	plated with matte Tin (Sn).	
(4)	Dimensions (Heats	ink ears) 10,67 and	d 1,78 do not include mouldprotrusion. Overall Ma	ax. dimensions incl. mould
(4)	protrusions is 10.92	2 mm. (max.) and 2	2.03 mm. (max.)	
(5)	Lead coplanarity ov	ver the leads is 0,1	mm. maximum.	
(6)	Surfaces may rema	ain unplated (not so	olderable surfaces)	
	TPA 1			
	B	Lead Dan	(0.3 max.)	DETAIL B SCALE 50 : 1
Package o	utline drawing:	Lead Dan	(D;55 max)	SCALE 50 : 1

#### Fig 10. Package outline SOT1482-1 (sheet 2 of 2)

BLP15H9S10\_BLP15H9S10G

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### Fig 11. Package outline SOT1483-1 (sheet 1 of 2)

BLP15H9S10\_BLP15H9S10G

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SOT1483-1

			<b>—</b> •	
Items			Description	
(1)		•	ision. The mold protrusion is maximum 0.15 mm	
			0.55mm max. in lenght and 0.3 mm max. in wid	
(2)			are not included. Add 0.14 mm max to the total le	ead dimension at the dambar location.
(3)			plated with matte Tin (Sn).	
(4)	, i i i i i i i i i i i i i i i i i i i	, ,	d 1,78 do not include mouldprotrusion. Overall M	ax. dimensions incl. mould
	protrusions is 10,92 n			
(5)	Surfaces may remain	unplated (not so	olderable surfaces).	
B-			(0.3 max.)	DETAIL B SCALE 50 : 1
	utline drawing:			SCALE 50 : 1

#### Fig 12. Package outline SOT1483-1 (sheet 2 of 2)

BLP15H9S10\_BLP15H9S10G

## 9. Handling information

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

#### Table 10.ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2B [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1C [2]

 $\label{eq:constraint} \begin{tabular}{ll} [1] & CDM \ classification \ C2B \ is granted to any part that passes after exposure to an ESD pulse of 750 \ V. \end{tabular}$ 

[2] HBM classification 1C is granted to any part that passes after exposure to an ESD pulse of 1000 V.

### **10. Abbreviations**

Table 11. Abbreviations			
Acronym	Description		
CW	Continuous Wave		
ESD	ElectroStatic Discharge		
HF	High Frequency		
LDMOS	Laterally Diffused Metal-Oxide Semiconductor		
MTF	Median Time to Failure		
RoHS	Restriction of Hazardous Substances		
SMD	Surface Mounted Device		
VSWR	Voltage Standing Wave Ratio		

## 11. Revision history

#### Table 12.Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP15H9S10_BLP15H9S10G v.2	20201210	Product data sheet	-	BLP15H9S10_BLP15H9S10G v.1
Modifications:	<u>Section 1.1 on page 1</u> : changed 1500 MHz to 2 GHz in first paragraph			
	• Table 1 on	page 1: updated tab	le	
	<ul> <li>Section 1.3 on page 1: changed 1500 MHz to 2 GHz</li> </ul>			
BLP15H9S10_BLP15H9S10G v.1	20200929	Product data sheet	-	-

## 12. Legal information

#### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions"

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