ADVANCE INFORMATION

Am386® EM

386-Based, 80C186/8-Compatible, 32-Bit Embedded Microcontroller

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **E86™ Family embedded microcontroller offering a 32-bit upgrade for 80C186/8 designs**
- **32-bit Am386 CPU core provides more address space and faster instruction execution.**
  - — 96-Mbyte maximum system memory address space
  - — Industry standard 386 instruction set
  - — 3.3 V or 5.0 V operation
  - — Fully static design
  - — 25-, 33-, and 40-MHz operating frequencies
- **Demultiplexed address/data bus design provides faster memory access along with 80C186/8 compatibility.**
  - — System bus design incorporates a 24-bit demultiplexed address bus, in addition to the 80C186/8-compatible 16-bit address/data bus. Both nonmultiplexed and 80C186-style multiplexed address and data cycles are supported.
- **Glueless interfaces and Design-Made-Easy™ solutions provide faster time-to-market and reduced system cost.**
  - — Comprehensive set of integrated peripherals on-chip eliminates the need for external glue logic and additional chip sets.
  - — Glueless DRAM, Flash, SRAM, and ROM interface
  - — Seven peripheral chip-select signals with programmable wait states
  - — Glueless connection to commonly used peripherals including Am85C30, Am53CF94, Am79C30A, Am79C940, PCNET32, and 16C30
- **80C186/8-compatible on-chip peripherals provide an easy upgrade path for greater performance.**
  - — Four enhanced DMA channels support fly-by transfers and chaining.
  - — Enhanced interrupt controller (up to 16 levels of priority) with cascade lines for additional 82C59 interface
  - — Three counter/timers with controls and outputs for two channels available for external system use
- **Additional on-chip peripherals enable increased functionality at lower system cost.**
  - — Fully integrated DRAM and Flash/SRAM/ROM controllers support six programmable memory device regions (up to four banks of which can be DRAM) in either an 8- or 16-bit configuration.
  - — 12-stage programmable watchdog timer with software reset
  - — Dual 8051-compatible serial ports for asynchronous and byte synchronous communication
  - — Up to 32 general-purpose peripheral I/O ports
- **Low-cost debug interface**
  - — Full system access via JTAG and tool support for integrated debugging
- **Widely available native development tools, applications, and system software**
  - — Microsoft At Work™, Novell NEST

GENERAL DESCRIPTION

The Am386EM microcontroller is an E86 Family microcontroller that offers a powerful 32-bit upgrade for 80C186/8 designs requiring additional address space, a glueless system design, and enhanced peripherals. Developed specifically for the embedded marketplace, the fully integrated Am386EM microcontroller delivers the benefits of the Am386 microprocessor architecture at a microcontroller cost structure.

The Am386EM microcontroller integrates the functions of CPU, memory and peripheral controller, watchdog timer, interrupt controller, DMA controller, dual serial ports, and integrated debugging support on one chip. Based on the Am386 processor, the Am386EM microcontroller allows designers to reduce the size, power consumption, and cost of embedded systems while increasing functionality and performance.

The Am386EM microcontroller is part of AMD's E86 Family of embedded microcontrollers and microprocessors based on the x86 architecture. The E86 Family includes the 80C186, 80C188, 80L186, 80L188,

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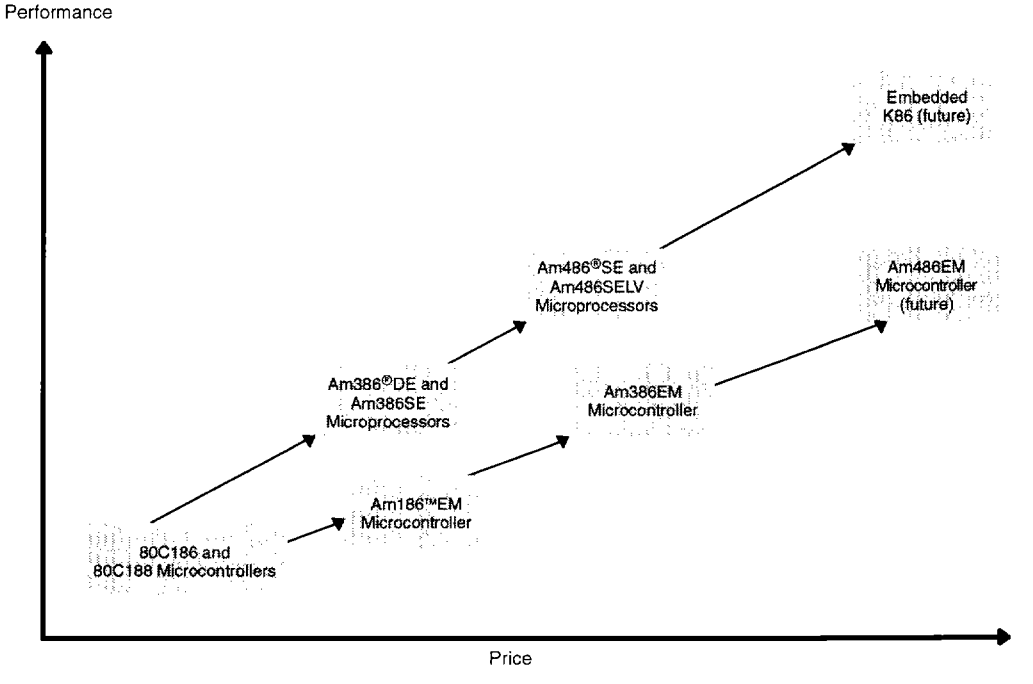
Am186™EM, and Am386EM microcontrollers; and the Am386SE, Am386DE, Am486®SE, and Am486SELV microprocessors.

The Am386EM microcontroller has been designed to meet the most common requirements of embedded products used in the office automation, mass storage, and general embedded markets. Specific applications include products using the Microsoft At Work operating system, faxes, terminals, printers, copiers, feature phones, switching, modems, base stations, digital line cards, shelf controllers, disk drives, and industrial control, among others.

The Am386EM microcontroller is available in a 132-lead plastic quad flat pack (PQFP) package.



The E86™ Family of Embedded Microprocessors and Microcontrollers

RELATED AMD PRODUCTS

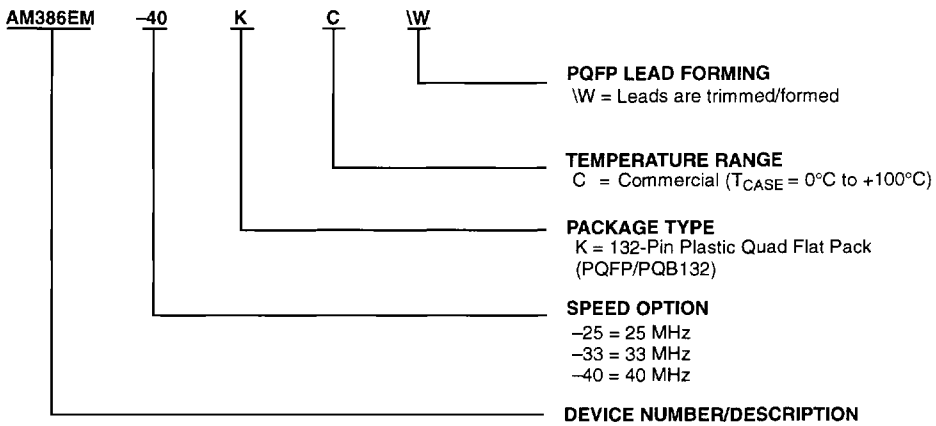
E86 Family Devices

Device	Description
80C186	16-bit microcontroller
80C188	16-bit microcontroller with 8-bit external data bus
80L186	Low-voltage, 16-bit microcontroller
80L188	Low-voltage, 16-bit microcontroller with 8-bit external data bus
Am186™EM	High-performance, 80C186/8-compatible, 16-bit embedded microcontroller
Am386®EM	386-based, 80C186/8-compatible, 32-bit embedded microcontroller
Am386®DE	High-performance, 32-bit embedded microprocessor
Am386®SE	High-performance, 32-bit embedded microprocessor with 16-bit external data bus
Am486®SE	High-performance, 32-bit embedded microprocessor
Am486®SELV	High-performance, low-voltage 32-bit embedded microprocessor

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the elements below.



Valid Combinations	
AM386EM–25 AM386EM–33 AM386EM–40	KC\W

Valid Combinations

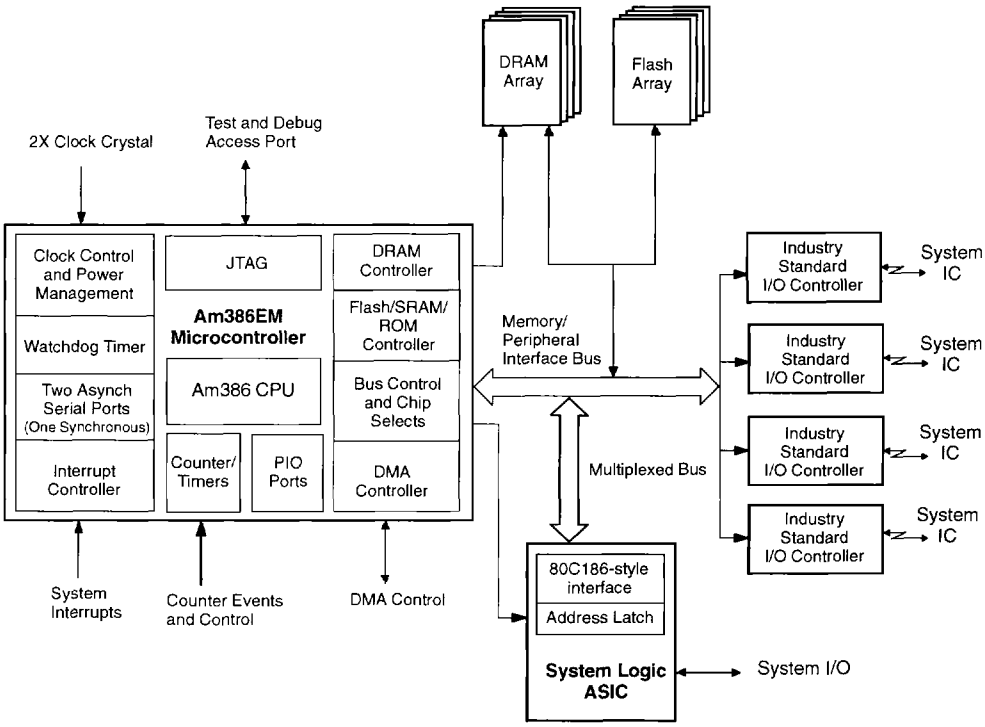
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

THIRD-PARTY DEVELOPMENT SUPPORT PRODUCTS

AMD's FusionE86SM Program of Partnerships for Application Solutions provides the customer with an array of products designed to meet critical time-to-market needs. Products and solutions available from the AMD FusionE86 partners include emulators, hardware and software debuggers, board-level products, and software development tools, among others.

In addition, a variety of mature development tools and applications for the Am386 CPU is widely available in the general marketplace.

SYSTEM BLOCK DIAGRAM

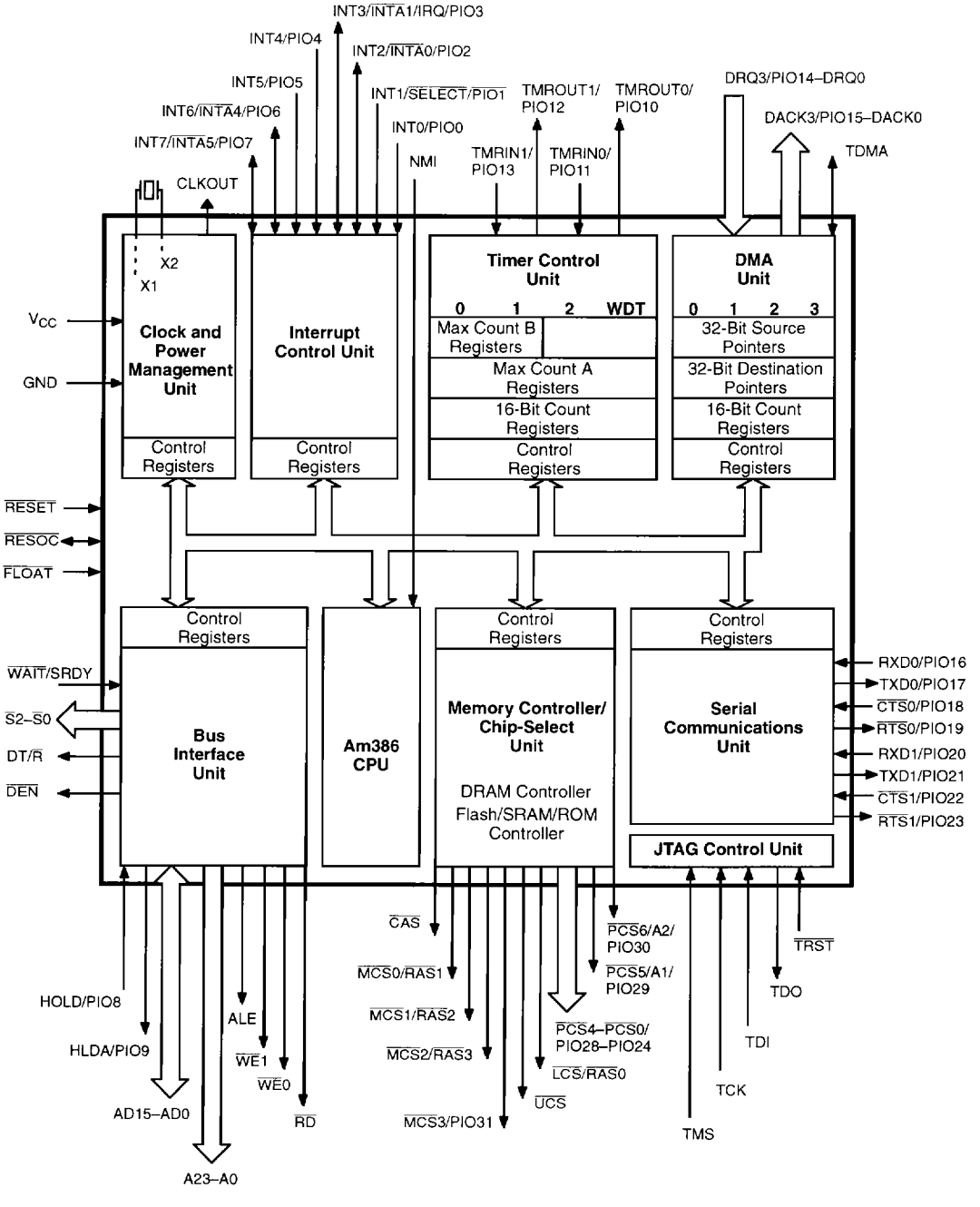


KEY FEATURES AND BENEFITS

The Am386EM microcontroller extends AMD's line of microcontrollers based on the industry-standard x86 architecture, providing powerful performance upgrades that can easily extend an 80C186/8-based product into a complete family of products. With the Am386EM microcontroller, the product designer can choose from among several different design strategies to reach variable price and performance goals.

- Upgrading to minimize total system cost—The Am386EM microcontroller connects to system memory and peripherals with a minimum of external logic.
- Upgrading for enhanced performance—For designers who want to overcome the architectural limitations of traditional 80C186/8 microcontrollers, the 32-bit Am386 CPU core of the Am386EM microcontroller offers higher performance, and the 96-Mbyte address space of the Am386EM microcontroller overcomes the 1-Mbyte limit of the 80C186/8. The nonmultiplexed memory bus offers faster, unbuffered access to memory.
- Upgrading for enhanced functionality—The new and enhanced on-chip peripherals of the Am386EM microcontroller include a DRAM controller and a watchdog timer, along with additional interrupts, DMA channels, serial ports, and chip selects.

INTERNAL BLOCK DIAGRAM



Bus Interface

The bus interface controls all cycles to external peripherals and memory devices. External cycle types include those to DRAM, SRAM, and Flash memory devices as well as memory and I/O mapped peripherals. The bus interface supports the following features:

- Both multiplexed (80C186-style) and nonmultiplexed memory and I/O cycles
- Multiplexed row and column addresses for DRAM devices
- 8- and 16-bit cycles
- CPU-initiated and DMA-controller-initiated cycles
- Multiple cycles to complete 32-bit and unaligned 16-bit accesses
- Bus arbitration for external masters

The Am386EM microcontroller provides maximum flexibility by allowing multiplexed and nonmultiplexed bus operation. When the processor initiates a cycle to an address that is mapped to a peripheral device designated as a multiplexed device, the bus interface unit performs a 80C186-style bus cycle. For nonmultiplexed bus cycles, an external 24-bit nonmultiplexed address bus A23–A0 is provided to directly address memory elements within each bank, allowing a 16-Mbyte maximum bank size.

Glueless Interfacing

The Am386EM microcontroller has been designed to connect to system memory and peripherals with a minimum of required external logic. To this end the DRAM and Flash interfaces are glueless, deriving multiplexed as well as nonmultiplexed addresses from the system address bus. All chip-select, status, and control information for peripheral and memory device cycles is generated directly by the Am386EM microcontroller.

On-Chip Memory and Peripheral Control

The Am386EM microcontroller provides a glueless high performance 8- or 16-bit data path to DRAM, SRAM, and Flash/ROM memory devices as well as 80C186-style multiplexed and nonmultiplexed peripheral devices.

The memory control unit includes a DRAM controller and a Flash/SRAM/ROM controller. Six memory device regions are provided, each programmable to support DRAM, Flash, SRAM, or ROM devices, which are mapped into the processor's memory address space. Each memory bank has a unique configuration register set allowing individual settings for parameters such as memory type, size and timing requirements.

DRAM Controller

The processor provides a glueless interface to DRAM devices by automatically generating the row and column addresses with the required row-address strobe (RAS) and column-address strobe (CAS) control signals. This feature eliminates the need for external multiplexing and timing controllers. All industry standard DRAM configurations are supported, including symmetrical and asymmetrical addressing modes. The DRAM controller includes the following features:

- Bank sizes of 512 Kbyte, 1 Mbyte, 2 Mbyte, 4 Mbyte, 8 Mbyte, and 16 Mbyte are supported.
- DRAM bank size and starting address are programmed on a per-bank basis.
- 8- or 16-bit interface to CPU
- Page-mode (CAS only) access with programmable page size
- CAS before RAS refresh cycles
- Individual refresh period per bank
- Support for firmware DRAM bank auto-sizing
- Write-protect mode with interrupt generation on write-fault

The DRAM configuration registers provide programmable timing parameters for each phase of the DRAM access as well as the DRAM refresh interval. This direct interface for a wide variety of DRAM devices at all processor speeds provides maximum flexibility for the product designer.

Flash/SRAM/ROM Controller

The Flash/SRAM/ROM controller provides glueless support for standard Flash/SRAM/ROM devices. It includes the following features:

- Direct interface to memory devices
- Support for 8- or 16-bit Flash, SRAM, and ROM devices
- Maximum of six banks of up to 16Mbyte size
- Programmable wait-state timing per bank
- Write-protect mode with interrupt generation on write-fault

The memory control unit supports configuration parameters for ROM/Flash read-only memories as well as static ram (SRAM) devices. For these devices, the processor provides a decoded chip-select signal, the address of the required memory element within the device, and the appropriate read or write strobe control signal. Individual timing parameters are provided to allow interface to varying access speed memory devices. A programmable number of CPU wait states can be specified to lengthen the read or write cycle.

Peripheral Chip-Select Controller

The 80C186-compatible peripheral chip-select controller provides a direct interface for up to seven peripheral devices. The peripheral controller supports the following features:

- Direct interface to multiplexed or nonmultiplexed devices up to 16 Mbyte in size
- 8- or 16- bit peripheral devices
- Maximum of seven banks
- Programmable wait-state and device-ready timing parameters
- Programmable command-delay and command-recovery parameters
- Write-protect mode with interrupt generation on write-fault

Both multiplexed and nonmultiplexed device types are supported with programmable wait-state and device-ready parameters. In multiplexed address mode, an 80C186-type multiplexed scheme using the A23–A16, AD15–AD0, and ALE signals is used to present the peripheral address to the external device. In nonmultiplexed mode, the A23–A0 signals are used to present the peripheral address directly to the external device. In both cases, a decode chip-select signal as well as read and write strobe signals are provided. A configuration parameter is provided to specify the number of CPU wait cycles to insert for peripheral read and write operations.

Programmable command-delay and command-recovery parameters allow flexible device interface characteristics. The command-delay parameter specifies the number of clock cycles after an access to a peripheral that the CPU will wait before proceeding. The command-recovery parameter is used for devices that require a minimum amount of time between CPU accesses. The peripheral chip-select controller ensures that the specified number of device-recovery cycles has elapsed before allowing the CPU to proceed with another device access. Both the command-delay and the command-recovery parameters are active during DMA as well as CPU-initiated cycles.

Enhanced DMA Support

The Am386EM microcontroller DMA controller is a four channel, 32-bit extension of the 80C186 DMA controller. It has been expanded to address the full Am386EM microcontroller address space. The DMA controller provides high-speed data interchange between processor memory contents and external peripherals. The controller supports all combinations of memory and I/O transfers in flow-through mode, as well as direct transfers between memory and I/O devices in fly-by mode.

The DMA controller includes the following features:

- Flow-through transfers simplify peripheral design
- Fly-by transfers for increased performance
- DMA supported over entire CPU memory and peripheral address ranges
- Two-stage queued operation
- Round robin arbitration or scalable four-level DMA/CPU priority scheme
- Flexible DMA request synchronization
- Programmable DMA request signal sense (edge/level modes)
- Transfer termination based upon count or signal from peripheral

Two types of transfer modes are supported: flow-through mode and fly-by mode. In flow-through mode, each transfer consists of a separate read and write cycle. This allows both the source and destination devices to be accessed using their programmed memory type, timing, bus size, and chip select information. Flow-through transfers can specify either processor memory or an I/O device as the source or destination address. Memory-to-memory, memory-to-I/O, I/O-to-memory, and I/O-to-I/O transfers are allowed. Both 8- and 16-bit transactions are supported.

Fly-by DMA transfers are supported to increase performance by directly transferring data between processor memory and an external device in a single access cycle. In this mode, only transfers between memory and external I/O devices that share the same data width are supported. Fly-by mode DMA cycles can be extended by using the $\overline{\text{WAIT}}$ input signal. The TDMA signal is active during fly-by DMA operation and can be used to terminate the transfer.

Each DMA channel has a two-entry queue of count, source, and destination address registers. The queued reload feature relaxes the response time requirement for software to initialize a new transfer and increases DMA throughput.

Each DMA control register contains a priority field that can be used to specify service priority of a DMA channel relative to the other channels within the processor. Four levels of priority are provided. This field is used to resolve simultaneous service requests from multiple channels.

Three synchronization modes are provided to allow flexibility when interfacing to external peripherals.

Each DMA channel can also be programmed to use the output of one of the internal timer devices as the DMA transfer request signal. In this mode, the DMA transfers occur periodically at the rate specified in the timer counter

register. All DMA source and destination modes are supported when the timer is used in this manner.

Enhanced Interrupt Handling

The interrupt controller provided on the Am386EM microcontroller is a superset of the 80C186/8 interrupt controller. Sixteen priority levels are provided. The programmer's model has been structured to provide a familiar and easy upgrade path for 80C186/8 users. It includes the following features:

- 16-level priority controller
- Programmable interrupt modes
- Individual request mask capability
- Cascade interrupt functions with external 82C59A devices

The interrupt controller accepts requests from peripherals, resolves priority on pending interrupts and interrupts in service, issues interrupt requests to the processor, and provides interrupt vectors for interrupt service routines.

The interrupt controller can operate in a master or a slave mode. The master mode can be used standalone without 82C59A interrupt controllers, or with slave 82C59A devices. In slave mode, the interrupt controller acts as a slave to an external 82C59A master.

Dual Serial Ports

The Am386EM microcontroller includes two independent 8051-compatible serial ports. Each serial port includes the following features:

- Full-duplex asynchronous operation
- Half-duplex synchronous operation
- Programmable seven, eight, or nine data bits
- Programmable odd, even, or no parity
- Clear-to-Send (CTS) and Request-to-Send (RTS) functions.
- Programmable baud rate generator

Several industry-standard asynchronous communications protocols are supported on the Am386EM microcontroller. Asynchronous transmission and reception are double-buffered and can occur simultaneously. Each port can transmit and receive seven, eight, or nine data bits. The last data bit can be replaced by an odd or even parity bit. Each port can transmit and detect break characters, and both framing and overrun errors can be detected. Interrupt service is supported for both transmission and reception.

One of the serial ports also supports a byte synchronous mode of operation. This mode is half-duplex, with the transmitted and received data multiplexed through the same I/O pin. The synchronous baud clock can originate from either the internal baud rate generator or from an external source. When the internal baud rate generator is chosen, the baud clock is output through an I/O pin.

The synchronous protocol is a simple eight-bit communications mode suitable for connection to external shift register interface devices.

Programmable Timers

The Am386EM microcontroller includes a two-stage programmable watchdog timer that can provide system interrupts and reset conditions. The watchdog timer includes the following features:

- Timer clock sourced from CLKOUT
- Two-stage operation
- Programmable count
- Timer is reloaded on key data write to ensure proper operation

The watchdog timer resets the chip upon reaching a preprogrammed time interval. It operates independently of the other timers and allows reliable recovery from a software malfunction. The watchdog timer in enabled following any reset. The system software must setup the watchdog timer before the counter reaches zero. During the setup period, the timeout interval can be programmed, or the watchdog timer can be disabled. This timer can be programmed to provide one- or two-stage operation. In one-stage operation the timer resets the CPU upon countdown. In two-stage operation, the NMI signal is asserted on the first countdown and a reset sequence occurs on the second countdown.

The Am386EM microcontroller also provides three internal, 80C186/8-compatible, 16-bit programmable timers. Two of these are highly flexible and are connected to four external pins (two per timer). They can be used to count external events, time external events, and generate nonrepetitive waveforms. The third timer is not connected to any external pins and is useful for real-time coding and time delay applications. In addition, the third timer can be used as a prescaler to the other two, or as a DMA request source.

Input/Output Ports

Thirty-two PIO (Port Input/Output) pins on the Am386EM microcontroller allow unused peripheral pins to be used as general-purpose I/O ports. Four PIO control registers control whether the designated pin functions as a peripheral pin or as a PIO pin and whether each designated PIO pin functions as an input or output.

Power Management

The Am386EM microcontroller provides three power management functions:

- Power Save (Clock divide) Mode
- Idle Mode (Frozen CPU, active peripherals)
- Power Down Mode (Total shutdown)

In Power Save mode, operation of both the CPU and the peripherals continue at a lower rate. Timer and DRAM refresh intervals must be reprogrammed to compensate for the slower clock rate.

In Idle Mode, the clocks to the CPU and bus interface are disabled. All other clocks, including CLKOUT, run normally. Reset, NMI, or any unmasked interrupt returns the processor to Active Mode.

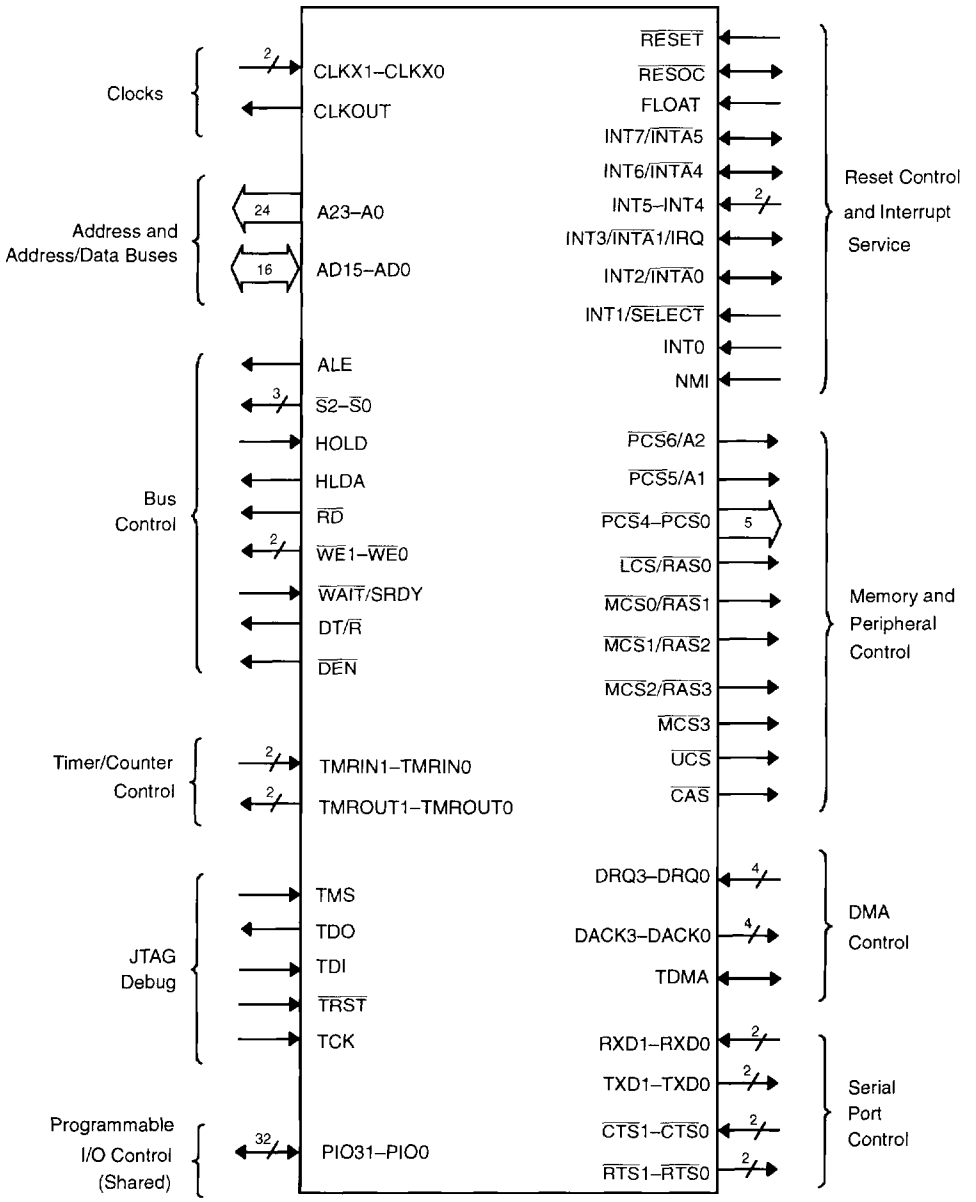
Power Down Mode disables all internal clocking except the crystal oscillator, which continues to run. This mode shuts down the entire system. The internal state of the device is maintained, and DRAM refresh is halted. An NMI or reset returns the processor to active mode.

Debug Support

An IEEE Standard 1149.1-1990 (JTAG) compliant test access port and hardware debug tool provides the basic JTAG boundary scan functions for testing processor and system hardware in a production environment. It also includes extensions that allow a hardware-development system to control and observe the processor without interposing hardware between the processor and system.

The hardware debug tool provides access to the internal address and data buses of the Am386EM microcontroller. The hardware debug tool is capable of generating all of the bus cycle types available to the CPU and monitoring certain internal signals.

LOGIC SYMBOL



Am386EM Microcontroller

PIN DESCRIPTIONS

A23–A0

System Address Bus (Outputs)

The A23–A0 outputs are the nonmultiplexed address lines for Flash, SRAM, ROM, and memory mapped peripheral access. During DRAM accesses, the A11–A0 signals also output multiplexed row (RAS) and column (CAS) addresses.

AD15–AD0

System-Multiplexed Address/Data Bus (Inputs/Outputs)

The AD15–AD0 signals are the system-multiplexed address and data bus for 80C186 multiplexed peripheral accesses. These signals also provide nonmultiplexed data for transfers to memory or I/O regions defined as nonmultiplexed.

ALE

Address Latch Enable (Output)

This output is used for external address latching during multiplexed accesses.

$\overline{\text{CAS}}$

Column Address Strobe (Output)

This Active Low output is the DRAM column address strobe.

CLKOUT

Clock Output (Output)

This Active Low clock output is driven at the external bus speed. All interface signals are synchronous to this clock.

$\overline{\text{CTS}}$1/PIO22, $\overline{\text{CTS}}$0/PIO18

Serial Port Clear-to-Send [Programmable I/O] (Inputs)

These Active Low signals control when Serial Ports 1 and 0 begin transmitting. The CTS pins are level-sensitive. They can also be configured as programmable I/O pins.

DACK3/PIO15–DACK0

DMA Acknowledge [Programmable I/O] (Outputs)

The DACK signals can be used by the processor to acknowledge an external transfer on a DMA channel. There is an individual DACK output signal for each DREQ input signal used by the processor. When configured for operation, the DACKn signal is asserted by the processor during a read or write cycle to an external peripheral. The DACKn signal can also be used to select a data transfer operation of an external device in place of an address decoded chip select. The DACK3 pin can also be configured as a programmable I/O pin.

$\overline{\text{DEN}}$

Data Enable (Output)

This Active Low output is used to enable access to devices placed on an extended (buffered) bus.

DRQ3/PIO14–DRQ0

DMA Requests [Programmable I/O] (Inputs)

These signals request an external transfer on an individual DMA channel. DRQ3 is associated with DMA channel three, DRQ2 with channel two, DRQ1 with channel one, and DRQ0 with channel zero. These request signals can be individually programmed to be edge- or level-sensitive and either Active High or Low signal polarity. The DRQ3 pin can also be configured as a programmable I/O pin.

DT/$\overline{\text{R}}$

Data Transmit/Receive (Output)

This output is a direction control signal for the external data bus buffer.

$\overline{\text{FLOAT}}$

Float (Input)

This Active Low input forces all outputs into a high-impedance state.

HLDA/PIO9

Bus Hold Acknowledge [Programmable I/O] (Output)

This output is a signal from the CPU that the bus has been granted. The HLDA pin can also be configured as a programmable I/O pin.

HOLD/PIO8

Bus Hold Request [Programmable I/O] (Input)

This input is used by an external bus master to request bus access. It also functions as wake-up in suspend mode. The HOLD pin can also be configured as a programmable I/O pin.

INT0, INT1/$\overline{\text{SELECT}}$, INT2/$\overline{\text{INTA}}$0, INT3/$\overline{\text{INTA}}$1/IRQ, INT4, INT5, INT6/$\overline{\text{INTA}}$4 INT7/$\overline{\text{INTA}}$5 [PIO7–PIO0]

Maskable Interrupt Requests [Programmable I/O] (Inputs, Inputs/Outputs)

Maskable interrupt requests can be requested by activating one of these pins. When configured as inputs, these pins are Active High. Interrupt requests are synchronized internally. INT2, INT3, INT6, and INT7 can be configured to provide Active-Low interrupt-acknowledge output signals. All interrupt inputs can be configured to be either edge or level triggered. To ensure recognition, all interrupt requests must remain active

until the interrupt is acknowledged. Certain interrupt inputs can also be configured as programmable I/O pins.

LCS/RAS0

Lower Memory Chip Select/
Row Address Strobe 0 (Output)

This Active Low output can be programmed as a ROM/Flash chip select or as RAS for the first bank of DRAM.

MCS0/RAS1

Mid-Range Memory Chip Select 0
[Row Address Strobe 1] (Output)

This Active Low output can be programmed as an SRAM/ROM/Flash chip select for a mid-range bank memory device or as RAS for the second bank of DRAM.

MCS1/RAS2

Mid-Range Memory Chip Select 1
[Row Address Strobe 2] (Output)

This Active Low output can be programmed as an SRAM/ROM/Flash chip select for a mid-range bank memory device or as RAS for the third bank of DRAM.

MCS2/RAS3

Mid-Range Memory Chip Select 2
[Row Address Strobe 3] (Output)

This Active Low output can be programmed as an SRAM/ROM/Flash chip select for a mid-range bank memory device or as RAS for the fourth bank of DRAM.

MCS3/PIO31

Mid-Range Memory Chip Select 3
[Programmable I/O] (Output)

This Active Low output can be programmed as an SRAM/ROM/Flash chip select only. This pin can also be configured as a programmable I/O pin.

NMI

Nonmaskable interrupt (Schmitt-Triggered Input)

This input signals the Am386EM microcontroller to suspend execution of the current program and execute an interrupt-acknowledge function. The operation of this signal cannot be masked or disabled by software control.

PCS6/A2/PIO30

Peripheral Chip Select 6
[Latched A2/Programmable I/O] (Output)

Peripheral Chip Select 6 or Latched A2 can be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating PCS6 is software programmable. When programmed to provide latched A2 rather than PCS6, this pin retains the previously latched value of A2 during a bus HOLD. A2 is active High. PCS6/A2 does not float during bus HOLD. This pin can also be configured as a programmable I/O pin.

PCS5/A1/PIO29

Peripheral Chip Select 5
[Latched A1/Programmable I/O] (Output)

Peripheral Chip Select 5 or Latched A1 can be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating PCS5 is software programmable. When programmed to provide latched A1 rather than PCS5, this pin will retain the previously latched value of A1 during a bus HOLD. A1 is active High. PCS5/A1 does not float during bus HOLD. This pin can also be configured as a programmable I/O pin.

PCS4/PIO28–PCS0/PIO24

Programmable Chip Selects 4–0
[Programmable I/O] (Outputs)

These Active Low outputs are decoded chip select signals for peripheral devices. These lines do not float during bus HOLD. The address ranges activating PCS4–PCS0 are software programmable. These pins can also be configured as programmable I/O pins.

RD

System Read Strobe (Output)

This Active Low output indicates that the CPU is performing a memory or I/O read operation.

RESET

Reset (Schmitt-Triggered Input)

This Active Low input can be used with an external RC network to provide a power-on reset function.

RESOC

Open Collector Reset (Input/Output, Internal Pullup)

This line is driven active in response to RESET active, or the CPU can be reset by driving the line to Active Low as an input. This line is pulled up internally.

RTS1/PIO23, RTS0/PIO19

Request to Send [Programmable I/O] (Outputs)

When the Request to Send (RTS) bit is enabled on Serial Port 1 or 0, the signal goes High after the transmitter is empty. These pins can also be configured as programmable I/O pins.

RXD1/PIO20, RXD0/PIO16

Receive Data [Programmable I/O] (Inputs)

In asynchronous modes, these inputs are used to receive data on Serial Ports 1 and 0. In synchronous mode, the device transmits and receives data on RXD. These pins can also be configured as programmable I/O pins.

$\overline{S2}$–$\overline{S0}$

CPU Cycle Status (Outputs)

These outputs provide information about CPU cycle status.

TCK

JTAG Test Access Port Controller Clock (Input)

This input is the clock for the JTAG Test Access Port controller.

TDI

JTAG Test Access Port Controller Data Input (Input)

This input supplies data to the JTAG Test Access Port controller from an external source.

TDMA

Terminate DMA (Input/Output)

This signal is an input and open-collector output intended to be "wire-or'ed" with other open-collector drivers. An external pullup resistor is assumed to be present in the system design. As an input, this signal can be asserted by an external peripheral during any DMA transfer cycle to terminate the transfer after the current access. As an output, this signal is asserted by the processor during the last DMA cycle to indicate the end of the current DMA transfer.

TDO

JTAG Test Access Port Controller Data Output (Output)

This output supplies data from the JTAG Test Access Port controller to an external destination.

TMRIN1/PIO13, TMRIN0/PIO11

Counter/Timer [Programmable I/O] (Inputs)

Timer inputs are used as either clock or control signals, depending on the programmed timer modes. These pins can also be configured as programmable I/O pins.

TMROUT1/PIO12, TMROUT0/PIO10

Counter/Timer [Programmable I/O] (Outputs)

Timer outputs are used to provide single-pulse or continuous waveform generation, depending upon the timer mode selected. These pins can also be configured as programmable I/O pins.

TMS

JTAG Test Access Port Controller Mode Select (Input)

This input controls the operation of the JTAG Test Access Port controller.

$\overline{TRST}$

JTAG Test Access Port Controller Reset (Schmitt-Triggered Input)

This Active Low input resets the JTAG Test Access Port controller.

TXD1/PIO21, TXD0/PIO17

Transmit Data [Programmable I/O] (Outputs)

In asynchronous modes, these outputs are used to transmit data from Serial Ports 1 and 0. In synchronous mode, the device outputs a synchronizing clock on TXD when internal baud generation is selected. In external baud mode, the TXD pin is used to input the synchronous baud clock. These pins can also be configured as programmable I/O pins.

$\overline{UCS}$

Upper Memory Chip Select (Output)

This output can be programmed as a ROM/Flash chip select only. Power-on default is enabled at addresses FFFFF000–FFFFFFFFh for 8-bit boot ROM chip select.

$\overline{WAIT}$/SRDY

Wait State Control [Synchronous Ready] (Input)

The wait state control input is used by an external device to add CPU wait states to the current access.

$\overline{WE1}$–$\overline{WE0}$

Write Data Strobes (Outputs)

These outputs indicate that the CPU is performing a memory or I/O write operation. $\overline{WE0}$ active indicates write enable for the lower byte, and $\overline{WE1}$ indicates write operation to the upper byte.

X2

Crystal Output (Output)

This pin and the X1 pin provide connections for a fundamental mode or third overtone parallel resonant crystal used by the internal oscillator circuit. To provide the microcontroller with an external clock source instead, leave the X2 pin unconnected and connect the source to the X1 pin.

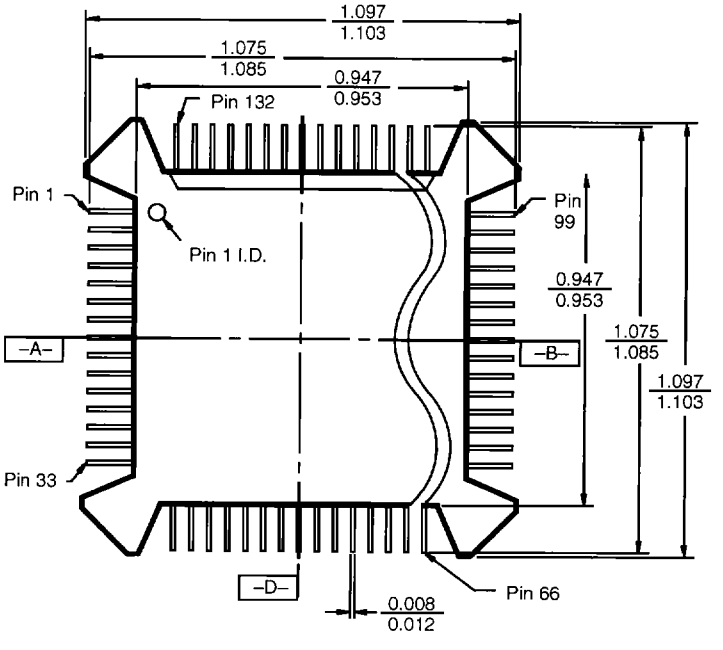
X1

Crystal Input (Input)

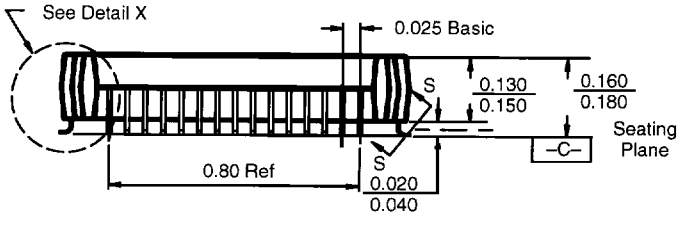
This pin and the X2 pin provide connections for a fundamental mode or third overtone parallel resonant crystal used by the internal oscillator circuit. To provide the microcontroller with an external clock source instead, connect the source to the X1 pin and leave the X2 pin unconnected.

PHYSICAL DIMENSIONS

PQB 132—Plastic Quad Flat Pack; Trimmed and Formed



Top View

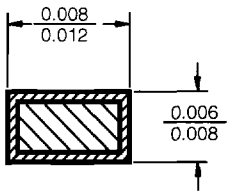


Side View

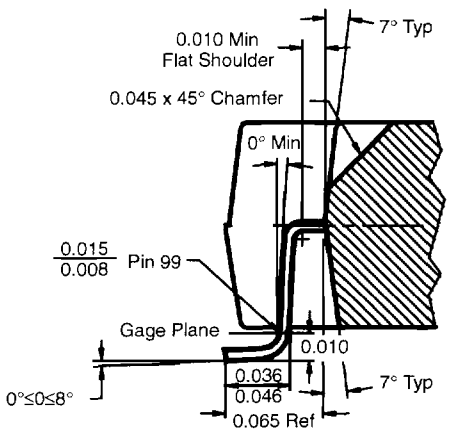
Note:

All measurements are in inches unless otherwise noted. Not to scale. For reference only. BSC is an ANSI standard for Basic Space Centering

PQB 132 (continued)



Section S–S



Detail X

Note:

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