Enpirion® Power Datasheet

EP53A8LQI/HQI 1A PowerSoC Voltage Mode Synchronous PWM Buck with Integrated Inductor

Description

The EP53A8LQI and EP53A8HQI are 1A PowerSoCs with integrated MOSFET switches, control, compensation, and inductor in an advanced 3mm x 3mm QFN Package.

Integrated inductor ensures the complete power solution is fully characterized with the inductor carefully matched to the silicon and compensation network. It enables a tiny solution footprint, low output ripple, low part-count, and high reliability, while maintaining high efficiency. The complete solution can be implemented in as little as 21mm^2 and operate from -40°C to 85°C ambient temperature range.

The EP53A8xQI uses a 3-pin VID to easily select the output voltage setting. Output voltage settings are available in 2 optimized ranges providing coverage for typical V_{OUT} settings.

The VID pins can be changed on the fly for fast dynamic voltage scaling. EP53A8LQI further has the option to use an external voltage divider.

Features

- Integrated Inductor Technology
- 3mm x 3mm x 1.1mm QFN Package
- Total Solution Footprint ~ 21mm^2
- Low V_{OUT} Ripple for IO Compatibility
- High Efficiency, up to 94%
- V_{OUT} Range 0.6V to V_{IN} – 0.5V
- 1A Continuous Output Current
- 5 MHz Switching Frequency
- 3-pin VID for Glitch Free Voltage Scaling
- Short Circuit and Over Current Protection
- UVLO and Thermal Protection
- IC Level Reliability in a PowerSoC Solution

Applications

- Portable Wireless and RF applications
- Wireless Broad Band Data Cards
- Solid State Storage Applications
- Noise and Space Sensitive Applications

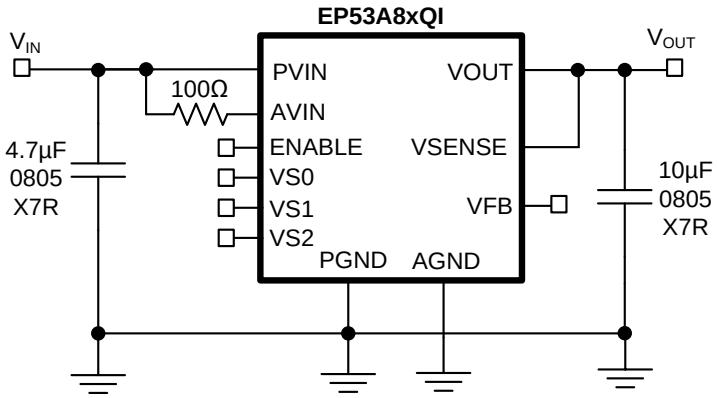


Figure 1. Simplified Applications Circuit

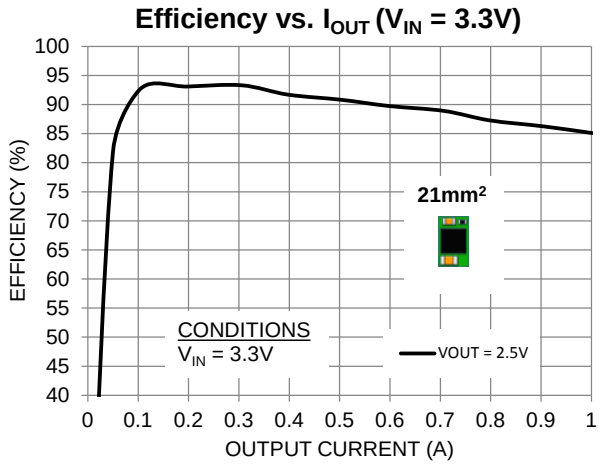


Figure 2. Highest Efficiency in Smallest Solution Size

Ordering Information

Part Number	Package Markings	T_A (°C)	Package Description
EP53A8LQI	AJXX	-40 to +85	16-pin (3mm x 3mm x 1.1mm) QFN
EP53A8HQI	AMXX	-40 to +85	16-pin (3mm x 3mm x 1.1mm) QFN
EVB-EP53A8xQI		QFN Evaluation Board	

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Pin Assignments (Top View)

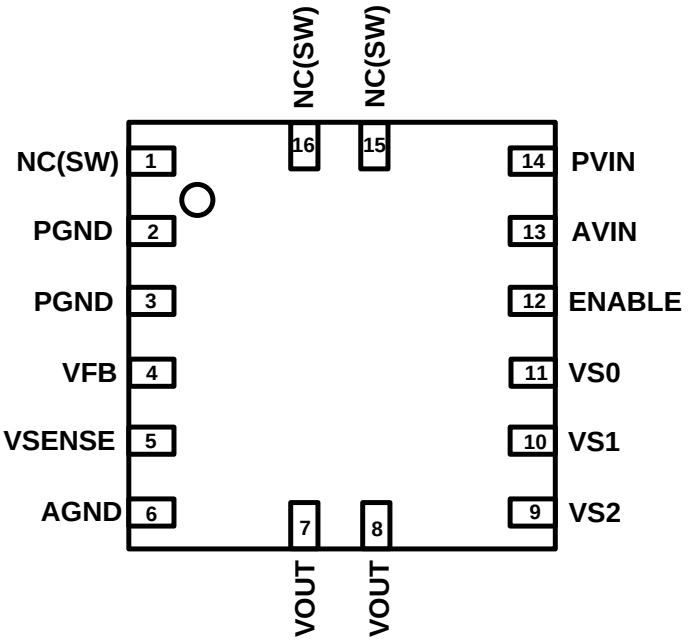


Figure 3. EP53A8LQI Pin Out Diagram (Top View)

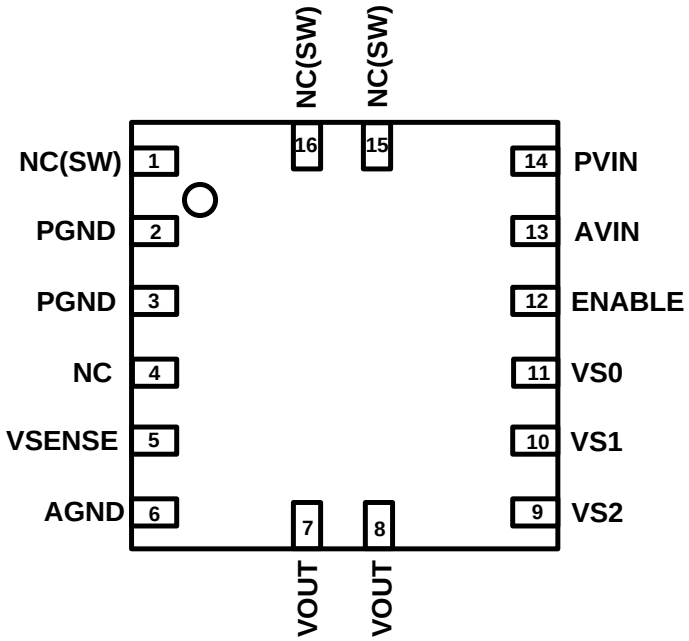


Figure 4. EP53A8HQI Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White 'dot' on top left is pin 1 indicator on top of the device package.

Pin Description

PIN	NAME	FUNCTION
PIN	**NAME**	**FUNCTION**
1, 15, 16	NC(SW)	NO CONNECT – These pins are internally connected to the common switching node of the internal MOSFETs. NC (SW) pins are not to be electrically connected to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage to the device.
2,3	PGND	Power ground. Connect this pin to the ground electrode of the Input and output filter capacitors.
4	VFB / NC	EP53A8LQI: Feedback pin for external divider option. EP53A8HQI: No Connect
5	VSENSE	Sense pin for preset output voltages. Refer to application section for proper configuration.
6	AGND	Analog ground. This is the quiet ground for the internal control circuitry, and the ground return for external feedback voltage divider
7, 8	VOUT	Regulated Output Voltage. Refer to application section for proper layout and decoupling.

PIN	NAME	FUNCTION
9, 10, 11	VS2, VS1, VS0	Output voltage select. VS2 = pin 9, VS1 = pin 10, VS0 = pin 11. EP53A8LQI: Selects one of seven preset output voltages or an external resistor divider. EP53A8HQI: Selects one of eight preset output voltages. (Refer to section on output voltage select for more details.)
12	ENABLE	Output Enable. Enable = logic high; Disable = logic low
13	AVIN	Input power supply for the controller circuitry. Connect to PVIN through a 100 Ohm resistor.
14	PVIN	Input Voltage for the MOSFET switches.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage	V_{IN}	-0.3	6.0	V
Voltages on: ENABLE, V_{SENSE}, $V_{SO} – V_{S2}$		-0.3	V_{IN}+ 0.3	V
Voltages on: V_{FB} (EP53A8LQI)		-0.3	2.7	V
Maximum Operating Junction Temperature	T_{J-ABS}		150	°C
Storage Temperature Range	T_{STG}	-65	150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020C			260	°C
ESD Rating (based on Human Body Mode)			2000	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.4	5.5	V
Operating Ambient Temperature	T_A	- 40	+85	°C
Operating Junction Temperature	T_J	- 40	+125	°C

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient –0 LFM (**Note 1**)	θ_{JA}	80	°C/W
Thermal Overload Trip Point	T_{J-TP}	+155	°C
Thermal Overload Trip Point Hysteresis		25	°C

Note 1: Based on a four layer copper board and proper thermal design per JEDEC EIJ/JESD51 standards.

Electrical Characteristics

NOTE: V_{IN}=3.6V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		2.4		5.5	V
Under Voltage Lock-out – V_{IN} Rising	V_{UVLO_R}			2.0		V
Under Voltage Lock-out – V_{IN} Falling	V_{UVLO_F}			1.9		V

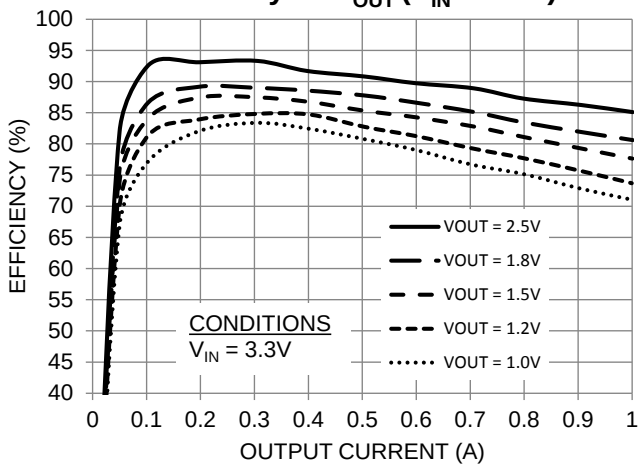
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drop Out Resistance	R_{DO}	Input to Output Resistance		350	500	mΩ
Output Voltage Range	V_{OUT}	EP53A8LQI ($V_{DO} = I_{LOAD} X R_{DO}$) EP53A8HQI	0.6 1.8		V_{IN}-V_{DO} 3.3	V
Dynamic Voltage Slew Rate	V_{SLEW}	EP53A8HQI EP53A8LQI		8 4		V/ms
VID Preset V_{OUT} Initial Accuracy	ΔV_{OUT}	T_A = 25°C, V_{IN} = 3.6V; I_{LOAD} = 100mA ; 0.8V ≤ V_{OUT} ≤ 3.3V	-2		+2	%
VFB Pin Voltage (Load and Temperature)	V_{VFB}	0A ≤ I_{LOAD} ≤ 1A Starting Date Code: X501 or greater	0.588	0.6	0.612	V
Line Regulation	ΔV_{OUT_LINE}	2.4V ≤ V_{IN} ≤ 5.5V; Load = 0A		0.03		%/V
Load Regulation	ΔV_{OUT_LOAD}	0A ≤ I_{LOAD} ≤ 1A; V_{IN} = 3.6V		0.6		%/A
Temperature Variation	ΔV_{OUT_TEMPL}	-40°C ≤ T_A ≤ +85°C		30		ppm/°C
Output Current Range	I_{OUT}	Subject to de-rating	0		1000	mA
Shut-down Current	I_{SD}	Enable = Low		0.75		µA
OCP Threshold	I_{LIM}	2.4V ≤ V_{IN} ≤ 5.5V 0.6V ≤ V_{OUT} ≤ 3.3V	1.25	1.4		A
VS0-VS2, Pin Logic Low	V_{VSLO}		0.0		0.3	V
VS0-VS2, Pin Logic High	V_{VSHI}		1.4		V_{IN}	V
VS0-VS2, Pin Input Current	I_{VSX}	Note 1		<100		nA
Enable Pin Logic Low	V_{ENLO}				0.3	V
Enable Pin Logic High	V_{ENHI}		1.4			V
Enable Pin Current	I_{ENABLE}	Note 1		<100		nA
Feedback Pin Input Current	I_{FB}	Note 1		<100		nA
Operating Frequency	F_{OSC}			5		MHz
Soft Start Operation						
Soft Start Slew Rate	ΔV_{SS}	EP53A8HQI (VID only) EP53A8LQI (VID only)		8 4		V/ms
Soft Start Rise Time	ΔT_{SS}	EP53A8LQI (VFB mode); Note 2	170	225	280	µs

Note 1: Parameter guaranteed by design and characterization.

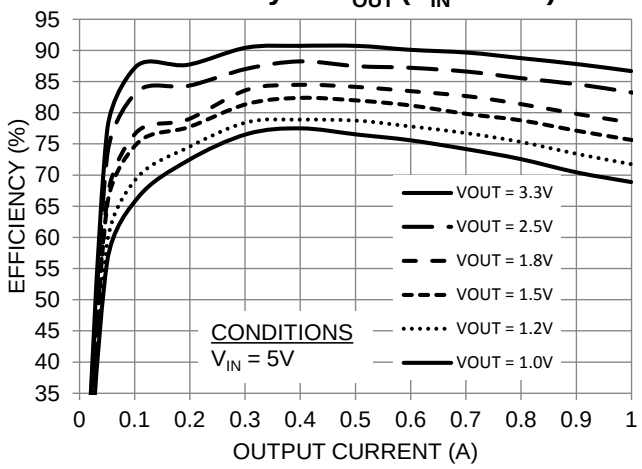
Note 2: Measured from when V_{IN} ≥ V_{UVLO_R} & ENABLE pin crosses its logic High threshold.

Typical Performance Curves

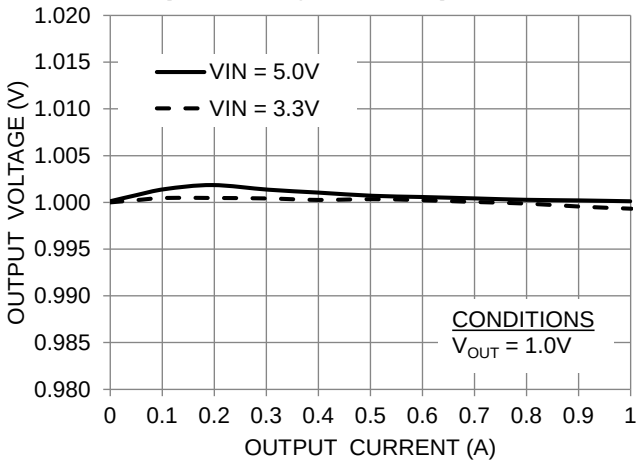
Efficiency vs. I_{OUT} (V_{IN} = 3.3V)



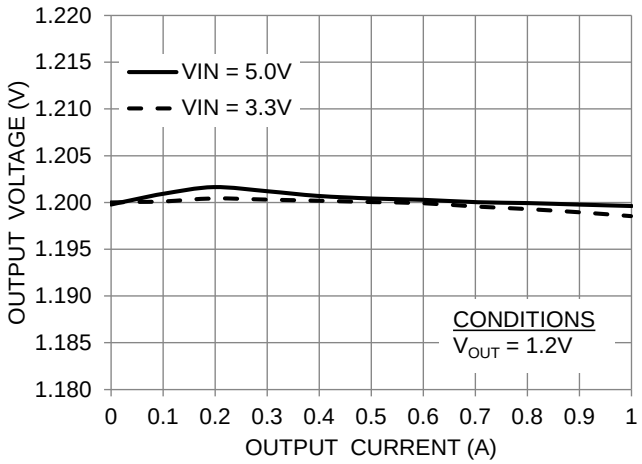
Efficiency vs. I_{OUT} (V_{IN} = 5.0V)



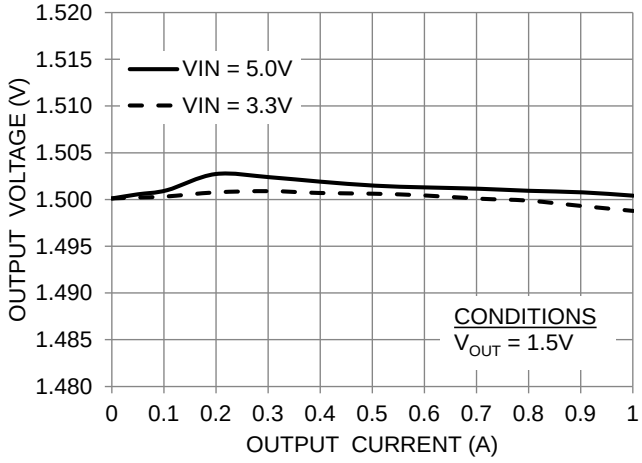
Output Voltage vs. Output Current



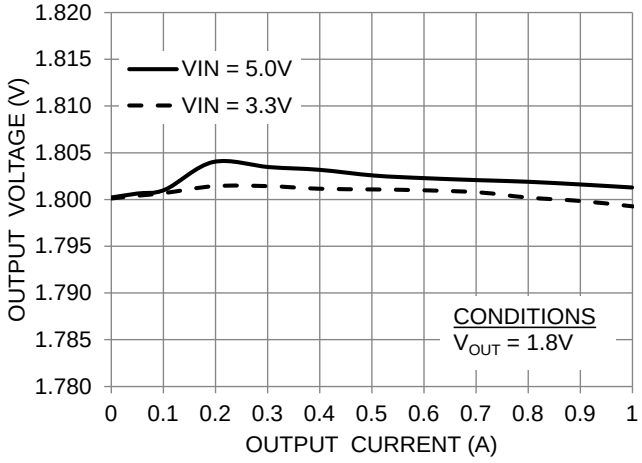
Output Voltage vs. Output Current



Output Voltage vs. Output Current

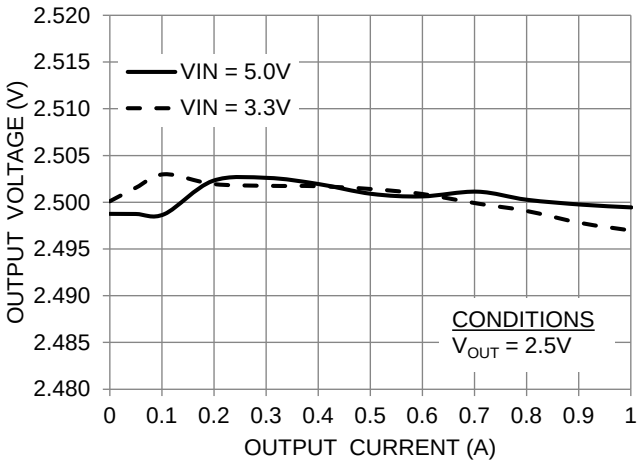


Output Voltage vs. Output Current

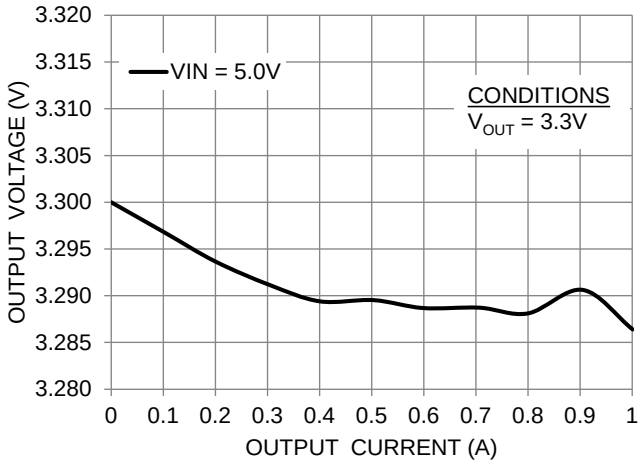


Typical Performance Curves (Continued)

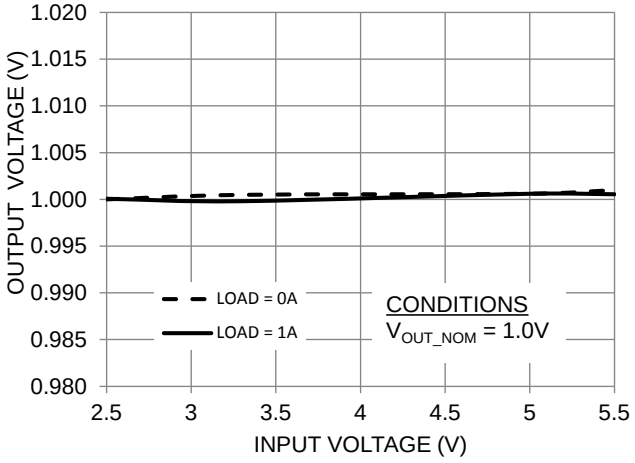
Output Voltage vs. Output Current



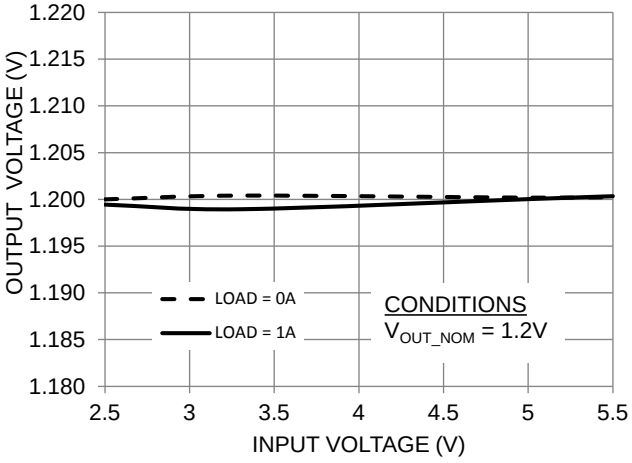
Output Voltage vs. Output Current



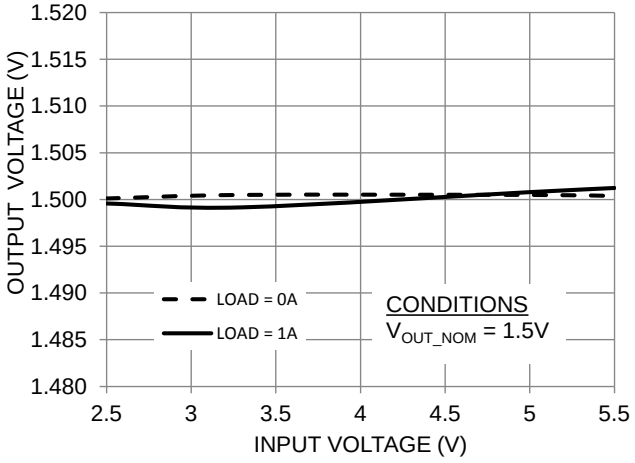
Output Voltage vs. Input Voltage



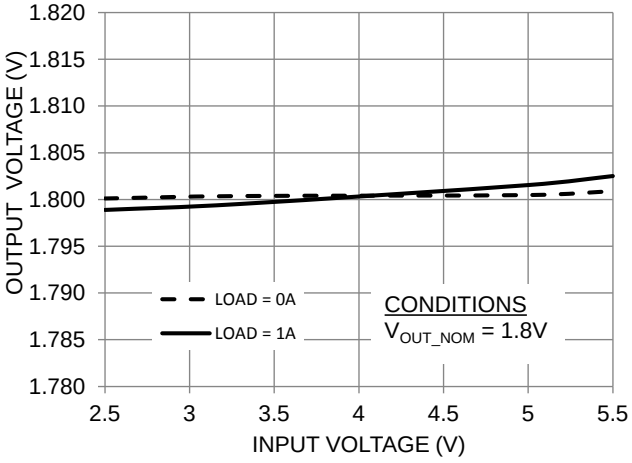
Output Voltage vs. Input Voltage



Output Voltage vs. Input Voltage

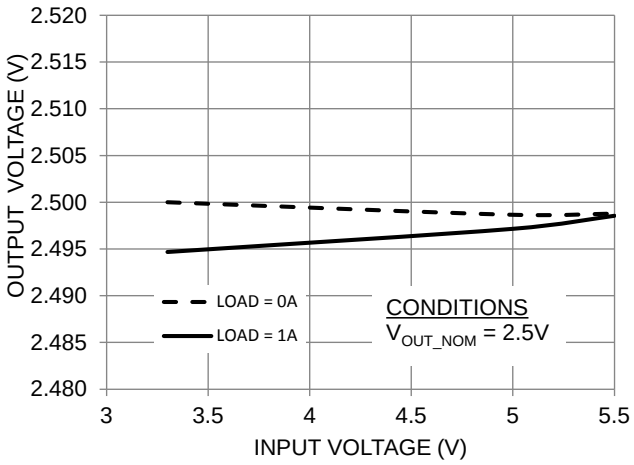


Output Voltage vs. Input Voltage

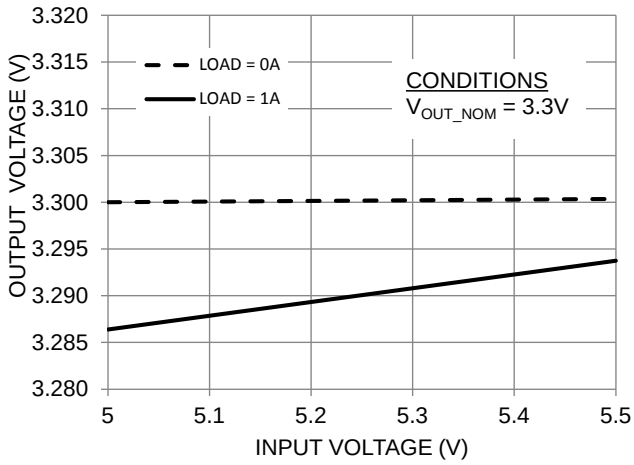


Typical Performance Curves (Continued)

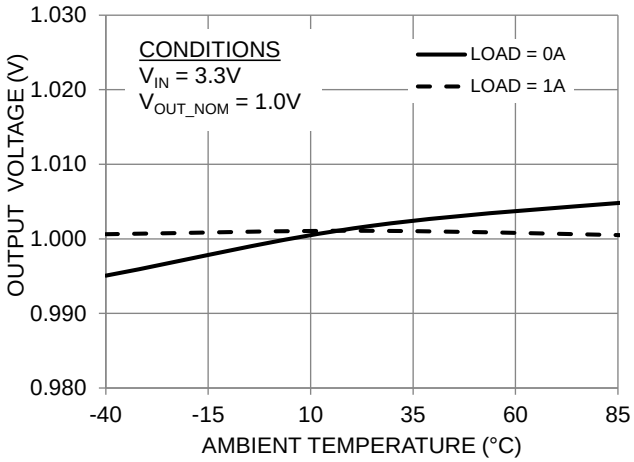
Output Voltage vs. Input Voltage



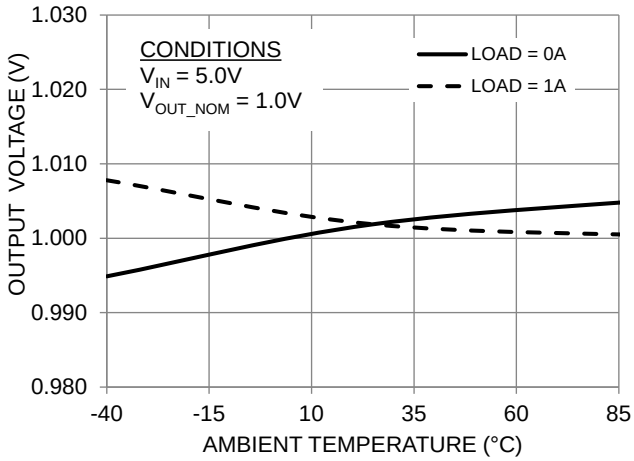
Output Voltage vs. Input Voltage



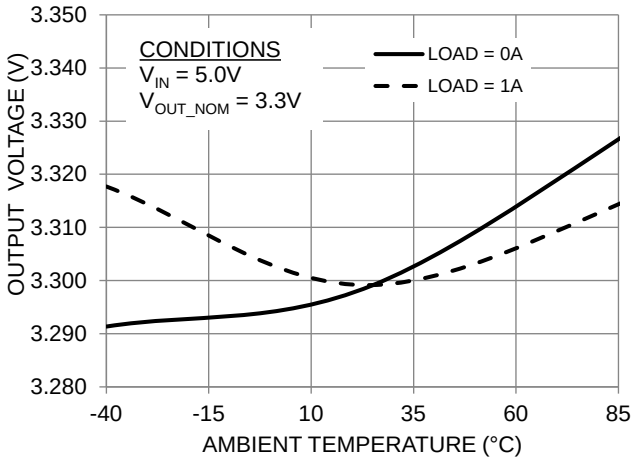
Output Voltage vs. Temperature



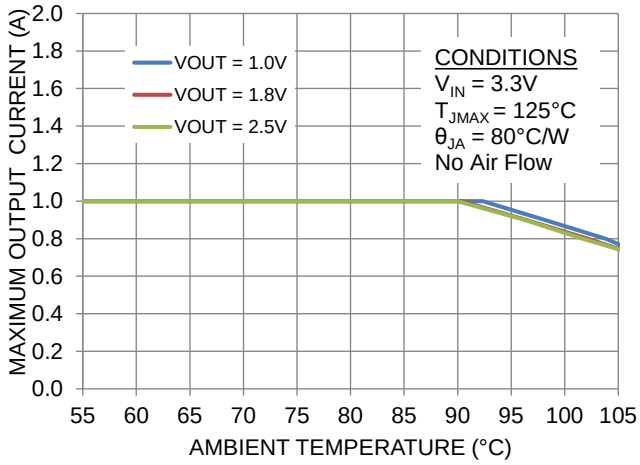
Output Voltage vs. Temperature



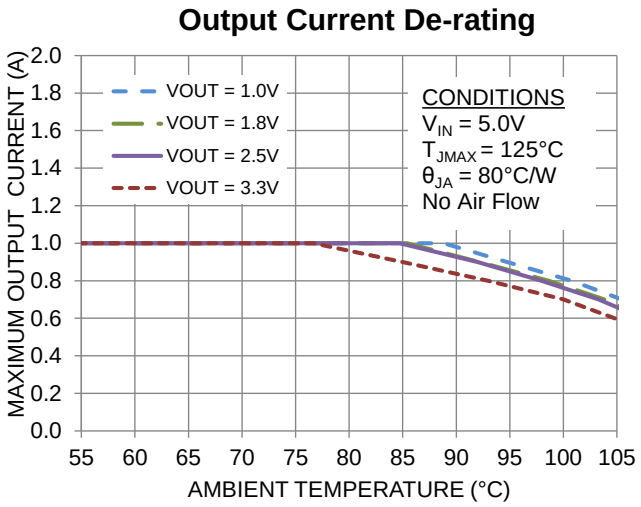
Output Voltage vs. Temperature



Output Current De-rating

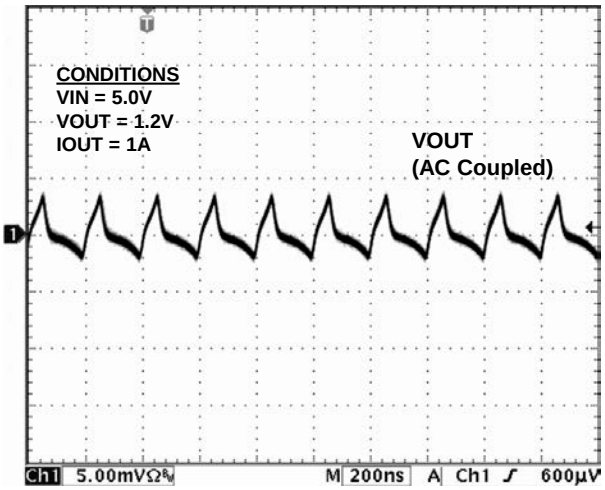


Typical Performance Curves (Continued)

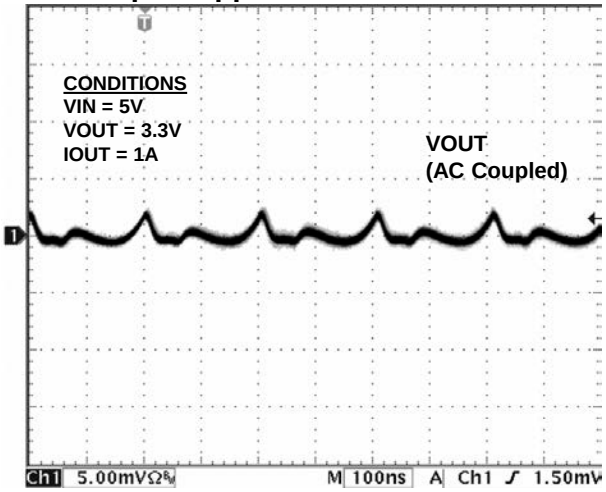


Typical Performance Characteristics

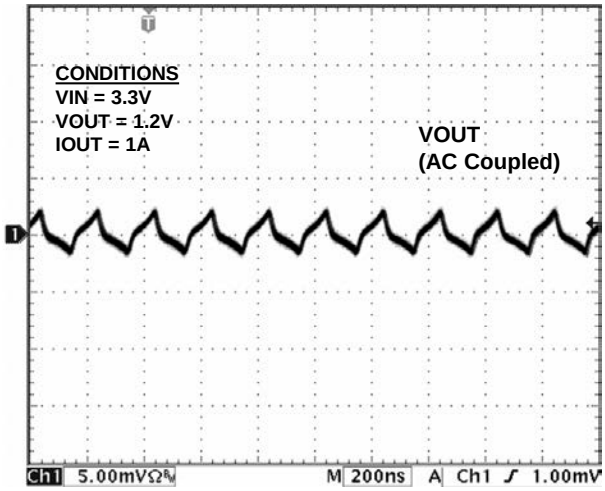
Output Ripple at 20MHz Bandwidth



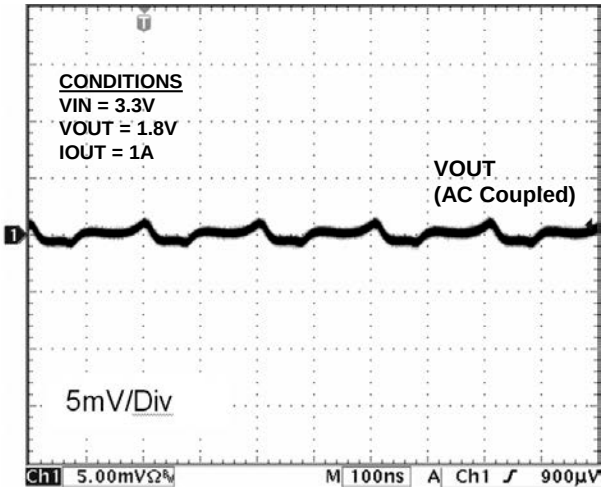
Output Ripple at 20MHz Bandwidth



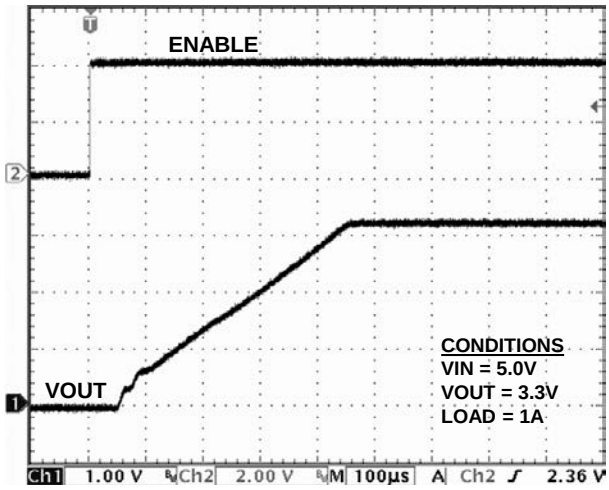
Output Ripple at 20MHz Bandwidth



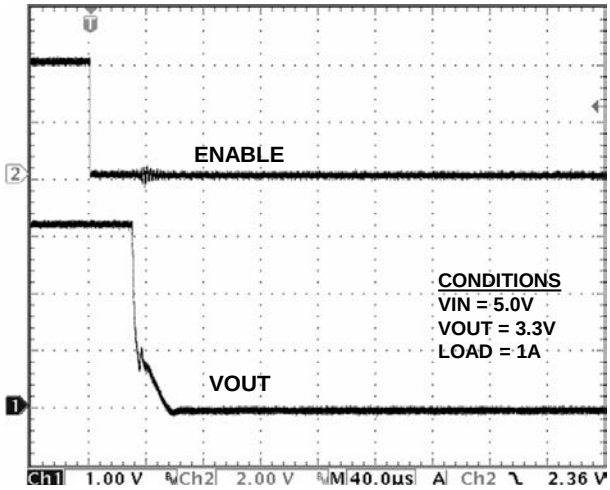
Output Ripple at 20MHz Bandwidth



Enable Power Up

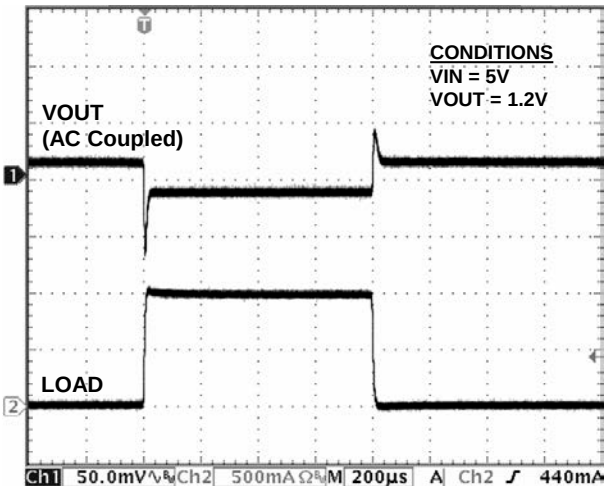


Enable Power Down

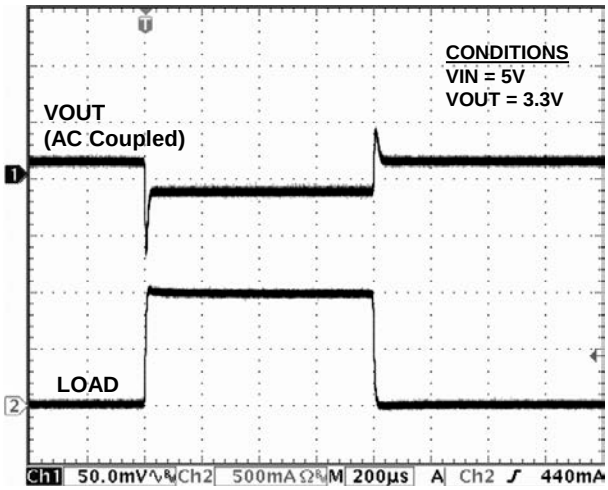


Typical Performance Characteristics (Continued)

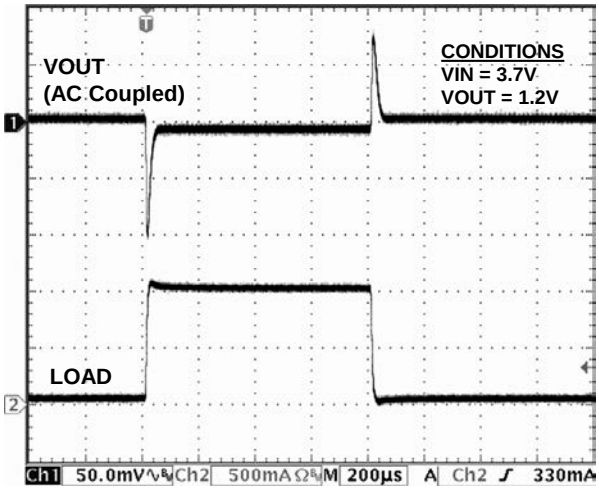
Load Transient from 0 to 1A



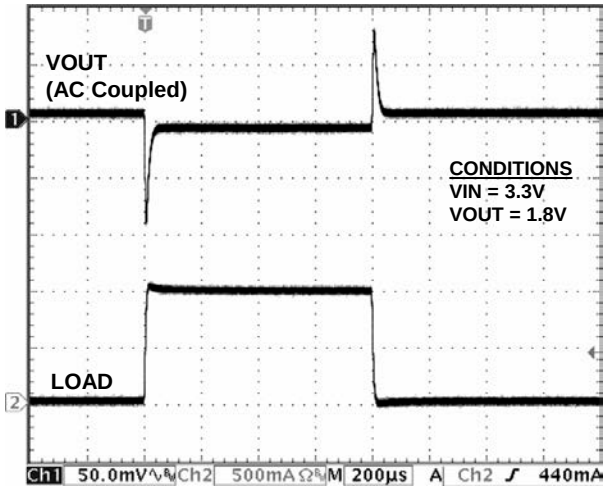
Load Transient from 0 to 1A



Load Transient from 0 to 1A



Load Transient from 0 to 1A



Functional Block Diagram

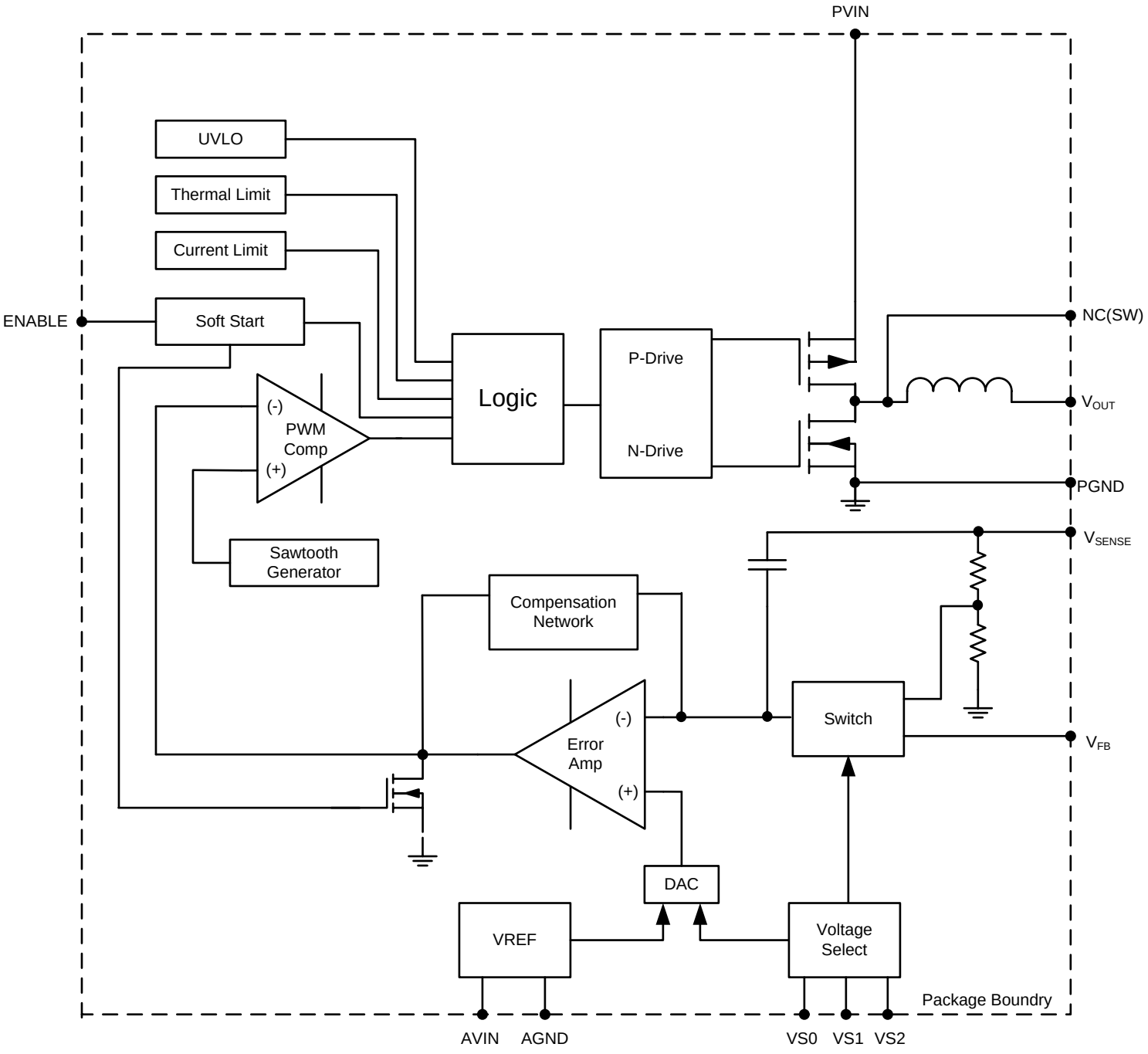


Figure 5. Functional Block Diagram

Functional Description

Functional Overview

The EP53A8xQI requires only 2 small MLCC capacitors and an 0201 MLC resistor for a complete DC-DC converter solution. The device integrates MOSFET switches, PWM controller, Gate-drive, compensation, and inductor into a tiny 3mm x 3mm x 1.1mm QFN package. Advanced package design, along with the high level of integration, provides very low output ripple and noise. The EP53A8xQI uses voltage mode control for high noise immunity and load matching to advanced ≤90nm loads. A 3-pin VID allows the user to choose from one of 8 output voltage settings. The EP53A8xQI comes with two VID output voltage ranges. The EP53A8HQI provides V_{OUT} settings from 1.8V to 3.3V, the EP53A8LQI provides VID settings from 0.8V to 1.5V, and also has an external resistor divider option to program output setting over the 0.6V to V_{IN}-0.5V range. The EP53A8xQI provides the industry's highest power density of any 1A DCDC converter solution.

The key enabler of this revolutionary integration is Altera's proprietary power MOSFET technology. The advanced MOSFET switches are implemented in deep-submicron CMOS to supply very low switching loss at high switching frequencies and to allow a high level of integration. The semiconductor process allows seamless integration of all switching, control, and compensation circuitry.

The proprietary magnetics design provides high-density/high-value magnetics in a very small footprint. Altera Enpirion magnetics are carefully matched to the control and compensation circuitry yielding an optimal solution with assured performance over the entire operating range.

Protection features include under-voltage lock-out (UVLO), over-current protection (OCP), short circuit protection, and thermal overload protection.

Integrated Inductor: Low-Noise Low-EMI

The EP53A8xQI utilizes a proprietary low loss integrated inductor. The integration of the inductor greatly simplifies the power supply design process. The inherent shielding and compact construction of the integrated inductor reduces the conducted and radiated noise that can couple into the traces of the printed circuit board. Further, the package layout is optimized to reduce the electrical path length for the high di/dT input AC ripple currents that are a major source of radiated emissions from DC-DC converters. The integrated inductor provides the optimal solution to the complexity, output ripple, and noise that plague low power DCDC converter design.

Voltage Mode Control, High Bandwidth

The EP53A8xQI utilizes an integrated type III compensation network. Voltage mode control is inherently impedance matched to the sub 90nm process technology that is used in today's advanced ICs. Voltage mode control also provides a high degree of noise immunity at light load currents so that low ripple and high accuracy are maintained over the entire load range. The very high switching frequency allows for a very wide control loop bandwidth and hence excellent transient performance.

Soft Start

Internal soft start circuits limit in-rush current when the device starts up from a power down condition or when the "ENABLE" pin is asserted "high". Digital control circuitry limits the V_{OUT} ramp rate to levels that are safe for the Power MOSFETS and the integrated inductor.

The EP53A8HQI has a soft-start slew rate that is twice that of the EP53A8LQI.

When the EP53A8LQI is configured in external resistor divider mode, the device has a fixed VOUT ramp time. Therefore, the ramp rate will vary with the output voltage setting. Output voltage ramp time is given in the Electrical Characteristics Table.

Excess bulk capacitance on the output of the device can cause an over-current condition at startup. Assuming no-load at startup, the

maximum total capacitance on the output, including the output filter capacitor and bulk and decoupling capacitance, at the load, is given as:

EP53A8LQI:

$C_{OUT\_TOTAL\_MAX} = C_{OUT\_Filter} + C_{OUT\_BULK} = 250uF$

EP53A8HQI:

$C_{OUT\_TOTAL\_MAX} = C_{OUT\_Filter} + C_{OUT\_BULK} = 125uF$

EP53A8LQI (in external divider mode):

$C_{OUT\_TOTAL\_MAX} = 2.25x10^{-4}/V_{OUT}$ Farads

The nominal value for C_{OUT} is 10uF. See the applications section for more details.

Over Current/Short Circuit Protection

The current limit function is achieved by sensing the current flowing through a sense P-MOSFET which is compared to a reference current. When this level is exceeded the P-FET is turned off and the N-FET is turned on, pulling V_{OUT} low. This condition is maintained for approximately 0.5mS and then a normal soft start is initiated. If the over current condition still persists, this cycle will repeat.

Under Voltage Lockout

During initial power up, an under voltage lockout circuit will hold-off the switching circuitry until the input voltage reaches a sufficient level to insure proper operation. If

the lockout circuitry will again disable the switching. Hysteresis is included to prevent chattering between states.

Enable

The ENABLE pin provides a means to shut down the converter or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation.

NOTE: The ENABLE pin must not be left floating.

Thermal Shutdown

When excessive power is dissipated in the chip, the junction temperature rises. Once the junction temperature exceeds the thermal shutdown temperature, the thermal shutdown circuit turns off the converter output voltage thus allowing the device to cool. When the junction temperature decreases by 25C°, the device will go through the normal startup process.

Application Information

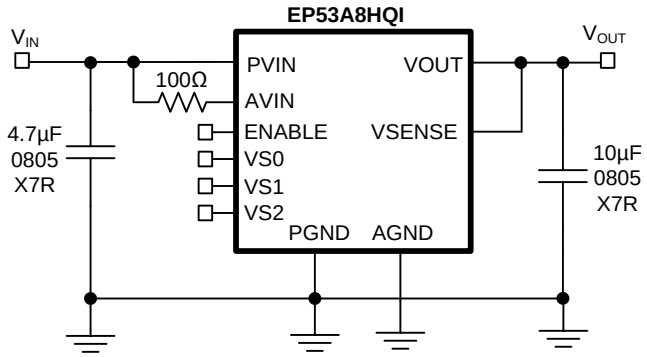


Figure 6. EP53A8HQI VID Application Circuit

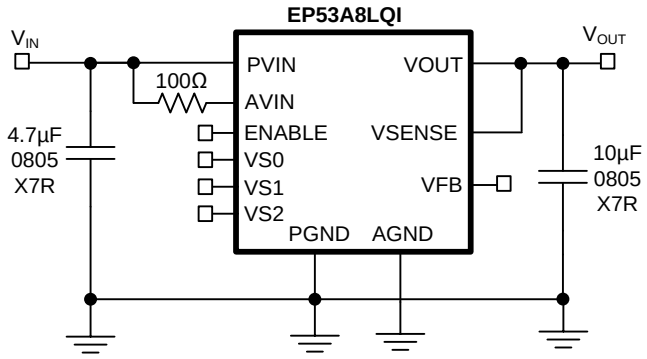


Figure 7. EP53A8LQI VID Application Circuit

Output Voltage Programming

The EP53A8xQI utilizes a 3-pin VID to program the output voltage value. The VID is available in two sets of output VID programming ranges. The VID pins should be connected either to an external control signal, AVIN or to AGND to avoid noise coupling into the device.

The "Low" range is optimized for low voltage applications. It comes with preset VID settings ranging from 0.80V and 1.5V. This VID set also has an external divider option.

To specify this VID range, order part number EP53A8LQI.

The "High" VID set provides output voltage settings ranging from 1.8V to 3.3V. This version does not have an external divider option. To specify this VID range, order part number EP53A8HQI.

Internally, the output of the VID multiplexer sets the value for the voltage reference DAC, which in turn is connected to the non-inverting input of the error amplifier. This allows the use of a single feedback divider with constant loop gain and optimum compensation, independent of the output voltage selected.

NOTE: The VID pins must not be left floating.

Table 1: EP53A8LQI VID Voltage Select Settings

VS2	VS1	VS0	VOUT
0	0	0	1.50
0	0	1	1.45
0	1	0	1.20
0	1	1	1.15
1	0	0	1.10
1	0	1	1.05
1	1	0	0.8
1	1	1	EXT

EP53A8L Low VID Range Programming

The EP53A8LQI is designed to provide a high degree of flexibility in powering applications that require low V_{OUT} settings and dynamic voltage scaling (DVS). The device employs a 3-pin VID architecture that allows the user to choose one of seven (7) preset output voltage settings, or the user can select an external voltage divider option. The VID pin settings can be changed on the fly to implement glitch-free voltage scaling.

Table 1 shows the VS2-VS0 pin logic states for the EP53A8LQI and the associated output voltage levels. A logic "1" indicates a connection to AVIN or to a "high" logic voltage level. A logic "0" indicates a connection to AGND or to a "low" logic voltage level. These pins can be either hardwired to AVIN or AGND or alternatively can be driven by standard logic levels. Logic levels are defined in the electrical characteristics table. Any level between the logic high and logic low is indeterminate.

EP53A8LQI External Voltage Divider

The external divider option is chosen by connecting VID pins VS2-VS0 to V_{IN} or a logic "1" or "high". The EP53A8LQI uses a separate

feedback pin, V_{FB}, when using the external divider. V_{SENSE} must be connected to V_{OUT} as indicated in Figure 8.

The output voltage is selected by the following formula:

$$V_{OUT} = 0.6V\left(1+\frac{Ra}{Rb}\right)$$

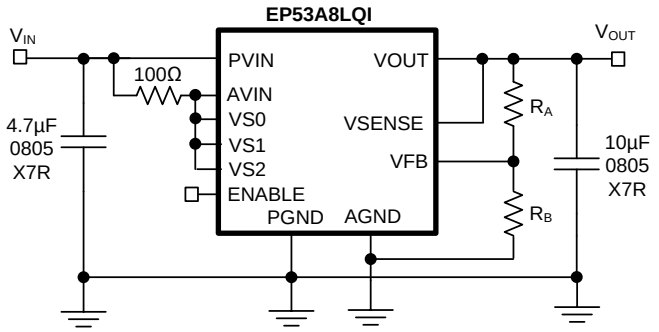


Figure 8. EP53A8LQI External VOUT Setting

R_a must be chosen as 237KΩ to maintain loop gain. Then R_b is given as:

$$R_b = \frac{142.2x10^3}{V_{OUT}-0.6}\Omega$$

V_{OUT} can be programmed over the range of 0.6V to (V_{IN} – 0.5V).

NOTE: Dynamic Voltage Scaling is not allowed between internal preset voltages and external divider.

EP53A8HQI High VID Range Programming

The EP53A8HQI V_{OUT} settings are optimized for higher nominal voltages such as those required to power IO, RF, or IC memory. The preset voltages range from 1.8V to 3.3V. There are eight (8) preset output voltage settings. The EP53A8HQI does not have an external divider option. As with the EP53A8LQI, the VID pin settings can be changed while the device is enabled.

Table 2 shows the VS0-VS2 pin logic states for the EP53A8HQI and the associated output voltage levels. A logic "1" indicates a connection to AVIN or to a "high" logic voltage level. A logic "0" indicates a connection to AGND or to a "low" logic voltage level. These pins can be either hardwired to AVIN or AGND or alternatively can be driven by standard logic levels. Logic levels are defined in the electrical characteristics table. Any level between the logic high and logic low is indeterminate. These pins must not be left floating.

Table 2: EP53A8HQI VID Voltage Select Settings

VS2	VS1	VS0	VOUT
0	0	0	3.3
0	0	1	3.0
0	1	0	2.9
0	1	1	2.6
1	0	0	2.5
1	0	1	2.2
1	1	0	2.1
1	1	1	1.8

Power-Up/Down Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. The PVIN should never be powered when AVIN is off. During power down, the AVIN should not be powered down before the PVIN. Tying PVIN and AVIN or all three pins (AVIN, PVIN, ENABLE) together during power up or power down meets these requirements.

Pre-Bias Start-up

The EP53A8xQI does not support startup into a pre-biased condition. Be sure the output capacitors are not charged or the output of the EP53A8xQI is not pre-biased when the EP53A8xQI is first enabled.

Input Filter Capacitor

The **input** filter capacitor requirement is a 4.7µF 0603 low ESR MLCC capacitor. The input capacitor must use X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and with temperature, and are not suitable for switch-mode DC-DC converter input filter applications.

Output Filter Capacitor

The **output** filter capacitor requirement is a minimum of 10µF 0805 MLCC. Ripple performance can be improved by using 2x10µF

0805 MLCC capacitors.

The maximum output filter capacitance next to the output pins of the device is 60µF low ESR MLCC capacitance. V_{OUT} has to be sensed at the last output filter capacitor next to the EP53A8xQI.

Additional bulk capacitance for decoupling and bypass can be placed at the load as long as there is sufficient separation between the V_{OUT} Sense point and the bulk capacitance. The separation provides an inductance that isolates the control loop from the bulk capacitance.

Excess total capacitance on the output (Output Filter + Bulk) can cause an over-current condition at startup. Refer to the section on Soft-Start for the maximum total capacitance on the output.

The output capacitor must use X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations lose capacitance with frequency, bias, and temperature and are not suitable for switch-mode DC-DC converter output filter applications.

Thermal Considerations

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be accounted for. The Enpirion PowerSoC helps alleviate some of those concerns. The Enpirion EP53A8xQI DC-DC converter is packaged in a 3x3x1.1mm 16-pin QFN package. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 155°C.

The following example and calculations illustrate the thermal performance of the EP53A8xQI.

Example:

V_{IN} = 5V

V_{OUT} = 3.3V

I_{OUT} = 1A

First calculate the output power.

P_{OUT} = 3.3V x 1A = 3.3W

Next, determine the input power based on the efficiency (η) shown in Figure 9.

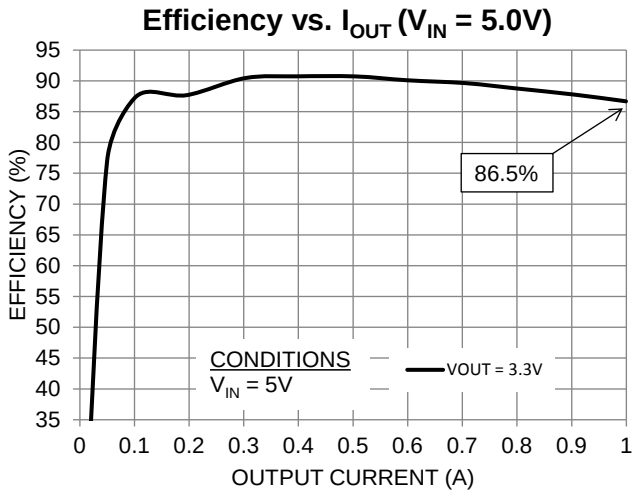


Figure 9. Efficiency vs. Output Current

For V_{IN} = 5V, V_{OUT} = 3.3V at 1A, η ≈ 86.5%

η = P_{OUT} / P_{IN} = 86.5% = 0.865

P_{IN} = P_{OUT} / η

P_{IN} ≈ 3.3W / 0.865 ≈ 3.815W

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

P_D = P_{IN} – P_{OUT}

≈ 3.815W – 3.3W ≈ 0.515W

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EP53A8xQI has a θ_{JA} value of 80 ºC/W without airflow.

Determine the change in temperature (ΔT) based on P_D and θ_{JA}.

ΔT = P_D x θ_{JA}

ΔT ≈ 0.515W x 80°C/W = 41.2°C ≈ 41°C

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

T_J = T_A + ΔT

T_J ≈ 25°C + 41°C ≈ 66°C

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

T_{AMAX} = T_{JMAX} – P_D x θ_{JA}

≈ 125°C – 41°C ≈ 84°C

The maximum ambient temperature (before de-rating) the device can reach is 84°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.

Layout Recommendations

Figure 10 shows critical components and layer 1 traces of a recommended minimum footprint EP53A8LQI/EP53A8HQI layout with ENABLE tied to V_{IN}. Alternate ENABLE configurations, and other small signal pins need to be connected and routed according to specific customer application. Please see the Gerber files on the Altera website www.altera.com/enpirion for exact dimensions and other layers. Please refer to Figure 10 while reading the layout recommendations in this section.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EP53A8xQI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EP53A8xQI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: Input and output grounds are separated until they connect at the PGND pins. The separation shown on Figure 10 between the input and output GND circuits helps minimize noise coupling between the converter input and output switching loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors. Please see the Gerber files on the Altera website www.altera.com/enpirion.

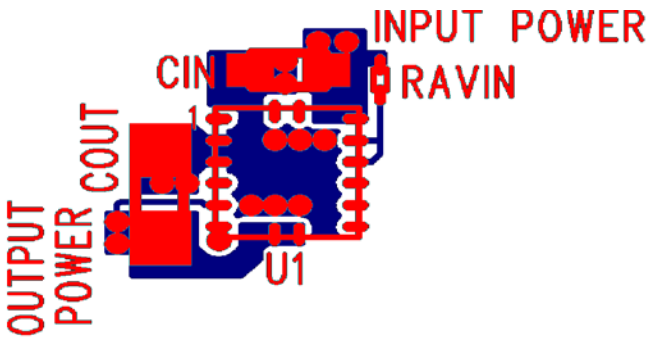


Figure 10. Top PCB Layer Critical Components and Copper for Minimum Footprint

Recommendation 4: Multiple small vias should be used to connect the ground traces under the device to the system ground plane on another layer for heat dissipation. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. It is preferred to put these vias under the capacitors along the edge of the GND copper closest to the +V copper. Please see Figure 10. These vias connect the input/output filter capacitors to the GND plane and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT}, then put them just outside the capacitors along the GND. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

Recommendation 5: AVIN is the power supply for the internal small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 10 this connection is made with RAVIN at the input capacitor close to the V_{IN} connection.

Recommended PCB Footprint

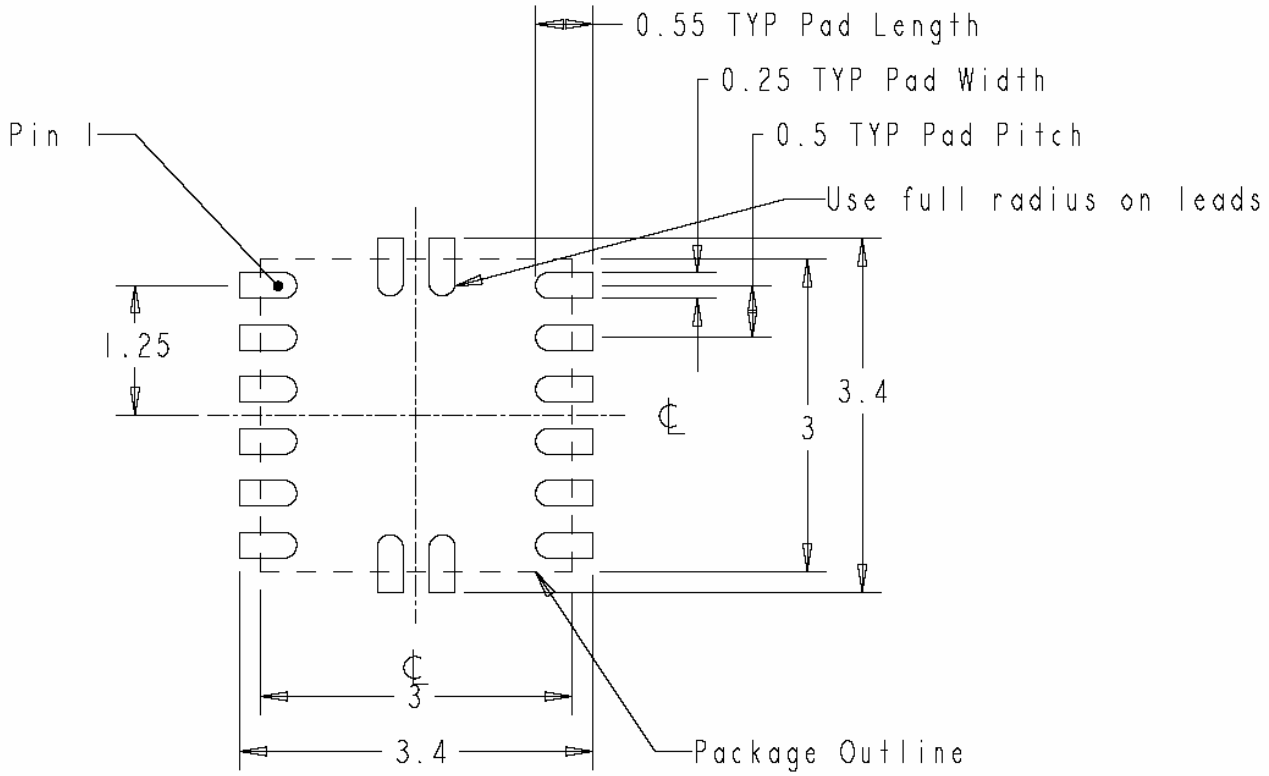


Figure 11. EP53A8xQI PCB Footprint (Top View)

Package and Mechanical

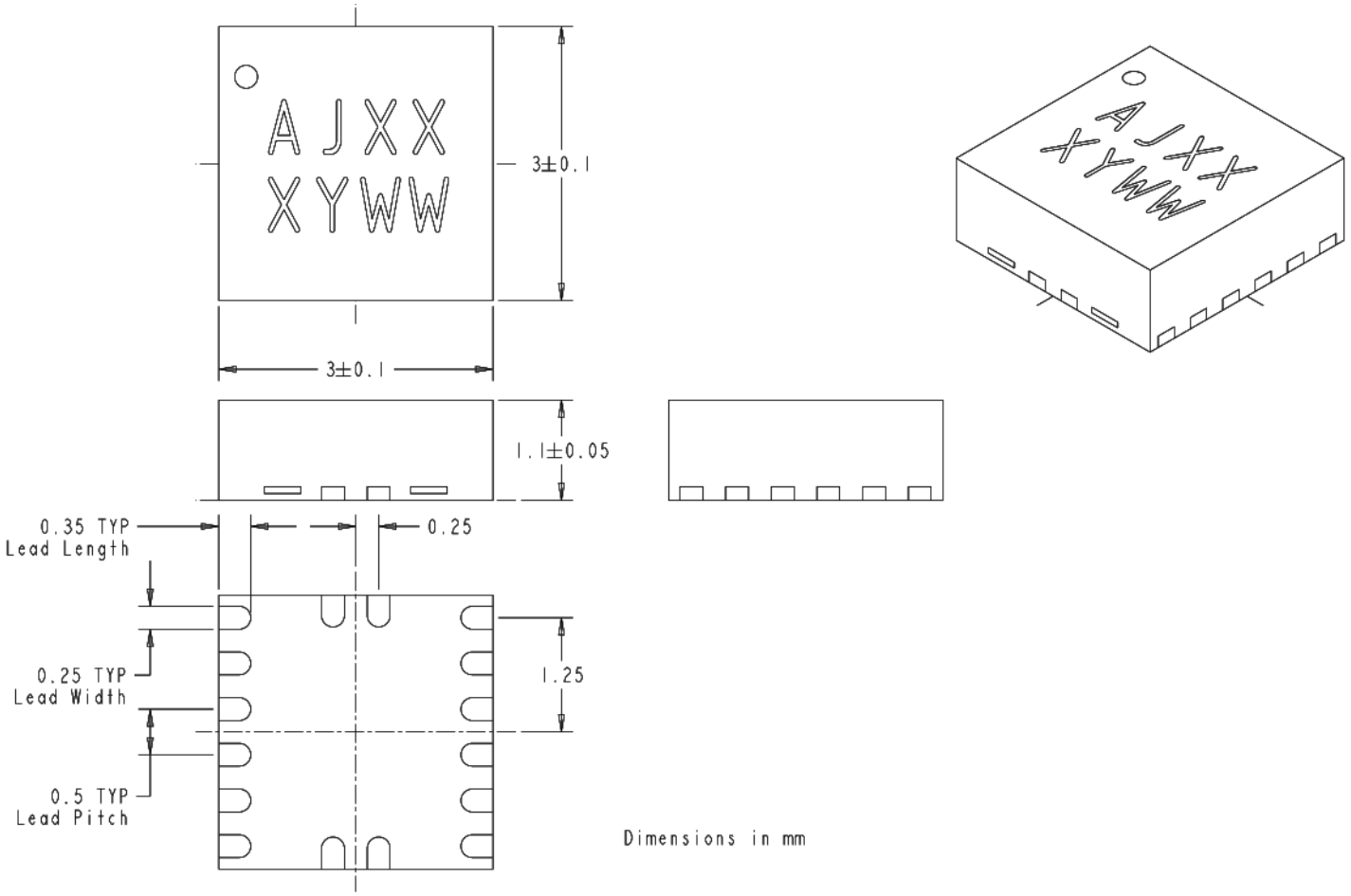


Figure 12. EP53A8LQI Package Dimensions (Bottom View)

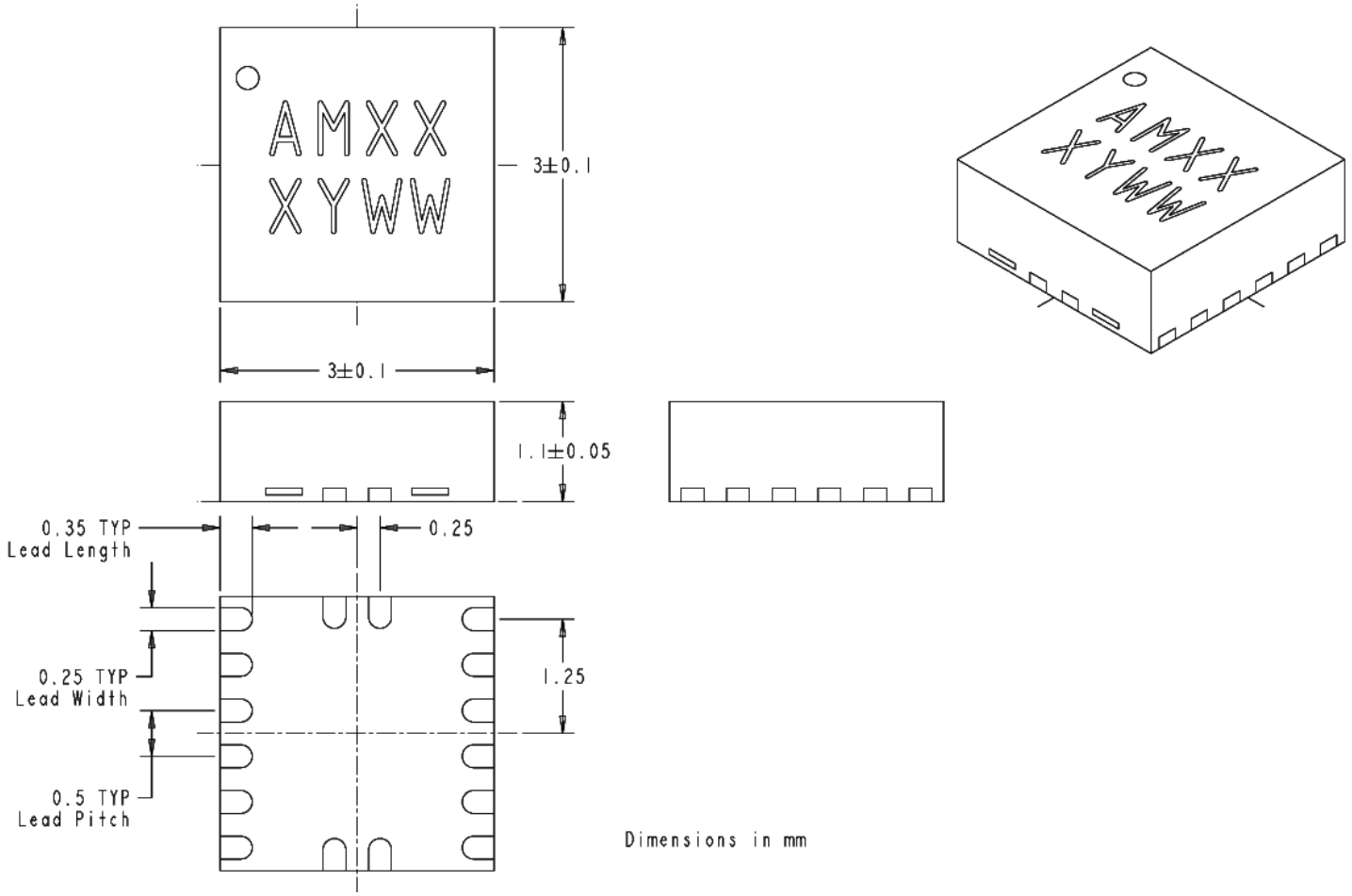


Figure 13. EP53A8HQI Package Dimensions (Bottom View)

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Contact Information

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
Phone: 408-544-7000
www.altera.com