

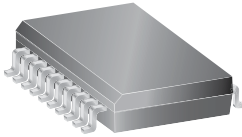
## 8-Channel Source Driver

### Features and Benefits

- TTL, DTL, PMOS, or CMOS compatible inputs
- 500 mA output source current capability
- Transient-protected outputs
- Output breakdown voltage to 50 V
- DIP or SOIC packaging

### Package: 20-pin SOICW (suffix LW)

*Not to scale*



(drop-in replacement for discontinued 18-pin SOIC variants)

### Description

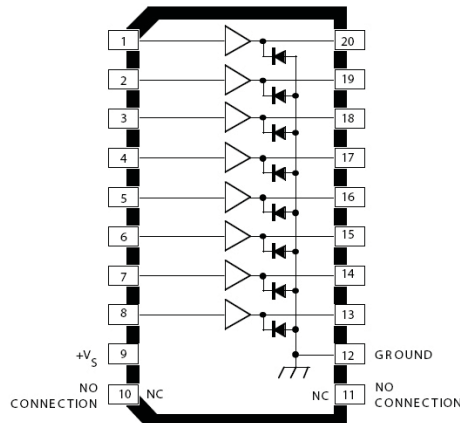
Recommended for high-side switching applications that benefit from separate logic and load grounds, these devices encompass load supply voltages to 50 V and output currents to -500 mA. These 8-channel source drivers are useful for interfacing between low-level logic and high-current loads. Typical loads include relays, solenoids, lamps, stepper and/or servo motors, print hammers, and LEDs.

All devices may be used with 5 V logic systems—TTL, Schottky TTL, DTL, and 5 V CMOS. The device packages offered are electrically interchangeable, and will withstand a maximum output off voltage of 50 V, and operate to a minimum of 5 V. All devices in this series integrate input current limiting resistors and output transient suppression diodes, and are activated by an active high input.

The package is a 20-pin wide-body SOIC with improved thermal characteristics compared to the 18-pin SOIC version it replaces (100% pin-compatible electrically).

The package is lead (Pb) free, with 100% matte-tin leadframe plating.

### Simplified Block Diagram



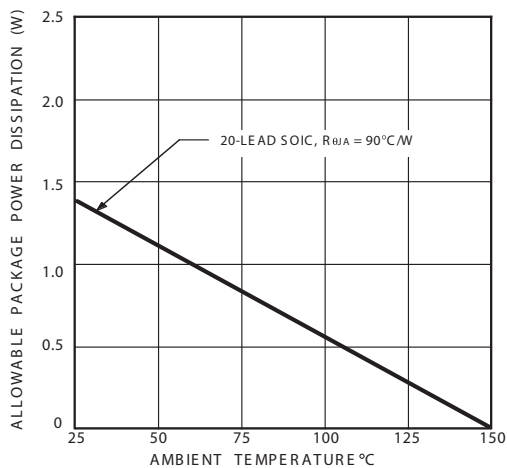
(NC pins, 10 and 11, not present on discontinued 18-pin LW package)

## Selection Guide

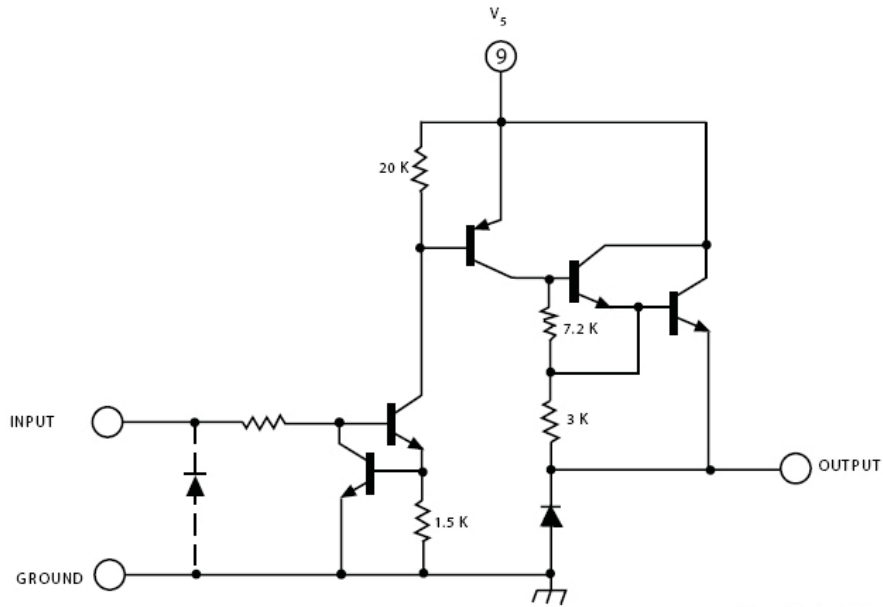
Part Number	Package	Packing	Ambient Temperature $T_A$ (°C)
A2982SLWTR-T	20-pin SOICW	1000 per reel	-20 to 85

## Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Output Voltage Range	$V_{CE}$		5 to 50	V
Input Voltage	$V_{IN}$		20	V
Output Current	$I_{OUT}$		-500	mA
Package Power Dissipation	$P_D$	See graph	-	-
Operating Ambient Temperature	$T_A$	Range S	-20 to 85	°C
Maximum Junction Temperature	$T_J(max)$		150	°C
Storage Temperature	$T_{stg}$		-55 to 150	°C

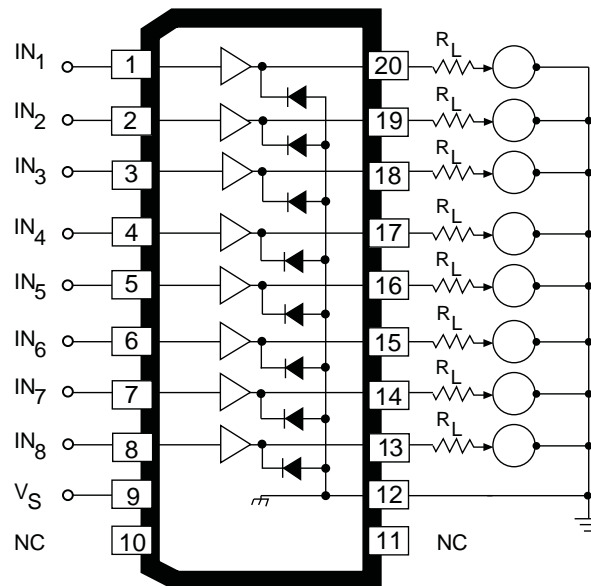


One of Eight Drivers



Dwg. No. A-10,242USA

Typical electroensitive printer application



Pins 10 and 11 can float; other pins match discontinued 18-pin SOIC: 1 to 9 same, pins 12 to 20 match pins 10 to 18

**ELECTRICAL CHARACTERISTICS<sup>1,2</sup> at  $T_A = +25^\circ\text{C}$  (unless otherwise specified).**

Characteristic	Symbol	Test Conditions	Test Fig.	Min.	Typ.	Max.	Units
Output Leakage Current <sup>3</sup>	$I_{CEX}$	$V_{IN} = 0.4\text{ V}, V_S = 50\text{ V}$	1	—	—	20	$\mu\text{A}$
Output Sustaining Voltage	$V_{CE(SUS)}$	$I_{OUT} = -45\text{ mA}$	—	35	—	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$V_{IN} = 2.4\text{ V}, I_{OUT} = -100\text{ mA}$	2	—	1.6	1.8	V
		$V_{IN} = 2.4\text{ V}, I_{OUT} = -225\text{ mA}$	2	—	1.7	1.9	V
		$V_{IN} = 2.4\text{ V}, I_{OUT} = -350\text{ mA}$	2	—	1.8	2.0	V
Input Current	$I_{IN(ON)}$	$V_{IN} = 2.4\text{ V}$	3	—	140	200	$\mu\text{A}$
		$V_{IN} = 12\text{ V}$	3	—	1.25	1.93	mA
Output Source Current (Outputs Open)	$I_{OUT}$	$V_{IN} = 2.4\text{ V}, V_{CE} = 2.0\text{ V}$	2	-350	—	—	mA
Supply Current Leakage Current	$I_S$	$V_{IN} = 2.4\text{ V}^*, V_S = 50\text{ V}$	4	—	—	10	mA
Clamp Diode Current	$I_R$	$V_R = 50\text{ V}, V_{IN} = 0.4\text{ V}^*$	5	—	—	50	$\mu\text{A}$
Clamp Diode Forward Voltage	$V_F$	$I_F = 350\text{ mA}$	6	—	1.5	2.0	V
Turn-On Delay	$t_{ON}$	$0.5 E_{IN}$ to $0.5 E_{OUT}$ , $R_L = 100\Omega, V_S = 35\text{ V}$	—	—	0.3	2.0	$\mu\text{s}$
Turn-Off Delay <sup>4</sup>	$t_{OFF}$	$0.5 E_{IN}$ to $0.5 E_{OUT}$ , $R_L = 100\Omega, V_S = 35\text{ V}$ , See Note	—	—	2.0	10	$\mu\text{s}$

<sup>1</sup>Negative current is defined as coming out of (sourcing) the specified device terminal.

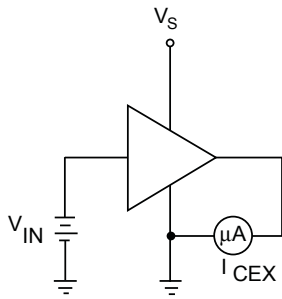
<sup>2</sup>All unused inputs must be connected to ground. Pull-down resistors (approximately 10 k $\Omega$ ) are recommended for inputs that are allowed to float while power is being applied to  $V_S$ .

<sup>3</sup>All inputs simultaneously.

<sup>4</sup>Turn-off delay is influenced by load conditions. Systems applications well below the specified output loading may require timing considerations for some designs, i.e., multiplexed displays or when used in combination with sink drivers in a totem pole configuration.

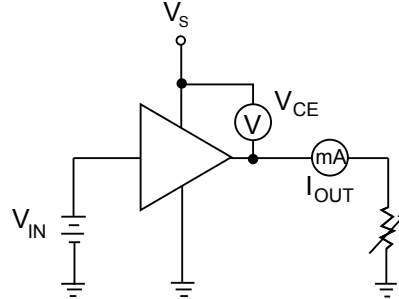
TEST FIGURES

Figure 1



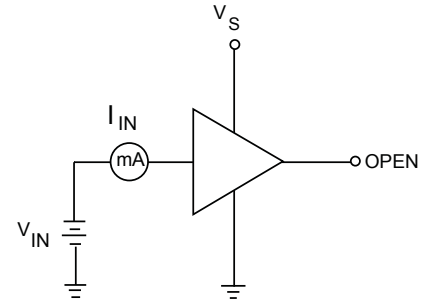
Dwg. No. A-11,083

Figure 2



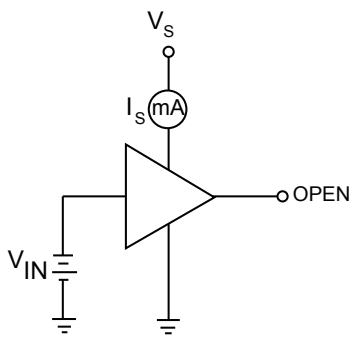
Dwg. No. A-11,084

Figure 3



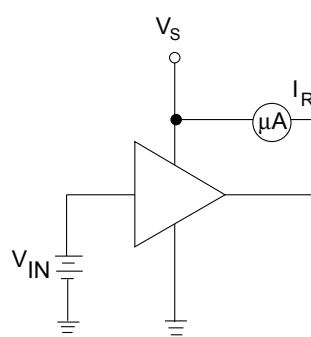
Dwg. No. A-11,085

Figure 4



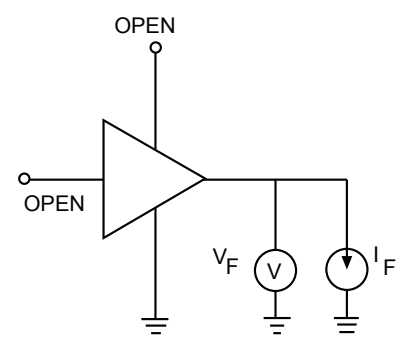
Dwg. No. A-11,086

Figure 5



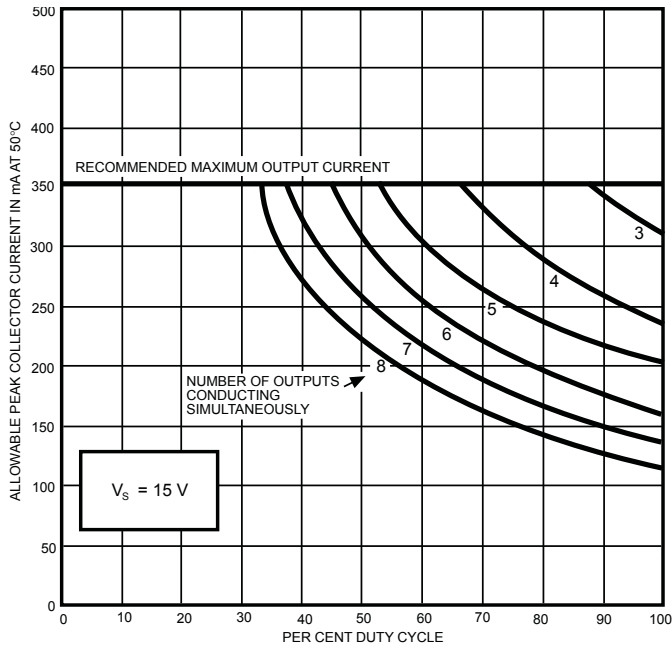
Dwg. No. A-11,087

Figure 6

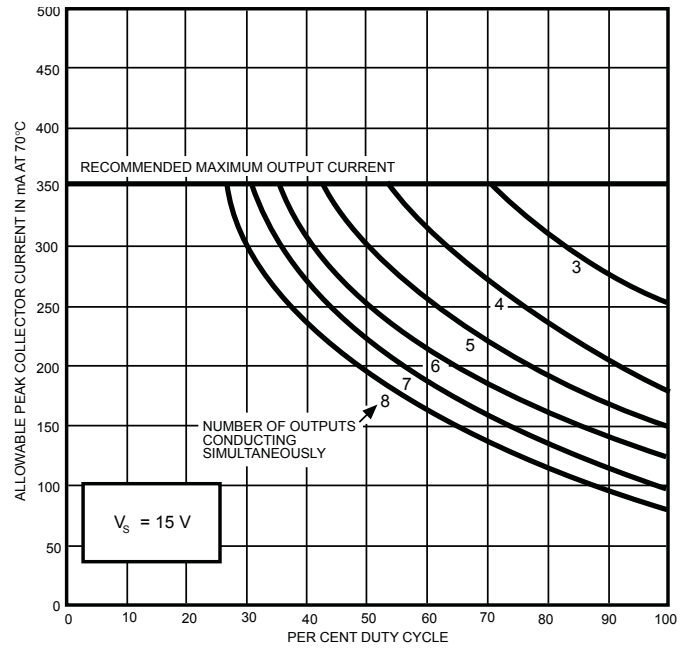


Dwg. No. A-11,088

Allowable peak collector current as a function of duty cycle

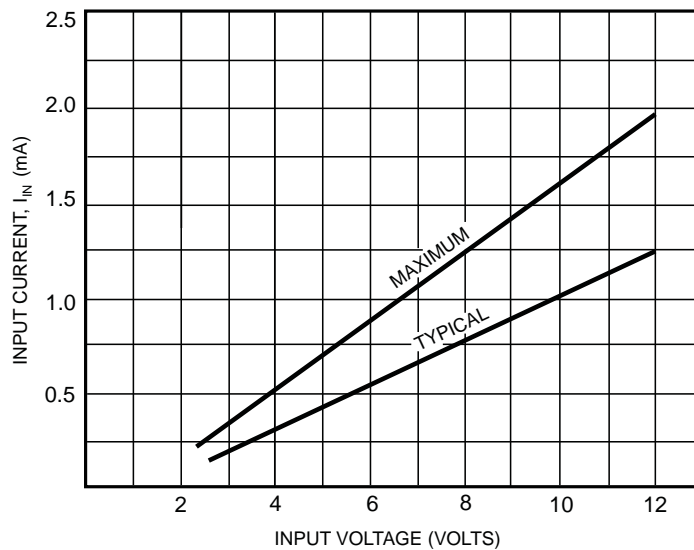


Dwg. No. A-11,107B



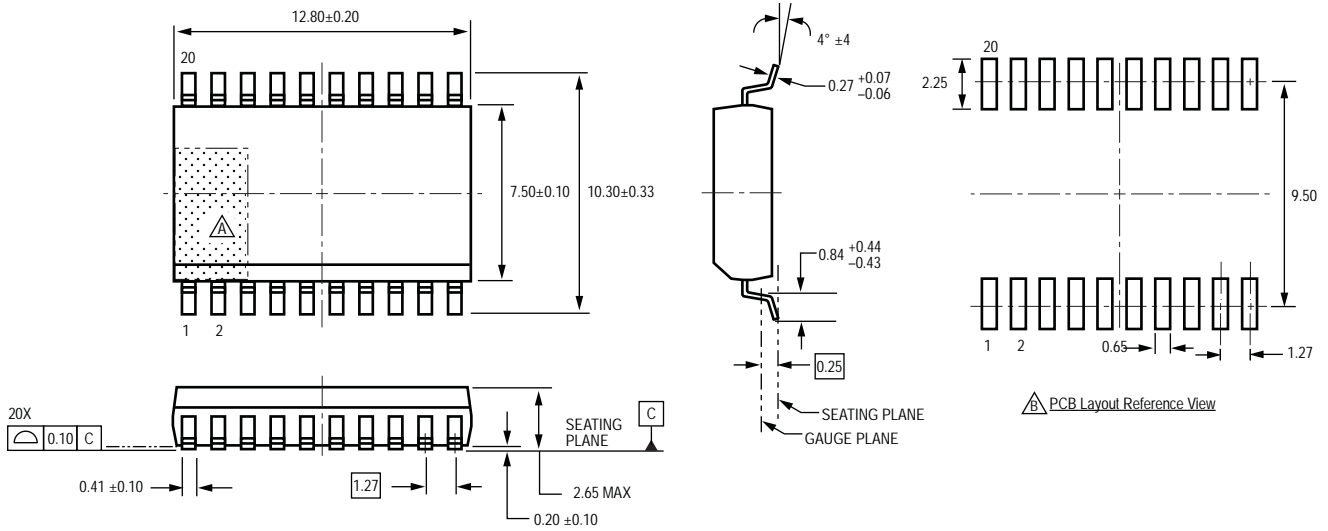
Dwg. No. A-11,108B

Input current as a function of input voltage



Dwg. No. A-11,115B

LW Package, 20-Pin SOICW



For Reference Only  
 Dimensions in millimeters  
 (Reference JEDEC MS-013 AC)  
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
 Exact case and lead configuration at supplier discretion within limits shown

△ Terminal #1 mark area  
 △ Reference pad layout (reference IPC SOIC127P1030X265-20M)  
 All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

**Revision History**

Revision	Revision Date	Description of Revision
Rev. U	April 30, 2012	Update product availability

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