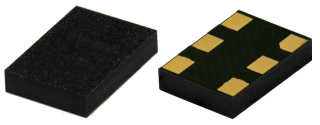
Ultra-Low Phase Jitter SMD Clock Oscillator



7.0 x 5.0 x 1.4mm

ASVMX

ESD Sensitive

RoHS/RoHS II compliant

Moisture Sensitivity Level – MSL 3

FEATURES:

- Excellent integrated phase jitter
- ±50ppm total frequency stability over -40°C to +85°C temperature range
- Output Type: LVCMOS, LVDS, LVPECL, HCSL
- Industry standard 6-Pin 7 x 5mm LGA package

APPLICATIONS:

- Fiber Channel 10G/12G SERDES
- 10/40/400 Gigabit Ethernet
- PCI-Express
- Storage
- Communications
- Backplane reference clock
- FPGA

KEY ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Item	Minimum	Maximum	Unit	Condition
Supply Voltage	-0.3	+3.6	V	
Storage Temp.	-55	+125	°C	
Lead Temp.(soldering, 10s)		+260	°C	
ESD (HBM)		2	kV	

Common Key Electrical Specifications – LVCMOS, LVPECL, LVDS, HCSL

Parameters	Minimum	Typical	Maximum	Units	Notes
Frequency	Please see Table 1- Frequency Code for available frequencies				
Output Type	LVCMOS, LVPECL, LVDS, HCSL				
Operating Temperature (T_A)	-40		+85	°C	
Overall Frequency Stability [1]	-50		+50	ppm	
Supply Voltage (V_{DD})	+2.375		+3.63	V	

Key Electrical Specifications – LVCMOS

V_{DD} = 2.375 - 3.63V, T_A = -40°C to +85°C, output terminated with 50 Ohms to VDD/2.[2]

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current (I_{DD})				95	mA	
Output Logic Level	V_{OH}	V_{DD} -0.8			V	
	V_{OL}			0.6	V	
Start-up time (T_{start})				20	ms	
Rise Time (Tr)		100		500	ps	No load 20% to 80%
Fall Time (Tf)		100		500	ps	
Duty Cycle		45		55	%	
RMS Phase Noise		Frequency dependent				

Key Electrical Specifications – LVPECL

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, outputs terminated with 50 Ohms to VDD - 2.[2]

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current (I_{DD})				120	mA	
Output Logic Level	V_{OH}	V_{DD}-1.35	V_{DD}-1.01	V_{DD}-0.8	V	
	V_{OL}	V_{DD}-2.0	V_{DD}-1.78	V_{DD}-1.6	V	
Peak to Peak Output Swing (V_{swing})		0.65	0.77	0.95	V	Single ended
Start-up Time				20	ms	
Rise Time (Tr)		85		350	ps	RL=50Ω , CL=0pF 20% to 80%
Fall Time (Tf)		85		350		
Duty Cycle		45		55	%	
RMS Phase Jitter		Frequency dependent				

FOL

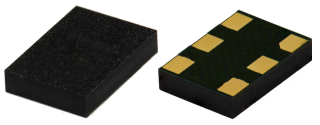
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KEY ELECTRICAL SPECIFICATIONS (Continued)

Key Electrical Specifications – LVDS

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, outputs terminated with 100 Ohms between Q and /Q.(2)

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current (I_{DD})				90	mA	
Common Mode Output Voltae (V_{CM})		1.125	1.2	1.375	V	
Output Differential Voltage (V_{OD})		247	350	454	mV	
Output Logic Level	V_{OH}	1.248	1.375	1.602	V	V_{OH} max = V_{CM} max + ½ V_{OD} max
	V_{OL}	0.898	1.025	1.252	V	V_{OH} min = V_{CM} min - ½ V_{OD} max
Start-up Time				20	ms	
Rise Time (Tr)		100		400	ps	RL=100Ω , CL=0pF 20% to 80%
Fall Time (Tf)		100		400		
Duty Cycle		45		55	%	
RMS Phase Jitter		Frequency dependent				

Key Electrical Specifications – HCSL

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, outputs terminated with 50 Ohms to VDD - 2.(2)

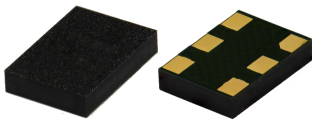
Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current (I_{DD})				95	mA	
Output Logic Level	V_{OH}	640	700	850	mV	
	V_{OL}	-150	0	27	mV	
Start-up Time				20	ms	
Rise Time (Tr)		150		450	ps	
Fall Time (Tf)		150		450		
Duty Cycle		45		55	%	
RMS Phase Jitter		Frequency dependent				

Notes:

1. Inclusive of initial accuracy, temperature drift, aging, shock, vibration from -40°C to +85°C.
2. Guaranteed after thermal equilibrium

EOL

Ultra-Low Phase Jitter SMD Clock Oscillator



7.0 x 5.0 x 1.4mm

ASVMX

ESD Sensitive

RoHS/RoHS II compliant

Moisture Sensitivity Level – MSL 3

PART IDENTIFICATION

ASVMX-[ ]MHz-[ ][ ][ ][ ]-[ ]

Output Frequency (See Notes)
See **Table 1** for developed frequencies.
e.g. 156.250 for 156.250MHz
83.333333 for 83.333333MHz

Frequency Code
See **Table 1** for frequency codes and the corresponding developed frequencies

Overall Frequency Stability
B: ±50ppm over -40°C ~ +85°C for OE= Pin 1
N: ±50ppm over -40°C ~ +85°C for OE= Pin 2

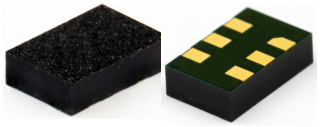
Output Format Code
See **Table 2** for output format codes

Packaging
Blank: Bulk or Tube
T: Tape & Reel

Table 1 – Frequency Codes vs. Developed Frequencies

Developed Frequencies	Frequency Codes						
	3E	3D	3A	3N	3B	3L	3S
	687.5	833.33333	814.58334	777.6	781.25	742.5	741.75824
	593.75	666.66667	779.16667	622.08	625	594	593.406592
	437.5	533.33333	743.75001	388.8	390.625	495	494.505493
	343.75	416.66667	708.33333	311.04	312.5	371.25	370.87912
	218.75	333.33333	672.91667	194.4	195.3125	297	296.703296
	125	266.66667	637.50001	155.52	156.25	247.5	247.252746
	93.75	166.66667	602.08334	77.76	78.125	198	197.802197
	62.5	133.33333	566.66667	38.88	39.0625	185.625	185.43956
	31.25	83.333333	531.25			148.5	148.351648
		66.666666	495.83334			123.75	123.626373
		33.333333	425			99	98.9010987
			389.58334			92.8125	92.71978
			354.16667			74.25	74.1758240
			318.75			61.875	61.8131867
			283.33334			59.4	59.3406592
			247.91667			49.5	49.4505493
			212.5			46.40625	37.087912
			177.08334			37.125	29.6703296
			141.66667			29.7	
			106.25				
			70.833334				
			53.125				
			35.416667				

SOL



7.0 x 5.0 x 1.4mm

PART IDENTIFICATION

Table 1 – Frequency Codes vs. Developed Frequencies (continued)

Developed Frequencies	Frequency Codes			
	4E	4J	4B	5A
	840	860.16	805.6640625	850
	760	573.44	684.8144531	800
	680	491.52	644.53125	750
	640	430.08	402.8320313	650
	560	286.72	322.265625	600
	520	245.76	201.4160156	550
	480	163.84	161.1328125	500
	440	143.36	80.5664063	450
	360	122.88	40.2832	400
	320	81.92		350
	280	61.44		300
	240			250
	160			200
	120			150
	80			100
	60			50
	40			25

Note: 1. For LVCMOS output, max. output frequency is 250MHz
2. Please contact Abracon for frequencies not listed in the above table.

Table 2 – Output Format Codes

Output Format Codes	Pinout Description	
A: LVPECL B: LVDS C: LVCMOS D: HCSL	Pin #1 = O/E Active High, Pullup (50kΩ) Pin #2 = NC Pin #3 = GND	Pin #4 = Q Pin # 5 = /Q Pin #6 = Vcc
F: LVPECL G: LVDS H: LVCMOS J: HCSL	Pin #1 = O/E Active Low, Pulldown (50kΩ) Pin #2 = NC Pin #3 = GND	Pin #4 = Q Pin # 5 = /Q Pin #6 = Vcc
L: LVPECL M: LVDS N: LVCMOS P: HCSL	Pin #1 = NC Pin #2 = O/E Active Low, Pulldown (50kΩ) Pin #3 = GND	Pin #4 = Q Pin # 5 = /Q Pin #6 = Vcc
R: LVPECL S: LVDS T: LVCMOS U: HCSL	Pin #1 = NC Pin #2 = O/E Active High, Pullup (50kΩ) Pin #3 = GND	Pin #4 = Q Pin # 5 = /Q Pin #6 = Vcc

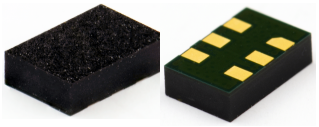
NOT FOR NEW DESIGN

Ultra-Low Phase Jitter SMD Clock Oscillator

ASVMX

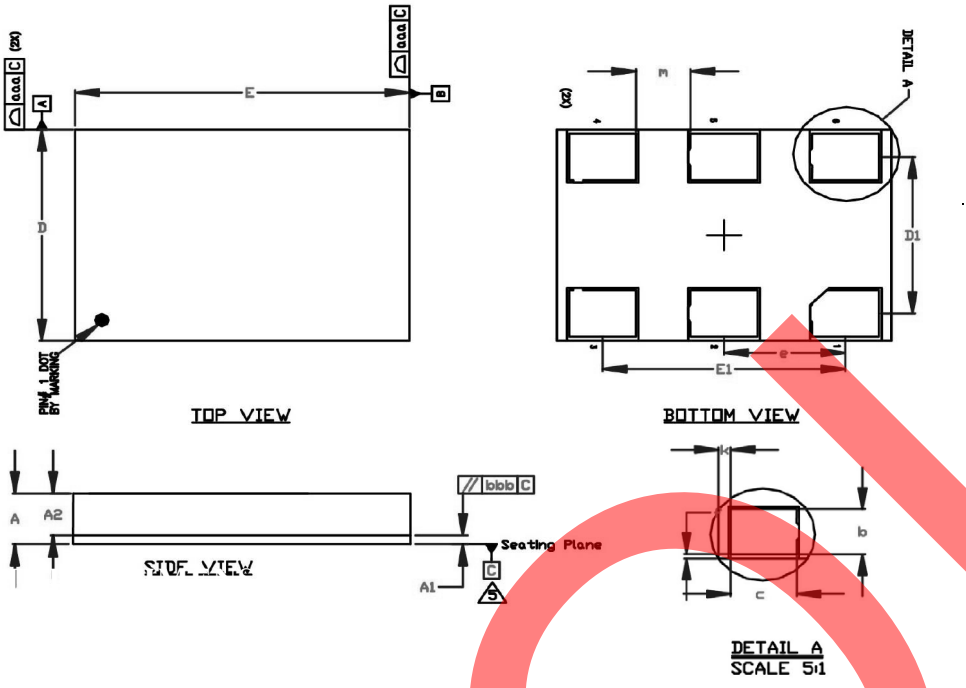
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RoHS/RoHS II compliant

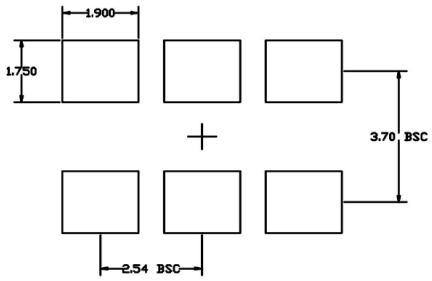


7.0 x 5.0 x 1.4mm

OUTLINE DIMENSION:



Recommended Land Pattern



Ref.	Min.	Nom.	Max.
A	1.260	1.330	1.400
A1	0.190	0.230	0.270
A2	1.070	1.100	1.130
D	4.900	5.000	5.100
D1		3.700 BSC	
E	6.900	7.000	7.100
E1		5.080 BSC	
b	1.050	1.100	1.150
c	1.350	1.400	1.450
e		2.540 BSC	
f	0.050	0.100	0.150
k	0.210	0.260	0.310
m	1.090	1.140	1.190
n		36	

Dimensional Tolerance	
aaa	0.100
bbb	0.070

Dimensions: mm

EOL

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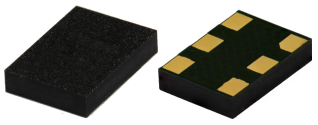
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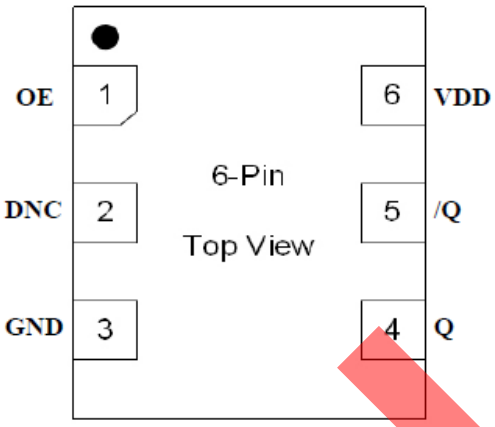
ASVMX

RoHS/RoHS II compliant



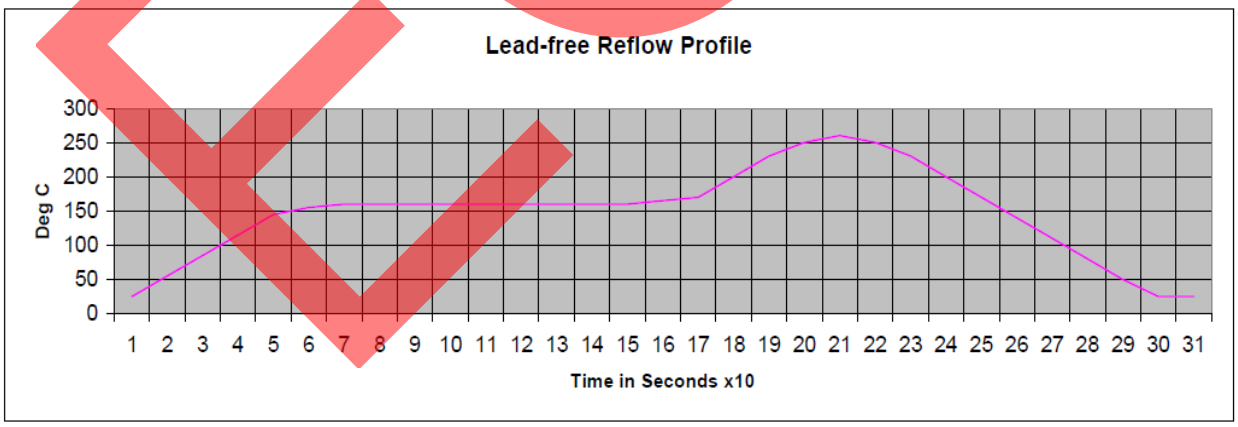
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PIN CONFIGURATION



Pin #	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVCMOS	Output Enable, disables output to tri-state.
	DNC			Make no connection, leave floating
2	DNC			Make no connection, leave floating
	OE	I, SE	LVCMOS	Output Enable, disables output to tri-state.
3	GND	PWR		Power Supply Ground
4	Q	O	LVCMOS/LVPECL/ LVDS/HCSL	Clock Output
5	DNC (for LVCMOS)			Make no connection, leave floating for LVCMOS output type
	/Q	O	LVPECL/ LVDS/HCSL	Complimentary Clock Output for differential output type
6	VDD	PWR		Power Supply

REFLOW PROFILE



Parameters	Specifications
Average Ramp-up Rate	3°C /second max.
Pre-Heat Temp 150 – 200°C	60 – 180 second
Temp > 217°C	60 – 150 second
Time @ Peak Temperature	20 – 40 second
Peak Temperature	260°C + 0°C / -5°C
Ramp-down Rate	-6°C / second max.
Time 25°C to Peak Temp.	8 minutes max.

PCN

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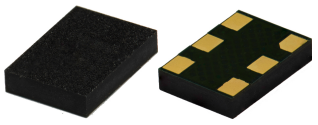
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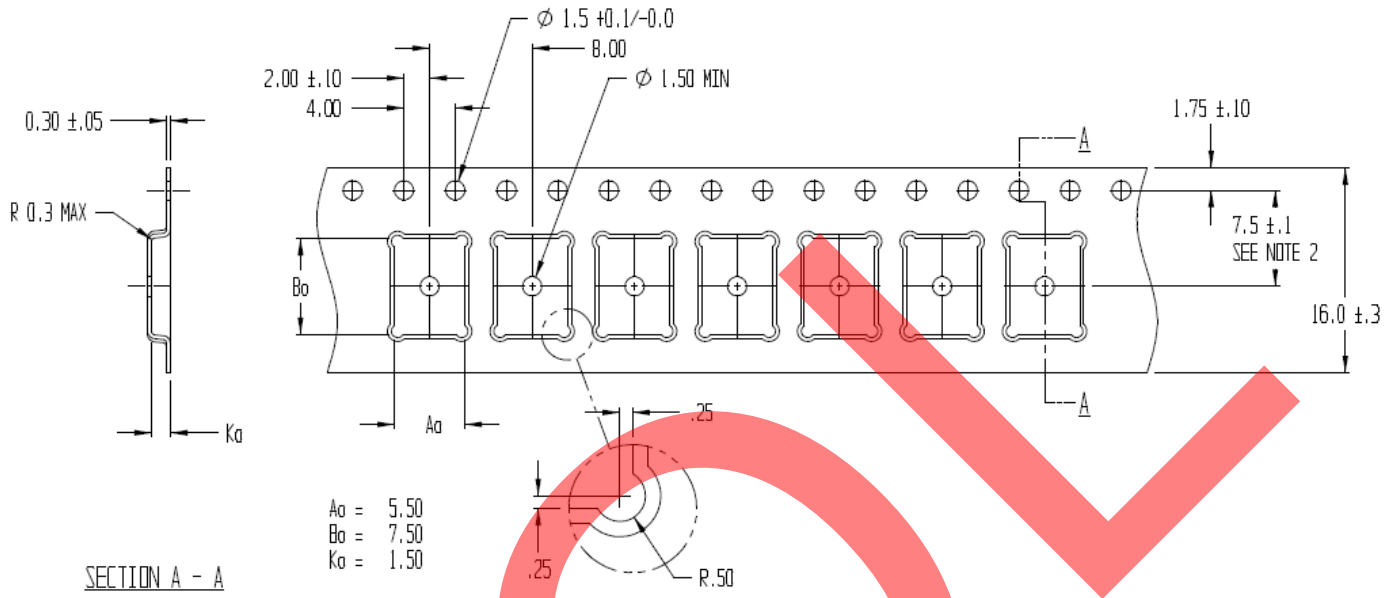


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TAPE & REEL

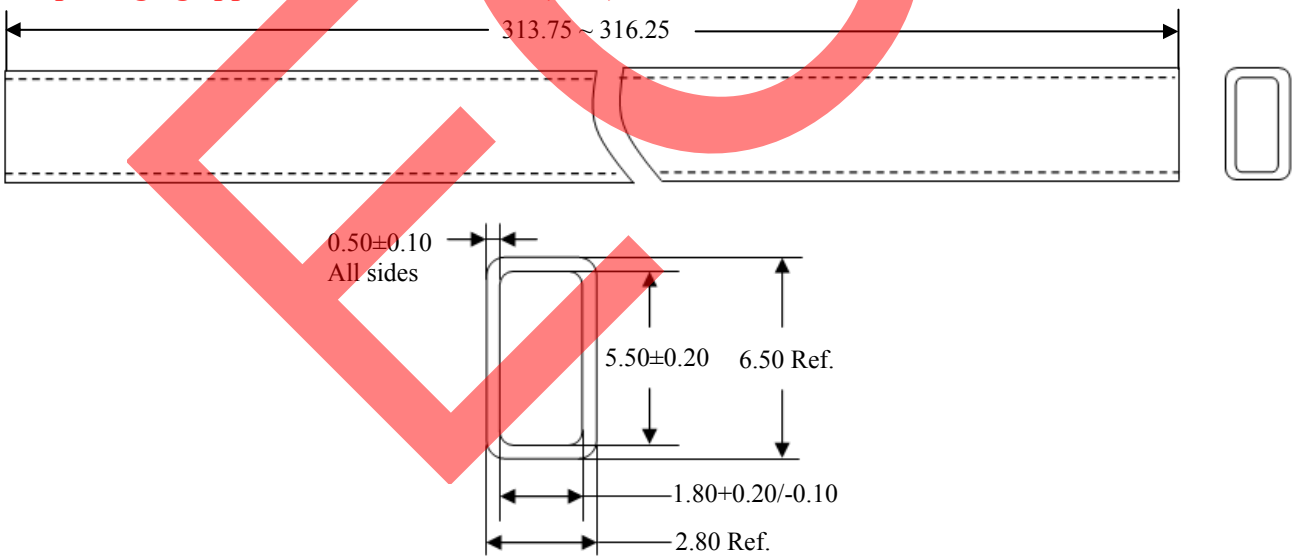
T= Tape & Reel, 1000pcs/reel. Reel Size = 7-inch Reel

MSL-3 packaging applies to –T option.



Blank = Bulk or Tube (43pcs/tube)

MSL-3 packaging applies to MOQ=43 units (tube)



Dimensions: mm

EOL

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