S-19316 Series

AUTOMOTIVE, 125°C OPERATION, 36 V INPUT, 40 mA VOLTAGE REGULATOR WITH INPUT MONITORING RESET FUNCTION

www.ablic.com

Rev.1.0_00

The S-19316 Series, developed by using high-withstand voltage CMOS process technology, is a positive voltage regulator with the reset function, which has high-withstand voltage and low current consumption.
Regarding a release signal output in the reset function, the S-19316 Series enables delay time adjustment by an external capacitor. Output form of the reset function is selectable from Nch open-drain output or CMOS output.

ABLIC Inc. offers a "thermal simulation service" which supports the thermal design in conditions when our power management ICs are in use by customers. Our thermal simulation service will contribute to reducing the risk in the thermal design at customers' development stage.
For more information regarding our thermal simulation service, contact our sales representatives.

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.

■ Features

Regulator block

- Output voltage: A type: 1.0 V to 5.3 V, selectable in 0.1 V step; B type: 1.8 V to 5.3 V, selectable in 0.1 V step
- Input voltage: 3.0 V to 36.0 V
- Output voltage accuracy: ±0.03 V (1.0 V ≤ $V_{OUT(S)}$ < 1.5 V, T_j = –40°C to +125°C); ±2.0% (1.5 V ≤ $V_{OUT(S)}$ ≤ 5.3 V, T_j = –40°C to +125°C)
- Dropout voltage: 240 mV typ. ($V_{OUT(S)}$ = 5.0 V, I_{OUT} = 30 mA)
- Output current: Possible to output 40 mA (1.0 V ≤ $V_{OUT(S)}$ < 2.0 V, V_{IN} ≥ 4.0 V)*1; Possible to output 40 mA (2.0 V ≤ $V_{OUT(S)}$ ≤ 5.3 V, V_{IN} = $V_{OUT(S)}$ + 2.0 V)*1
- Input and output capacitors: A ceramic capacitor can be used. (1.0 µF or more)
- Built-in overcurrent protection circuit: Limits overcurrent of output transistor
- Built-in thermal shutdown circuit: Detection temperature 160°C typ.

Detector block

- Detection voltage: 3.0 V to 11.3 V, selectable in 0.1 V step
- Operation voltage: A type: 1.8 V to 36.0 V; B type: 2.5 V to 36.0 V
- Detection voltage accuracy: ±2.0% (T_j = –40°C to +125°C)
- Hysteresis width selectable from "Available" / "Unavailable": "Available": 5.0% ≤ V_{HYS} ≤ 30.0% (T_j = –40°C to +125°C); "Unavailable": V_{HYS} = 0%
- Release delay time accuracy: ±20% (C_D = 3.3 nF, T_j = –40°C to +125°C)
- Output form: Nch open-drain output; CMOS output

Overall

- Current consumption: 2.2 µA typ. (T_j = –40°C to +125°C)
- Operation temperature range: Ta = –40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- Withstand 45 V load dump
- AEC-Q100 in process*2

*1. Please make sure that the loss of the IC will not exceed the power dissipation when the output current is large.
*2. Contact our sales representatives for details.

■ Applications

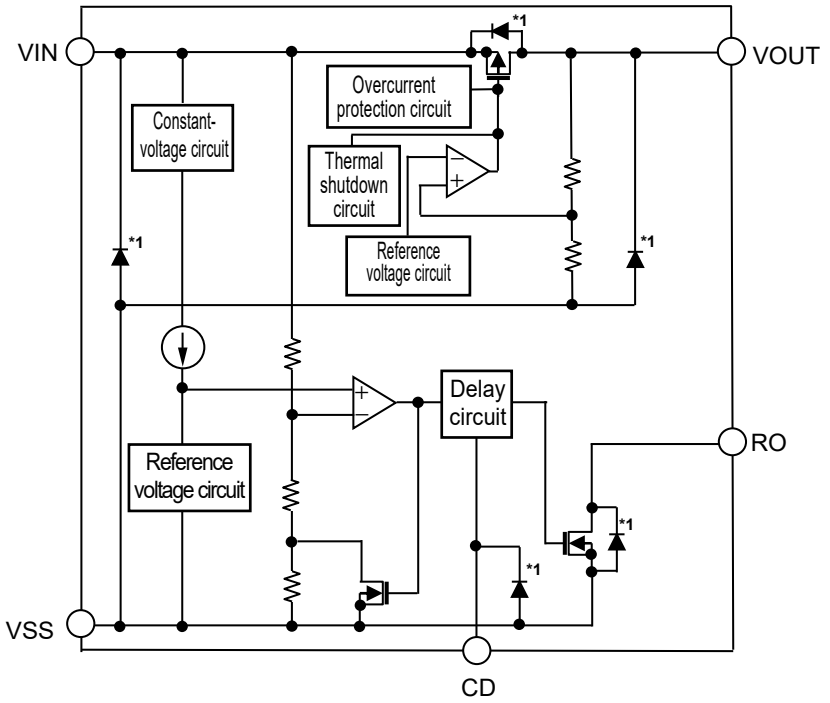
- Constant-voltage power supply and battery monitoring circuit for automotive electric component
- Power supply and battery monitoring circuit for low-current battery-powered device

■ Packages

- SOT-89-5
- HTMSOP-8
- SOT-23-5

■ Block Diagrams

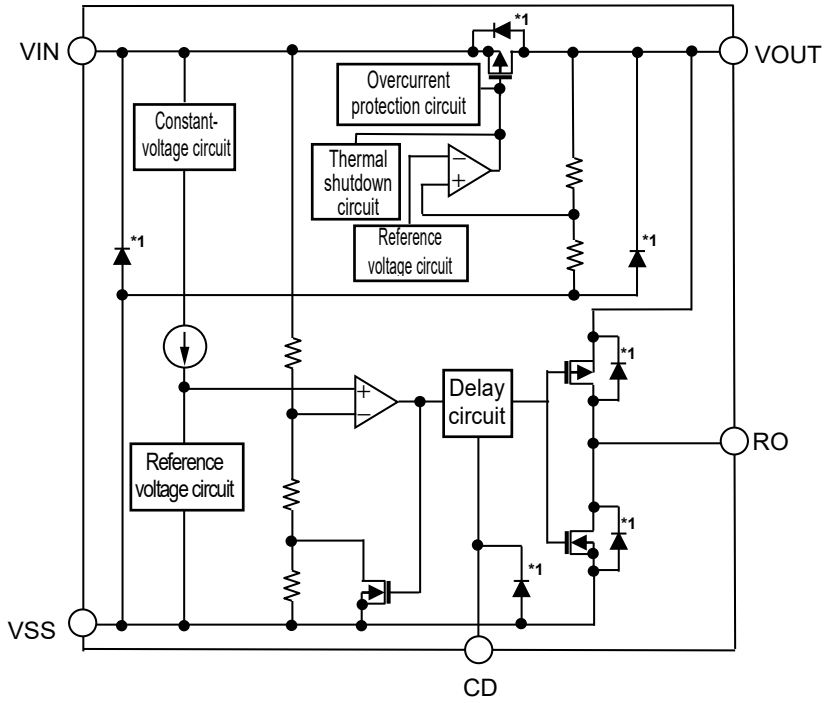
1. S-19316 Series A type



***1.** Parasitic diode

Figure 1

2. S-19316 Series B type



***1.** Parasitic diode

Figure 2

■ AEC-Q100 in Process

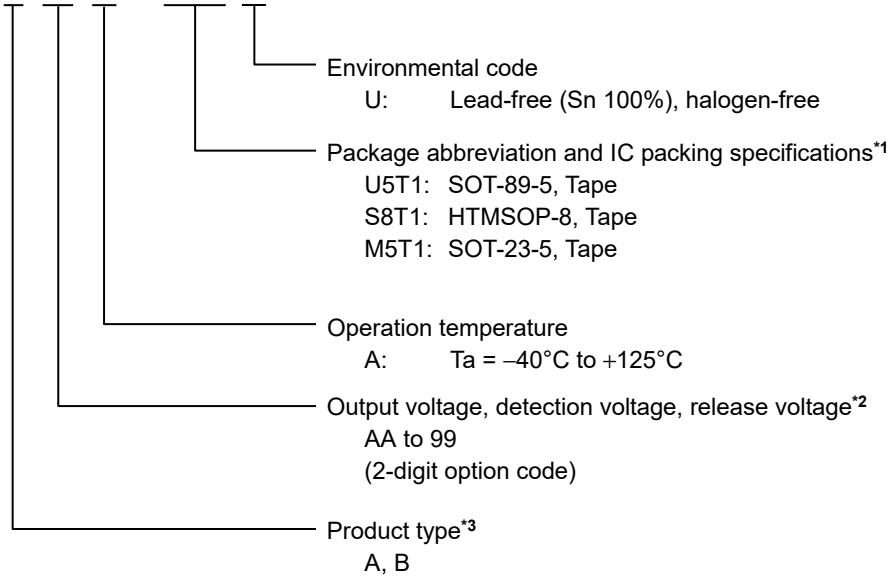
Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

Users can select the product type, output voltage, detection voltage, release voltage, and package type for the S-19316 Series. Refer to "**1. Product name**" regarding the contents of product name, "**3. Packages**" regarding the package drawings.

1. Product name

S-19316 x xx A - xxxx U 7



***1.** Refer to the tape drawing.
***2.** Contact our sales representatives for details on combination of output voltage, detection voltage, and release voltage.
***3.** Refer to "**2. Function list of product type**".

Remark 1. The output voltage (V_{OUT}) can be set in a range which satisfies the following conditions.
- Set output voltage ($V_{OUT(S)}$) is 100 mV step
- A type: $1.0\ V \le V_{OUT(S)} \le 5.3\ V$
  B type: $1.8\ V \le V_{OUT(S)} \le 5.3\ V$

2. The detection voltage ($-V_{DET}$) can be set in a range which satisfies the following conditions.
- Set detection voltage ($-V_{DET(S)}$) is 100 mV step
- $3.0\ V \le -V_{DET(S)} \le 11.3\ V$

3. The release voltage ($+V_{DET}$) can be set in a range which satisfies the following conditions. Release voltage possible setting range is shown in **Figure 3**.
- Set release voltage ($+V_{DET(S)}$) is 100 mV step
- $5.0\% \le V_{HYS} \le 30.0\%$

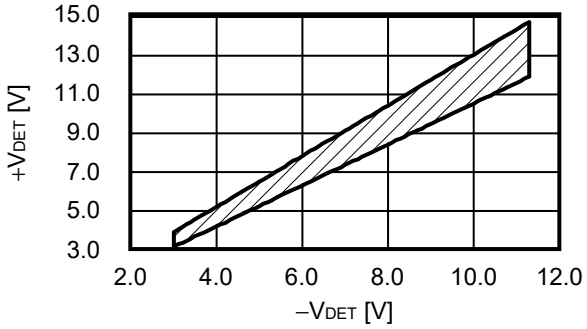


Figure 3 Release Voltage Possible Setting Area

If hysteresis width "Unavailable" was selected, $+V_{DET} = -V_{DET}$.

2. Function list of product type

Table 1

Product Type	RO Pin Output Form	RO Pin Output Logic
A	Nch open-drain output	Active "L"
B	CMOS output	Active "L"

3. Packages

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SOT-89-5	UP005-A-P-SD	UP005-A-C-SD	UP005-A-R-SD	–
HTMSOP-8	FP008-A-P-SD	FP008-A-C-SD	FP008-A-R-SD	FP008-A-L-SD
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD	–

■ Pin Configurations

1. SOT-89-5

Top view

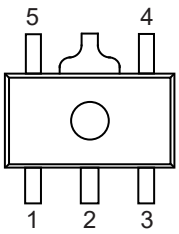


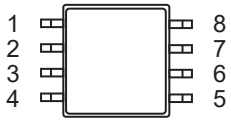
Figure 4

Table 3

Pin No.	Symbol	Description
1	CD	Connection pin for delay time adjustment capacitor
2	VSS	GND pin
3	VIN	Input voltage pin
4	VOUT	Output voltage pin
5	RO	Reset output pin

2. HTMSOP-8

Top view



Bottom view

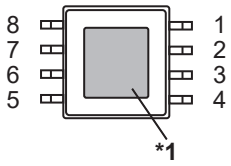


Figure 5

Table 4

Pin No.	Symbol	Description
1	NC*2	No connection
2	VOUT	Output voltage pin
3	RO	Reset output pin
4	NC*2	No connection
5	CD	Connection pin for delay time adjustment capacitor
6	VSS	GND pin
7	NC*2	No connection
8	VIN	Input voltage pin

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND. However, do not use it as the function of electrode.

***2.** The NC pin is electrically open.
The NC pin can be connected to the VIN pin or the VSS pin.

3. SOT-23-5

Top view

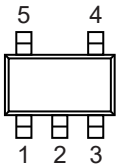


Figure 6

Table 5

Pin No.	Symbol	Description
1	RO	Reset output pin
2	VSS	GND pin
3	VOUT	Output voltage pin
4	VIN	Input voltage pin
5	CD	Connection pin for delay time adjustment capacitor

■ Absolute Maximum Ratings

Table 6

(Ta = +25°C unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
Input voltage		V_{IN}	V_{SS} – 0.3 to V_{SS} + 45.0	V
Output voltage		V_{OUT}	V_{SS} – 0.3 to V_{IN} + 0.3 ≤ V_{SS} + 7.0	V
RO pin voltage	Nch open-drain output	V_{RO}	V_{SS} – 0.3 to V_{SS} + 45.0	V
	CMOS output		V_{SS} – 0.3 to V_{OUT} + 0.3 ≤ V_{SS} + 7.0	V
CD pin voltage		V_{CD}	V_{SS} – 0.3 to V_{IN} + 0.3 ≤ V_{SS} + 7.0	V
Output current (Regulator block)		I_{OUT}	52	mA
Output current (Detector block)	Nch open-drain output	I_{RON}	20	mA
	CMOS output	I_{RON}	20	mA
		I_{ROP}	–20	mA
Junction temperature		T_j	–40 to +150	°C
Operation ambient temperature		T_{opr}	–40 to +125	°C
Storage temperature		T_{stg}	–40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 7

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SOT-89-5	Board A	–	119	–	°C/W
			Board B	–	84	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	46	–	°C/W
			Board E	–	35	–	°C/W
		HTMSOP-8	Board A	–	159	–	°C/W
			Board B	–	113	–	°C/W
			Board C	–	39	–	°C/W
			Board D	–	40	–	°C/W
			Board E	–	30	–	°C/W
		SOT-23-5	Board A	–	192	–	°C/W
			Board B	–	160	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Regulator block

Table 8

(T_j = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Output voltage*1	$V_{OUT(E)}$	V_{IN} = $V_{OUT(S)}$ + 2.0 V, I_{OUT} = 1 mA	1.0 V ≤ $V_{OUT(S)}$ < 1.5 V	$V_{OUT(S)}$ – 0.03	$V_{OUT(S)}$	$V_{OUT(S)}$ + 0.03	V	1
			1.5 V ≤ $V_{OUT(S)}$ ≤ 5.3 V	$V_{OUT(S)}$ × 0.98	$V_{OUT(S)}$	$V_{OUT(S)}$ × 1.02	V	1
Output current*2	I_{OUT}	V_{IN} = 4.0 V	1.0 V ≤ $V_{OUT(S)}$ < 2.0 V	40*4	–	–	mA	2
		V_{IN} = $V_{OUT(S)}$ + 2.0 V	2.0 V ≤ $V_{OUT(S)}$ ≤ 5.3 V	40*4	–	–	mA	2
Dropout voltage*3	V_{drop}	I_{OUT} = 30 mA	1.0 V ≤ $V_{OUT(S)}$ < 1.5 V	2.00	2.19	2.38	V	1
			1.5 V ≤ $V_{OUT(S)}$ < 2.0 V	1.50	1.73	1.95	V	1
			2.0 V ≤ $V_{OUT(S)}$ < 2.5 V	1.00	1.19	1.39	V	1
			2.5 V ≤ $V_{OUT(S)}$ < 3.0 V	0.50	0.66	0.82	V	1
			3.0 V ≤ $V_{OUT(S)}$ < 4.0 V	–	0.35	0.60	V	1
			4.0 V ≤ $V_{OUT(S)}$ ≤ 5.3 V	–	0.24	0.45	V	1
Line regulation	$\frac{\Delta V_{OUT1}}{\Delta V_{IN} \bullet V_{OUT}}$	$V_{OUT(S)}$ + 2.0 V ≤ V_{IN} ≤ 36.0 V, I_{OUT} = 1 mA		–	0.01	0.2	%/V	1
Load regulation	ΔV_{OUT2}	V_{IN} = 4.0 V, 1 μA ≤ I_{OUT} ≤ 30 mA	1.0 V ≤ $V_{OUT(S)}$ < 2.0 V	–	24	45	mV	1
		V_{IN} = $V_{OUT(S)}$ + 2.0 V, 1 μA ≤ I_{OUT} ≤ 30 mA	2.0 V ≤ $V_{OUT(S)}$ ≤ 5.3 V	–	24	45	mV	1
Input voltage	V_{IN}	–		3.0	–	36.0	V	–
Short-circuit current	I_{short}	V_{IN} = 4.0 V, V_{OUT} = 0 V	1.0 V ≤ $V_{OUT(S)}$ < 2.0 V	–	24	–	mA	2
		V_{IN} = $V_{OUT(S)}$ + 2.0 V, V_{OUT} = 0 V	2.0 V ≤ $V_{OUT(S)}$ ≤ 5.3 V	–	24	–	mA	2
Thermal shutdown detection temperature	T_{SD}	Junction temperature		–	160	–	°C	–
Thermal shutdown release temperature	T_{SR}	Junction temperature		–	135	–	°C	–

***1.** $V_{OUT(S)}$: Set output voltage
$V_{OUT(E)}$: Actual output voltage
Output voltage when fixing I_{OUT} (= 1 mA) and inputting $V_{OUT(S)}$ + 2.0 V

***2.** The output current at which the output voltage becomes 95% of $V_{OUT(E)}$ after gradually increasing the output current.

***3.** V_{drop} = V_{IN1} – (V_{OUT3} × 0.98)
V_{IN1} is the input voltage at which the output voltage becomes 98% of V_{OUT3} after gradually decreasing the input voltage.
V_{OUT3} is the output voltage when V_{IN} = 4.0 V (1.0 V ≤ $V_{OUT(S)}$ < 2.0 V), or V_{IN} = $V_{OUT(S)}$ + 2.0 V (2.0 V ≤ $V_{OUT(S)}$ ≤ 5.3 V), and I_{OUT} = 30 mA

***4.** Due to limitation of the power dissipation, this value may not be satisfied. Attention should be paid to the power dissipation when the output current is large.
This specification is guaranteed by design.

2. Detector block

Table 9

(T_j = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	–		$-V_{DET(S)} \times 0.98$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.02$	V	3
Release voltage*2	$+V_{DET}$	V_{HYS} = 0%		$-V_{DET(S)} \times 0.98$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.02$	V	3
		5.0% ≤ V_{HYS} ≤ 30.0%		$+V_{DET(S)} \times 0.98$	$+V_{DET(S)}$	$+V_{DET(S)} \times 1.02$	V	3
Operation voltage	V_{OPR}	S-19316 Series A type		1.8	–	36.0	V	–
		S-19316 Series B type		2.5	–	36.0	V	–
Output current "H"	I_{ROP}	CMOS output, V_{DS}*3 = 0.5 V	V_{IN} = 16.0 V	–	–	–0.68	mA	4
Output current "L"	I_{RON}	CMOS output, V_{DS}*3 = 0.5 V	V_{IN} = 2.5 V	2.50	–	–	mA	4
		Nch open-drain output, V_{DS}*3 = 0.5 V	V_{IN} = 2.5 V	2.80	–	–	mA	4
Leakage current	I_{LEAKN}	Nch open-drain output	V_{RO} = 36.0 V, V_{IN} = 36.0 V	–	–	2.0	µA	4
Detection response time*4	t_{RESET}	–		–	140	–	µs	5
Release response time*5	t_{DELAY}	C_D = 3.3 nF		8.0	10.0	12.0	ms	5

***1.** $-V_{DET(S)}$: Set detection voltage, $-V_{DET}$: Actual detection voltage

***2.** $+V_{DET(S)}$: Set release voltage, $+V_{DET}$: Actual release voltage

***3.** V_{DS}: Drain-to-source voltage of the output transistor

***4.** The time period from when the pulse voltage of $-V_{DET(S)}$ + 1.0 V → 2.5 V is applied to the VIN pin within 3.0 V ≤ $-V_{DET(S)}$ < 3.5 V or the pulse voltage of $-V_{DET(S)}$ + 1.0 V → $-V_{DET(S)}$ – 1.0 V is applied to the VIN pin within 3.5 V ≤ $-V_{DET(S)}$ ≤ 14.6 V until V_{RO} reaches 50% of either V_{IN} or V_{OUT}.

***5.** The time period from when the pulse voltage of 2.5 V → $+V_{DET(S)}$ + 1.0 V is applied to the VIN pin within 3.0 V ≤ $+V_{DET(S)}$ < 3.5 V or the pulse voltage of $+V_{DET(S)}$ – 1.0 V → $+V_{DET(S)}$ + 1.0 V is applied to the VIN pin within 3.5 V ≤ $+V_{DET(S)}$ ≤ 14.6 V until V_{RO} reaches 50% of either V_{IN} or V_{OUT}.

3. Overall

Table 10

(T_j = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Current consumption	I_{SS1}	V_{IN} = $V_{OUT(S)}$*1 + 2.0 V ($V_{OUT(S)}$ + 1.0 V ≥ $+V_{DET(S)}$*2), V_{IN} = $+V_{DET(S)}$ + 1.0 V ($V_{OUT(S)}$ + 1.0 V < $+V_{DET(S)}$), I_{OUT} = 0 mA	S-19316 Series A type	–	2.2	4.7	µA	6
			S-19316 Series B type	–	2.2	5.0	µA	6

***1.** $V_{OUT(S)}$: Set output voltage

***2.** $+V_{DET(S)}$: Set release voltage

■ Test Circuits

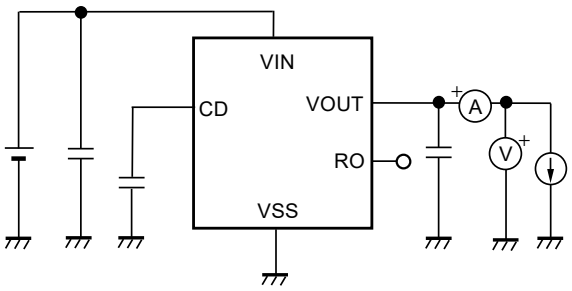


Figure 7 Test Circuit 1

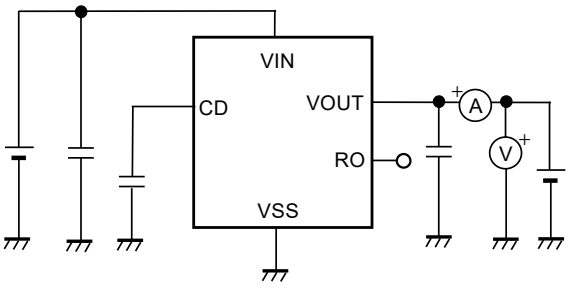


Figure 8 Test Circuit 2

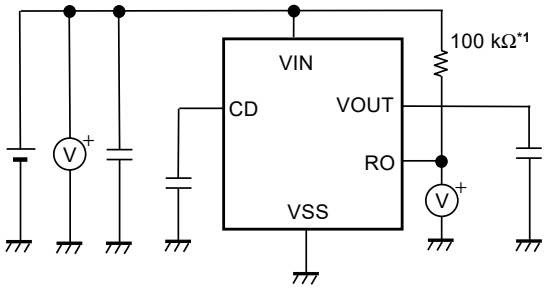


Figure 9 Test Circuit 3

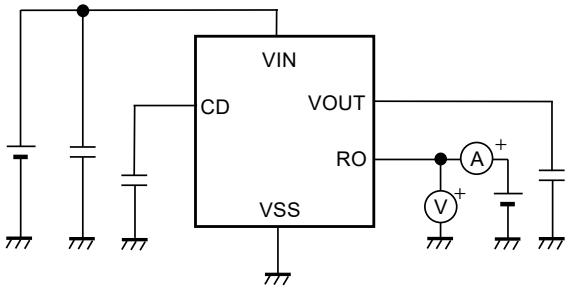


Figure 10 Test Circuit 4

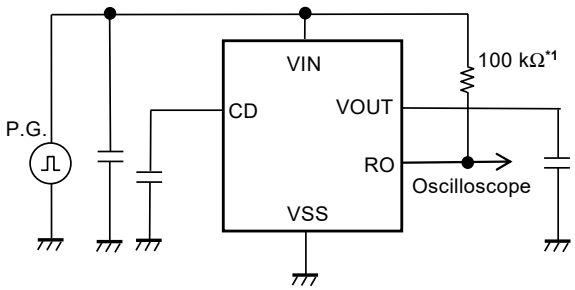


Figure 11 Test Circuit 5

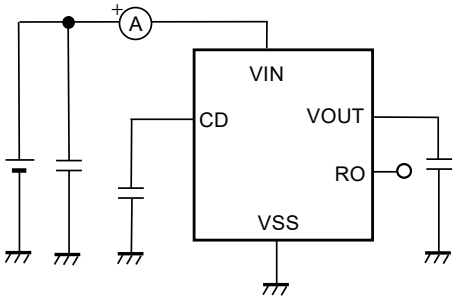
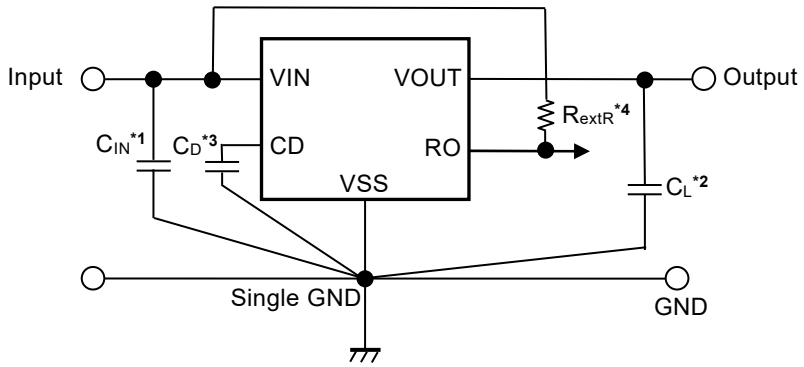


Figure 12 Test Circuit 6

1. Only S-19316 Series A type

■ Standard Circuit

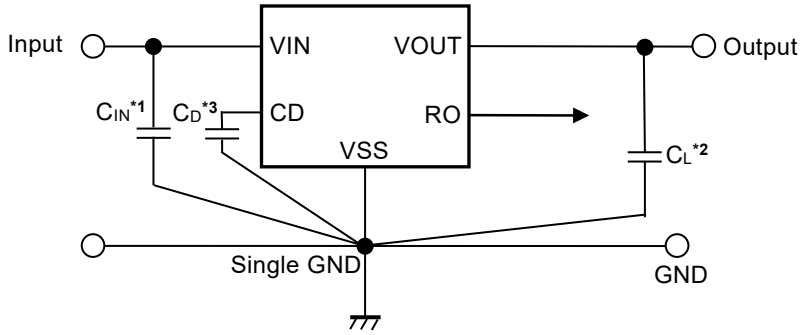
1. S-19316 Series A type



***1.** C_{IN} is a capacitor for stabilizing the input.
***2.** C_L is a capacitor for stabilizing the output.
***3.** C_D is the delay time adjustment capacitor.
***4.** R_{extR} is the external pull-up resistor for the reset output pin.

Figure 13

2. S-19316 Series B type



***1.** C_{IN} is a capacitor for stabilizing the input.
***2.** C_L is a capacitor for stabilizing the output.
***3.** C_D is the delay time adjustment capacitor.

Figure 14

Caution The above connection diagrams and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

■ Condition of Application

Input capacitor (C_{IN}): A ceramic capacitor with capacitance of 1.0 μF or more is recommended.
Output capacitor (C_L): A ceramic capacitor with capacitance of 1.0 μF or more is recommended.
Delay time adjustment capacitor (C_D): A ceramic capacitor with capacitance of 0.1 nF or more is recommended.

Caution Generally, in a voltage regulator, an oscillation may occur depending on the selection of the external parts. Perform thorough evaluation including the temperature characteristics with an actual application using the above capacitors to confirm no oscillation occurs.

■ Selection of Input Capacitor (C_{IN}) and Output Capacitor (C_L)

The S-19316 Series requires C_L between the VOUT pin and the VSS pin for phase compensation.
The operation is stabilized by a ceramic capacitor with capacitance of 1.0 μF or more. When using an OS capacitor, a tantalum capacitor or an aluminum electrolytic capacitor, the capacitance also must be 1.0 μF or more. However, an oscillation may occur depending on the equivalent series resistance (ESR).
Moreover, the S-19316 Series requires C_{IN} between the VIN pin and the VSS pin for a stable operation.
Generally, an oscillaiton may occur when a voltage regulator is used under the conditon that the impedance of the power supply is high.
Note that the output voltage (V_{OUT}) transient characteristics varies depending on the capacitance of C_{IN} and C_L and the value of ESR.

Caution Perform thorough evaluation including the temperature characteristics with an actual application to select C_{IN} and C_L.

■ Selection of Delay Time Adjustment Capacitor (C_D)

In the S-19316 Series, the delay time adjustment capacitor (C_D) is necessary between the CD pin and the VSS pin to adjust the release delay time (t_{DELAY}) of the detector. Refer to "**2. 2 Delay circuit**" of "**2. Detector block**" in "**■ Operation**" for details.

Caution Perform thorough evaluation including the temperature characteristics with an actual application to select C_D.

■ Explanation of Terms

1. Regulator block

1. 1 Low dropout voltage regulator

This is a voltage regulator which made dropout voltage small by its built-in low on-resistance output transistor.

1. 2 Output voltage (V_{OUT})

This voltage is output at an accuracy of ±2.0% or ±0.03 V[*2] when the input voltage, the output current and the temperature are in a certain condition[*1].

***1.** Differs depending on the product.
***2.** When $V_{OUT} < 1.5$ V: ±0.03 V, when $V_{OUT} \geq 1.5$ V: ±2.0%

Caution If the certain condition is not satisfied, the output voltage may exceed the accuracy range of ±2.0% or ±0.03 V. Refer to "1. Regulator block" in "■ Electrical Characteristics" and "1. Regulator block" in "■ Characteristics (Typical Data)" for details.

1. 3 Line regulation $\left(\frac{\Delta V_{OUT1}}{\Delta V_{IN} \bullet V_{OUT}}\right)$

Indicates the dependency of the output voltage against the input voltage. That is, the value shows how much the output voltage changes due to a change in the input voltage after fixing output current constant.

1. 4 Load regulation (ΔV_{OUT2})

Indicates the dependency of the output voltage against the output current. That is, the value shows how much the output voltage changes due to a change in the output current after fixing input voltage constant.

1. 5 Dropout voltage (V_{drop})

Indicates the difference between input voltage (V_{IN1}) and the output voltage when the output voltage becomes 98% of the output voltage value (V_{OUT3}) at V_{IN} = 4.0 V (1.0 V ≤ $V_{OUT(S)}$ < 2.0 V) or V_{IN} = $V_{OUT(S)}$ + 2.0 V (2.0 V ≤ $V_{OUT(S)}$ ≤ 5.3 V) after the input voltage (V_{IN}) is decreased gradually.

$V_{drop} = V_{IN1} - (V_{OUT3} \times 0.98)$

2. Detector block

2. 1 Detection voltage ($-V_{DET}$)

The detection voltage is a voltage at which the output of the RO pin turns to "L".
The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$ min.) and the maximum ($-V_{DET}$ max.) is called the detection voltage range (Refer to **Figure 15**, **Figure 17**).

2. 2 Release voltage ($+V_{DET}$)

The release voltage is a voltage at which the output of the RO pin turns to "H".
The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum ($+V_{DET}$ min.) and the maximum ($+V_{DET}$ max.) is called the release voltage range (Refer to **Figure 16**, **Figure 18**).

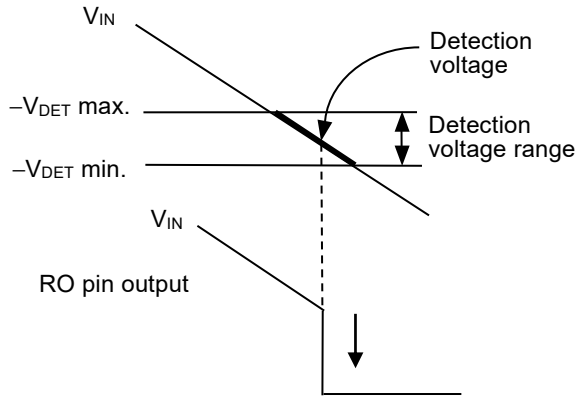


Figure 15 Detection Voltage (S-19316 Series A type)

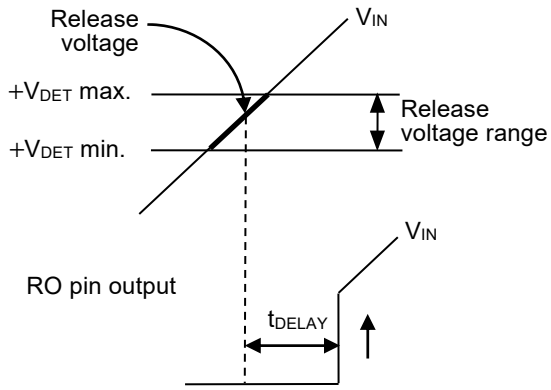


Figure 16 Release Voltage (S-19316 Series A type)

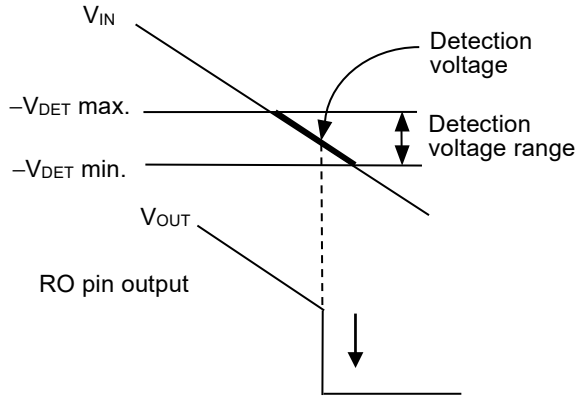


Figure 17 Detection Voltage (S-19316 Series B type)

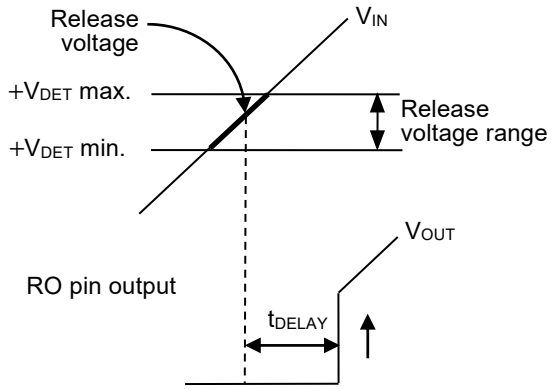


Figure 18 Release Voltage (S-19316 Series B type)

2. 3 Hysteresis width (V_{HYS})

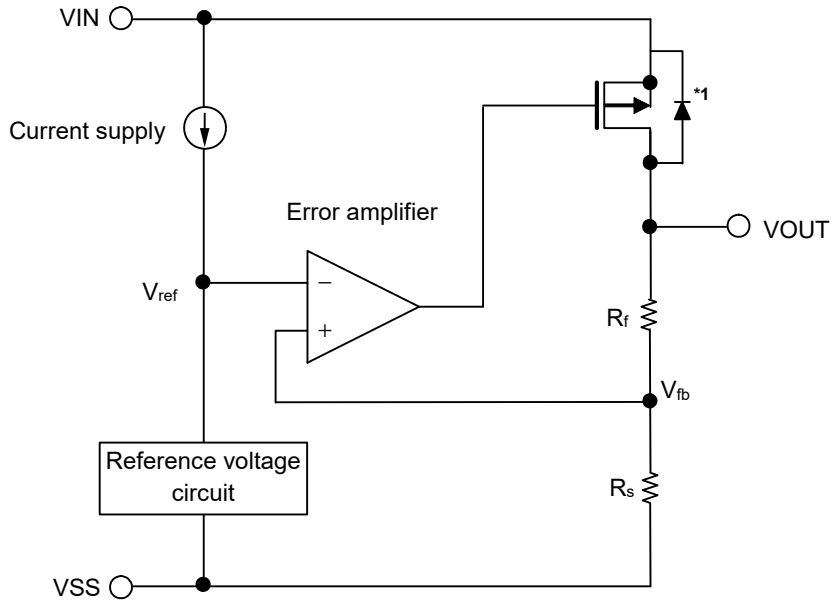
The hysteresis width is the voltage difference between the detection voltage and the release voltage. Setting the hysteresis width between the detection voltage and the release voltage prevents malfunction caused by noise on the pin voltage in the detection status.

■ Operation

1. Regulator block

1. 1 Basic operation

Figure 19 shows the block diagram of the regulator block to describe the basic operation.
The error amplifier compares the feedback voltage (V_{fb}) whose output voltage (V_{OUT}) is divided by the feedback resistors (R_s and R_f) with the reference voltage (V_{ref}). The error amplifier controls the output transistor, consequently, the regulator starts the operation that keeps V_{OUT} constant without the influence of the input voltage (V_{IN}).



***1.** Parasitic diode

Figure 19

1. 2 Output transistor

In the S-19316 Series, a low on-resistance P-channel MOS FET is used between the VIN pin and the VOUT pin as the output transistor. In order to keep V_{OUT} constant, the on-resistance of the output transistor varies appropriately according to the output current (I_{OUT}).

Caution Since a parasitic diode exists between the VIN pin and the VOUT pin due to the structure of the transistor, the IC may be damaged by a reverse current if V_{OUT} becomes higher than V_{IN}. Therefore, be sure that V_{OUT} does not exceed V_{IN} + 0.3 V.

1. 3 Overcurrent protection circuit

The S-19316 Series has a built-in overcurrent protection circuit to limit the overcurrent of the output transistor. When the VOUT pin is shorted to the VSS pin, that is, at the time of the output short-circuit, the output current is limited to 24 mA typ. due to the overcurrent protection circuit operation. The S-19316 Series restarts regulating when the output transistor is released from the overcurrent status.

Caution This overcurrent protection circuit does not work as for thermal protection. For example, when the output transistor keeps the overcurrent status long at the time of output short-circuit or due to other reasons, pay attention to the conditions of the input voltage and the load current so as not to exceed the power dissipation.

1. 4 Thermal shutdown circuit

The S-19316 Series has a built-in thermal shutdown circuit to limit overheating. When the junction temperature increases to 160°C typ., the thermal shutdown circuit becomes the detection status, and the regulating is stopped. When the junction temperature decreases to 135°C typ., the thermal shutdown circuit becomes the release status, and the regulator is restarted.

If the thermal shutdown circuit becomes the detection status due to self-heating, the regulating is stopped and V_{OUT} decreases. For this reason, the self-heating is limited and the temperature of the IC decreases. The thermal shutdown circuit becomes release status when the temperature of the IC decreases, and the regulating is restarted thus the self-heating is generated again. Repeating this procedure makes the waveform of V_{OUT} into a pulse-like form. This phenomenon continues unless decreasing either or both of the input voltage and the output current in order to reduce the internal power consumption, or decreasing the ambient temperature. Note that the product may suffer physical damage such as deterioration if the above phenomenon occurs continuously.

Caution If a large load current flows during the restart process of regulating after the thermal shutdown circuit changes to the release status from the detection status, the thermal shutdown circuit becomes the detection status again due to self-heating, and a problem may happen in the restart of regulating. A large load current, for example, occurs when charging to the C_L whose capacitance is large.
Perform thorough evaluation including the temperature characteristics with an actual application to select C_L.

Table 11

Thermal Shutdown Circuit	VOUT Pin Voltage
Release: 135°C typ.*1	Constant value*2
Detection: 160°C typ.*1	Pulled down to V_{SS}*3

***1.** Junction temperature
***2.** The constant value is output due to the regulating based on the set output voltage value.
***3.** The VOUT pin voltage is pulled down to V_{SS} due to the feedback resistors (R_s and R_f) and a load.

2. Detector block

2. 1 Basic operation

2. 1. 1 S-19316 Series A type

(1) When the input voltage (V_{IN}) is release voltage ($+V_{DET}$) of the detector or higher, the Nch transistor (N1) is off, and the RO pin output is "H".

Since the Nch transistor (N2) is off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{IN}}{R_A + R_B + R_C}$.

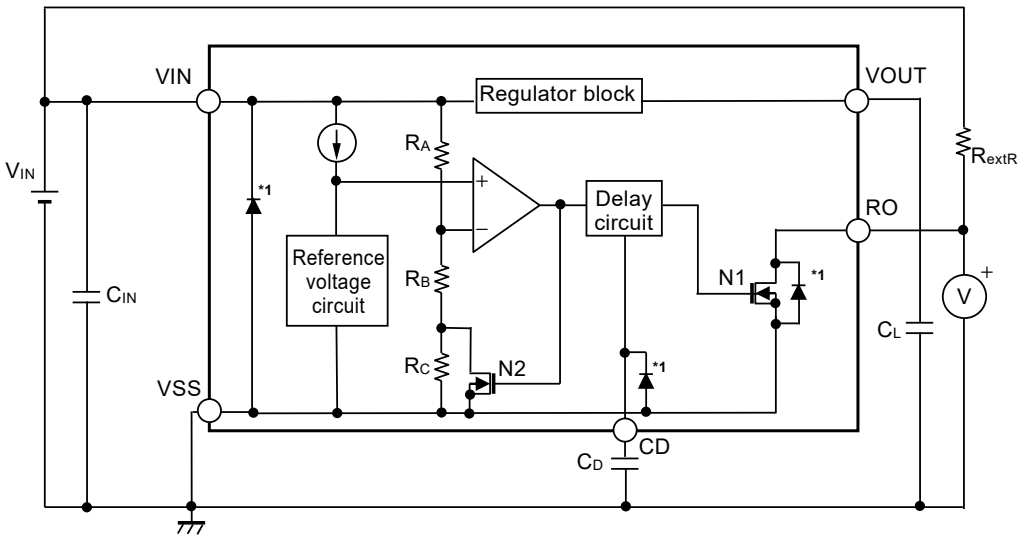
(2) Even if V_{IN} decreases to $+V_{DET}$ or lower, the RO pin output is "H" when V_{IN} is the detection voltage ($-V_{DET}$) or higher. When V_{IN} is $-V_{DET}$ (point A in **Figure 21**) or lower, N1 of output stage is on, and the RO pin output is "L".

At this time, N2 is on, and the input voltage to the comparator is $\frac{R_B \bullet V_{IN}}{R_A + R_B}$.

(3) When V_{IN} further decreases to the IC's minimum operation voltage or lower, the RO pin output is unstable.

(4) When V_{IN} increases and is the IC's minimum operation voltage or higher, the RO pin output is "L". Moreover, even if V_{IN} exceeds $-V_{DET}$, the RO pin output is "L" when V_{IN} is lower than $+V_{DET}$.

(5) When V_{IN} further increases to $+V_{DET}$ (point B in **Figure 21**) or higher, the delay circuit operates. The RO pin output is "H" after the elapse of the release delay time (t_{DELAY}).



***1.** Parasitic diode

Figure 20 Operation

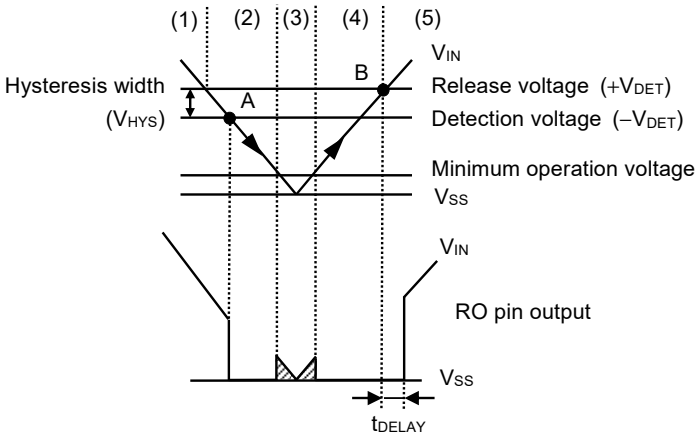


Figure 21 Timing Chart

2. 1. 2 S-19316 Series B type

(1) When the input voltage (V_{IN}) is release voltage ($+V_{DET}$) of the detector or higher, the Pch transistor (P1) is on, the Nch transistor (N1) is off, and the RO pin output is "H".

Since the Nch transistor (N2) is off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{IN}}{R_A + R_B + R_C}$.

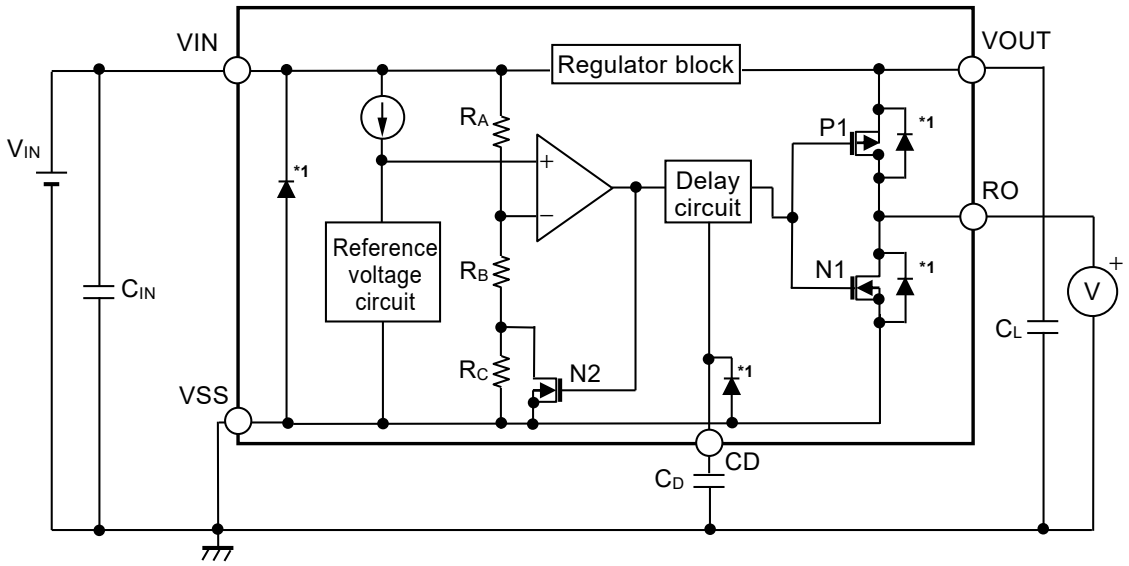
(2) Even if V_{IN} decreases to $+V_{DET}$ or lower, the RO pin output is "H" when V_{IN} is the detection voltage ($-V_{DET}$) or higher. When V_{IN} decreases to $-V_{DET}$ (point A in **Figure 23**) or lower, P1 of output stage is off, N1 of output stage is on, and the RO pin output is "L".

At this time, N2 is on, and the input voltage to the comparator is $\frac{R_B \bullet V_{IN}}{R_A + R_B}$.

(3) When V_{IN} further decreases to the IC's minimum operation voltage or lower, the RO pin output is unstable.

(4) When V_{IN} increases to the IC's minimum operation voltage or higher, the RO pin output is "L". Moreover, even if V_{IN} exceeds $-V_{DET}$, the RO pin output is "L" when V_{IN} is lower than $+V_{DET}$.

(5) When V_{IN} further increases to $+V_{DET}$ (point B in **Figure 23**) or higher, the delay circuit operates. The RO pin output is "H" after the elapse of the release delay time (t_{DELAY}).



***1.** Parasitic diode

Figure 22 Operation

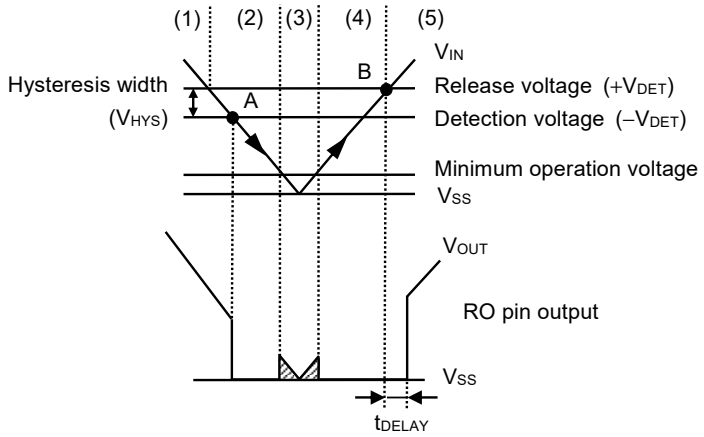


Figure 23 Timing Chart

2. 2 Delay circuit

The delay circuit has a function that adjusts the release delay time (t_{DELAY}) from when the input voltage (V_{IN}) reaches the release voltage ($+V_{DET}$) of the detector to when the output from the RO pin inverts.
t_{DELAY} is determined by the delay coefficient, the delay time adjustment capacitor (C_D) and the release delay time when the CD pin is open (t_{DELAY0}). It is calculated by the equation below.

$$t_{DELAY}\ [ms] = \text{Delay coefficient} \times C_D\ [nF] + t_{DELAY0}\ [ms]$$

Table 12

Junction Temperature	Delay Coefficient		
	Min.	Typ.	Max.
T_j = –40°C to +125°C	2.76	3.00	3.28

Table 13

Junction Temperature	Release Delay Time when CD Pin is Open (t_{DELAY0})		
	Min.	Typ.	Max.
T_j = –40°C to +125°C	0.03 ms	0.07 ms	0.36 ms

Caution 1. The above equation will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.
2. Mounted board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.
3. There is no limit for the capacitance of C_D as long as the leakage current of the capacitor can be ignored against the built-in constant current value (approximately 350 nA). The leakage current may cause error in delay time. When the leakage current is larger than the built-in constant current, no detect or release takes place.

2. 3 V_{IN} drop during release delay time (reference)

Figure 24 shows the relation between pulse width (t_{PW}) and V_{IN} lower limit (V_{DROP}) where a release signal can be output after the normal release delay time has elapsed when the VIN pin voltage instantaneously drops during release delay time.

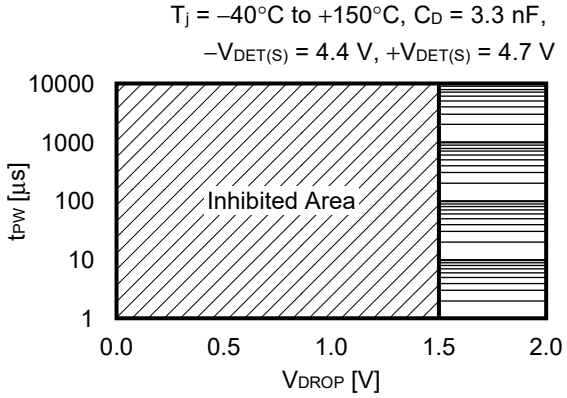
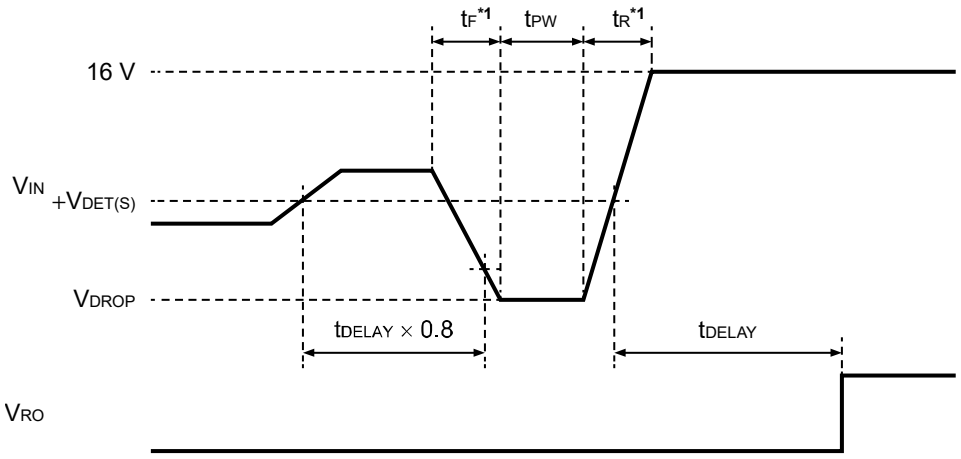


Figure 24



***1.** $t_R = t_F = 10$ µs

Figure 25 VIN Pin Input Voltage Waveform

Caution 1. Figure 24 shows the input voltage conditions when a release signal is output after the normal release delay time has elapsed. When this is within the inhibited area, release may erroneously be executed before the delay time completes.

2. When the VIN pin voltage is within the inhibited areas shown in Figure 24 during release delay time, input 0 V to the VIN pin then restart the detector.

■ Precautions

- Generally, when a voltage regulator is used under the condition that the impedance of the power supply is high, an oscillation may occur. Perform thorough evaluation including the temperature characteristics with an actual application to select C_{IN}.
- Generally, in a voltage regulator, an oscillation may occur depending on the selection of the external parts. The following use conditions are recommended in the S-19316 Series; however, perform thorough evaluation including the temperature characteristics with an actual application to select C_{IN} and C_L.

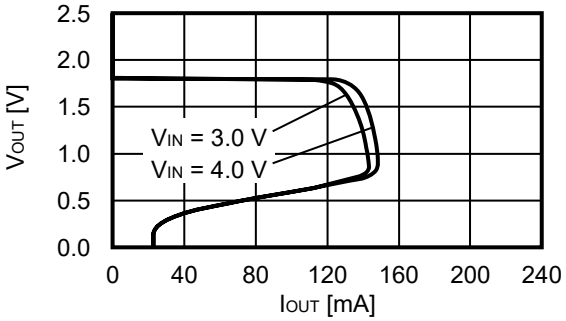
  Input capacitor (C_{IN}): A ceramic capacitor with capacitance of 1.0 μF or more is recommended.
  Output capacitor (C_L): A ceramic capacitor with capacitance of 1.0 μF or more is recommended.
- Generally, in a voltage regulator, the values of an overshoot and an undershoot in the output voltage vary depending on the variation factors of input voltage start-up, input voltage fluctuation, load fluctuation etc., or the capacitance of C_{IN} or C_L and the value of the equivalent series resistance (ESR), which may cause a problem to the stable operation. Perform thorough evaluation including the temperature characteristics with an actual application to select C_{IN} and C_L.
- Generally, in a voltage regulator, an overshoot may occur in the output voltage momentarily if the input voltage steeply changes when the input voltage is started up, the input voltage fluctuates, etc. Perform thorough evaluation including the temperature characteristics with an actual application to confirm no problems happen.
- Generally, in a voltage regulator, if the VOUT pin is steeply shorted with GND, a negative voltage exceeding the absolute maximum ratings may occur in the VOUT pin due to resonance phenomenon of the inductance and the capacitance including C_L on the application. The resonance phenomenon is expected to be weakened by inserting a series resistor into the resonance path, and the negative voltage is expected to be limited by inserting a protection diode between the VOUT pin and the VSS pin.
- If the input voltage is started up steeply under the condition that the capacitance of C_L is large, the thermal shutdown circuit may be in the detection status by self-heating due to the charge current to C_L.
- Make sure of the conditions for the input voltage, output voltage and the load current so that the internal loss does not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- When considering the output current value that the IC is able to output, make sure of the output current value specified in **Table 8** in "■ **Electrical Characteristics**" and footnote ***4** of the table.
- Wiring patterns on the application related to the VIN pin, the VOUT pin and the VSS pin should be designed so that the impedance is low. When mounting C_{IN} between the VIN pin and the VSS pin and C_L between the VOUT pin and the VSS pin, connect the capacitors as close as possible to the respective destination pins of the IC.
- In the package equipped with heat sink of backside, mount the heat sink firmly. Since the heat radiation differs according to the condition of the application, perform thorough evaluation with an actual application to confirm no problems happen.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

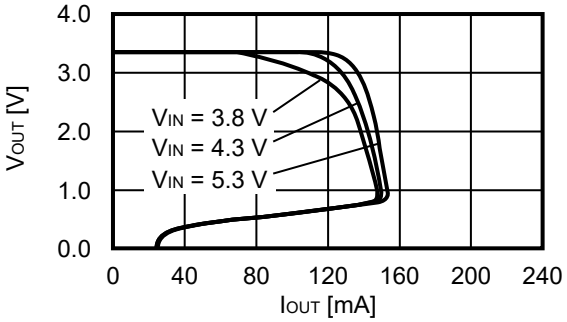
1. Regulator block

1. 1 Output voltage vs. Output current (When load current increases) (Ta = +25°C)

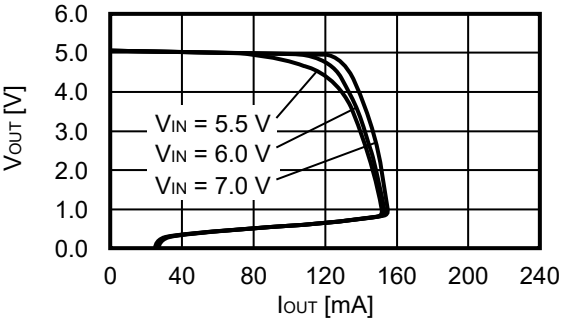
1. 1. 1 V_{OUT} = 1.8 V



1. 1. 2 V_{OUT} = 3.3 V



1. 1. 3 V_{OUT} = 5.0 V

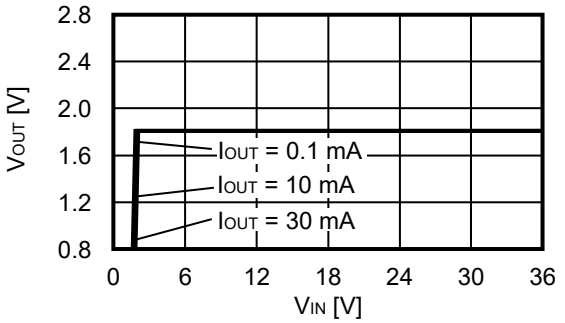


Remark In determining the output current, attention should be paid to the following.

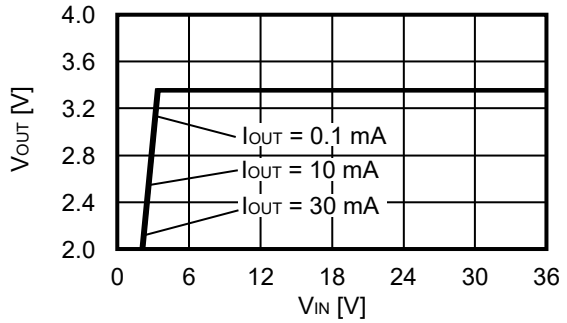
1. The minimum output current value and footnote ***4** of **Table 8** in "■ **Electrical Characteristics**"
2. Power dissipation

1. 2 Output voltage vs. Input voltage (Ta = +25°C)

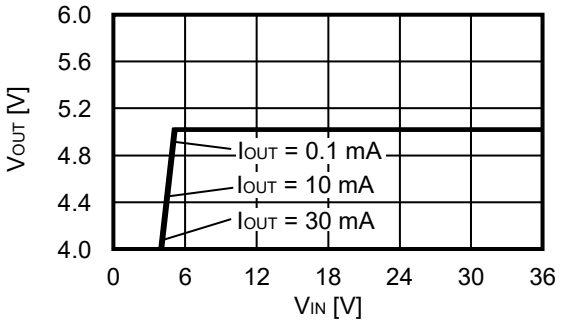
1. 2. 1 V_{OUT} = 1.8 V



1. 2. 2 V_{OUT} = 3.3 V

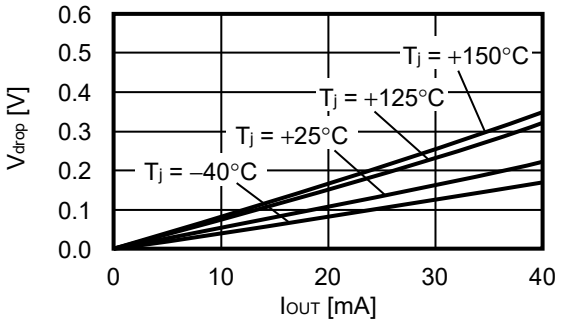


1. 2. 3 V_{OUT} = 5.0 V

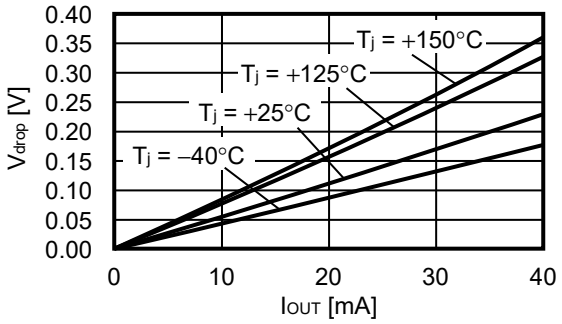


1. 3 Dropout voltage vs. Output current

1. 3. 1 V_{OUT} = 3.3 V

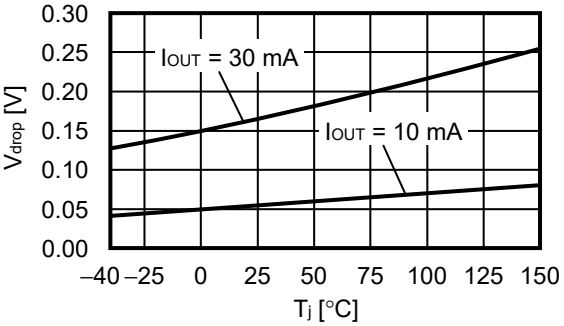


1. 3. 2 V_{OUT} = 5.0 V

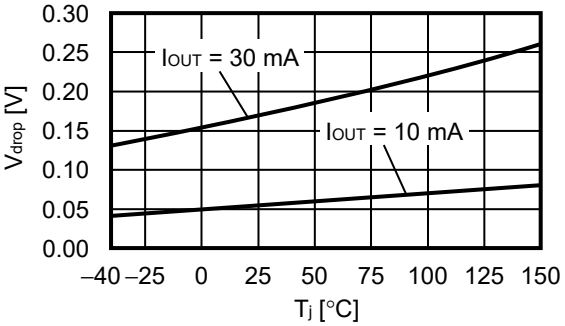


1. 4 Dropout voltage vs. Junction temperature

1. 4. 1 V_{OUT} = 3.3 V

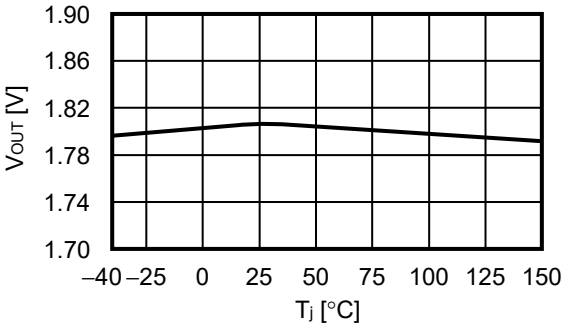


1. 4. 2 V_{OUT} = 5.0 V

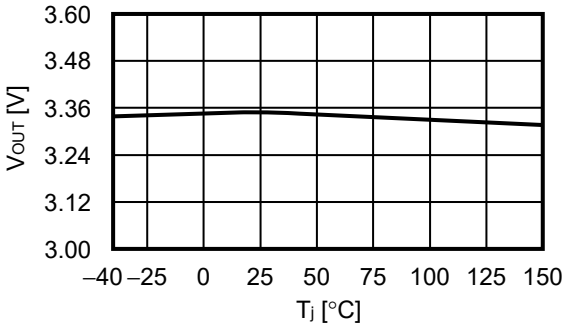


1. 5 Output voltage vs. Junction temperature

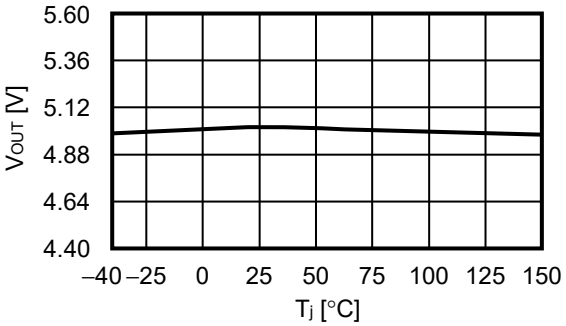
1. 5. 1 V_{OUT} = 1.8 V



1. 5. 2 V_{OUT} = 3.3 V

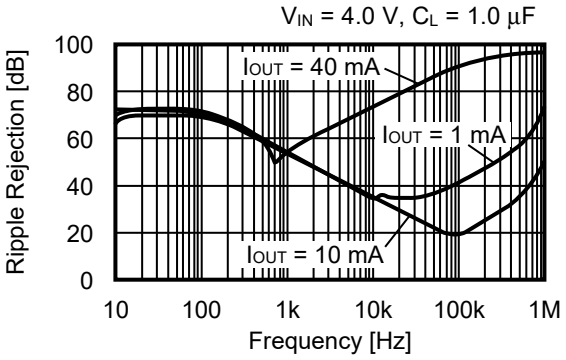


1. 5. 3 V_{OUT} = 5.0 V

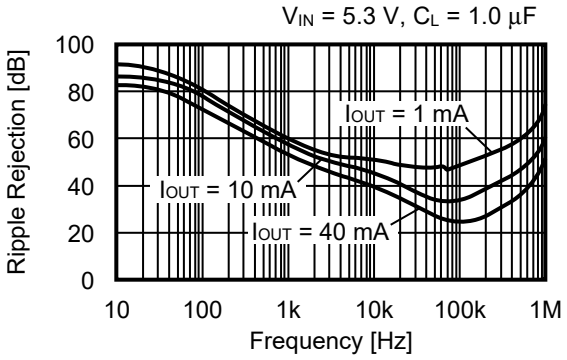


1. 6 Ripple rejection (Ta = +25°C)

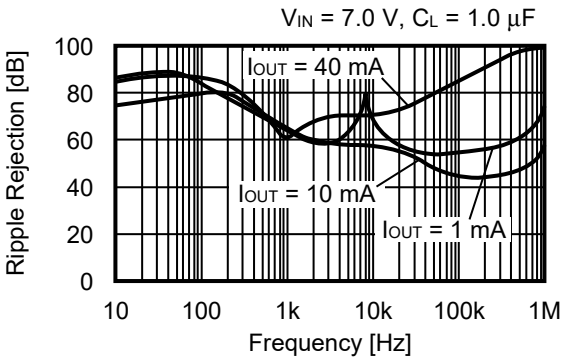
1. 6. 1 V_{OUT} = 1.8 V



1. 6. 2 V_{OUT} = 3.3 V



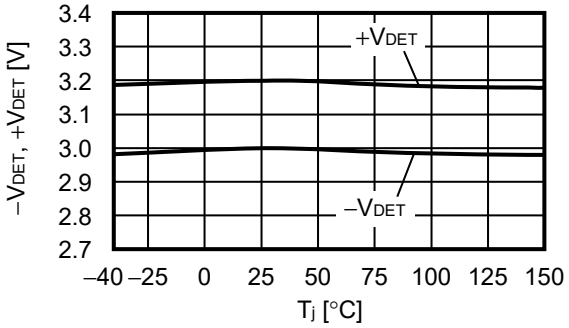
1. 6. 3 V_{OUT} = 5.0 V



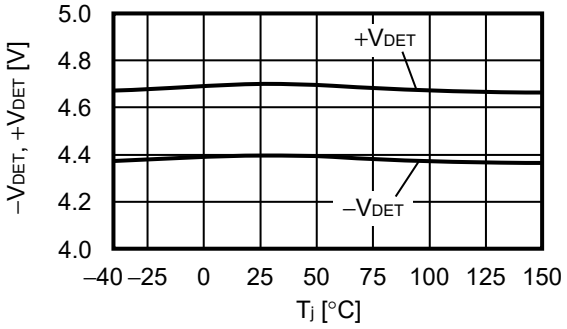
2. Detector block

2. 1 Detection voltage, Release voltage vs. Junction temperature

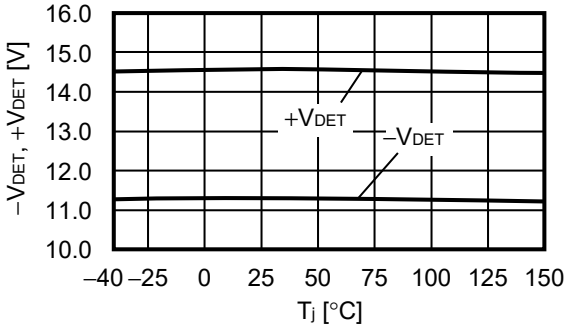
2. 1. 1 $-V_{DET}$ = 3.0 V, $+V_{DET}$ = 3.2 V



2. 1. 2 $-V_{DET}$ = 4.4 V, $+V_{DET}$ = 4.7 V

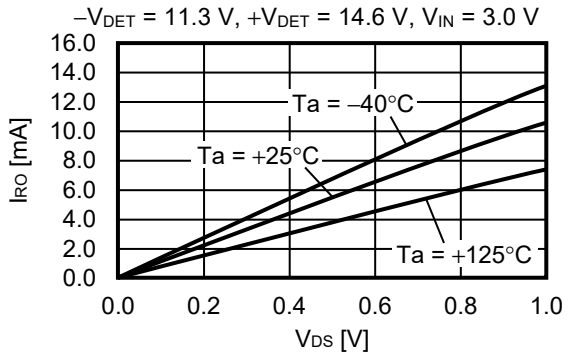


2. 1. 3 $-V_{DET}$ = 11.3 V, $+V_{DET}$ = 14.6 V

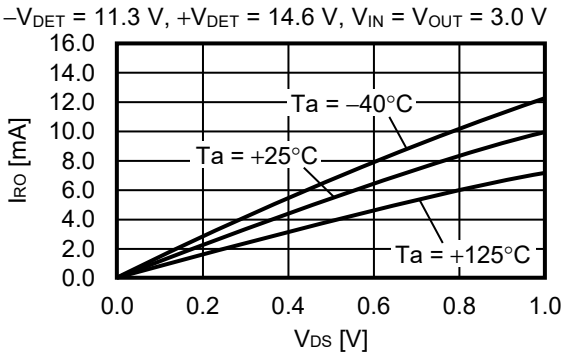


2. 2 Nch transistor output current vs. V_{DS}

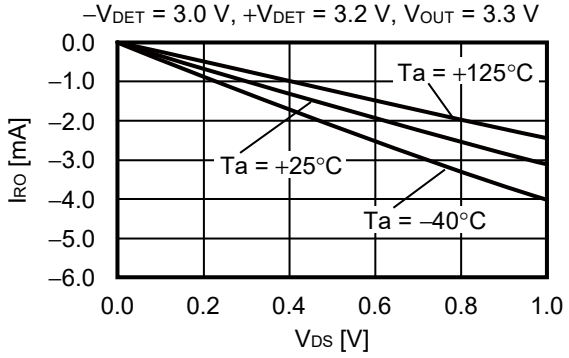
2. 2. 1 S-19316 Series A type



2. 2. 2 S-19316 Series B type



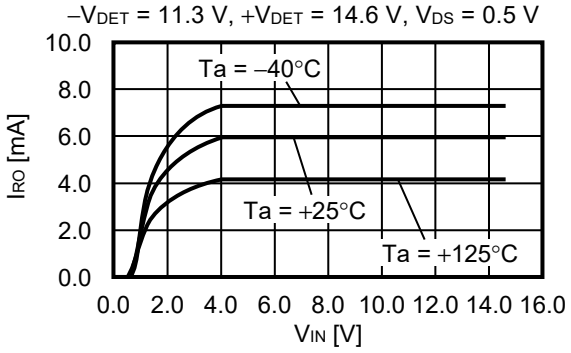
2. 3 Pch transistor output current vs. V_{DS} (S-19316 Series B type)



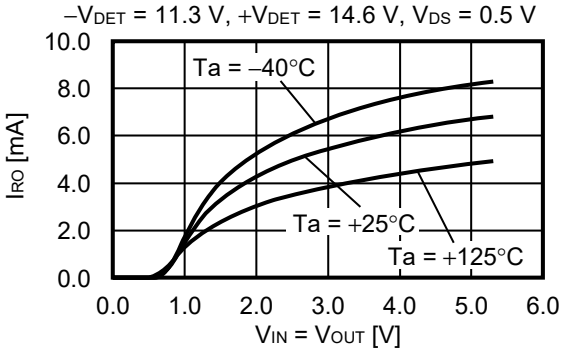
Remark V_{DS}: Drain-to-source voltage of the output transistor

2. 4 Nch transistor output current vs. Power supply voltage

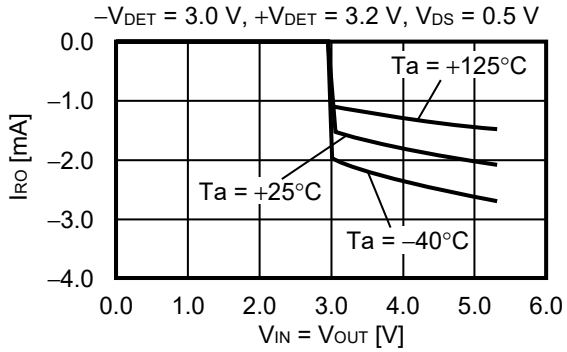
2. 4. 1 S-19316 Series A type



2. 4. 2 S-19316 Series B type



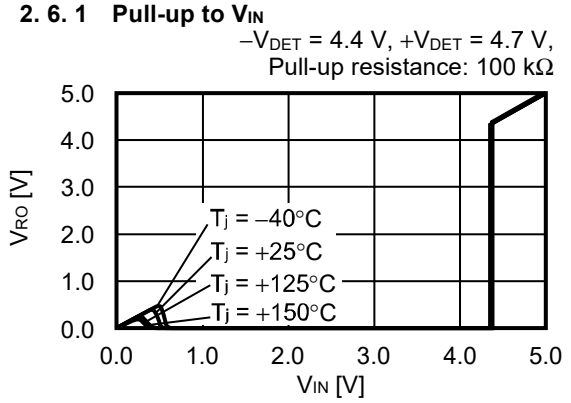
2. 5 Pch transistor output current vs. Output voltage (S-19316 series B type)



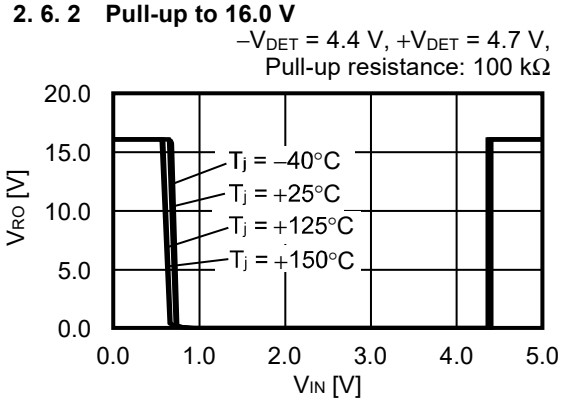
Remark V_{DS}: Drain-to-source voltage of the output transistor

2. 6 Minimum operation voltage vs. Power supply voltage / Output voltage (S-19316 series A type)

2. 6. 1 Pull-up to V_{IN}



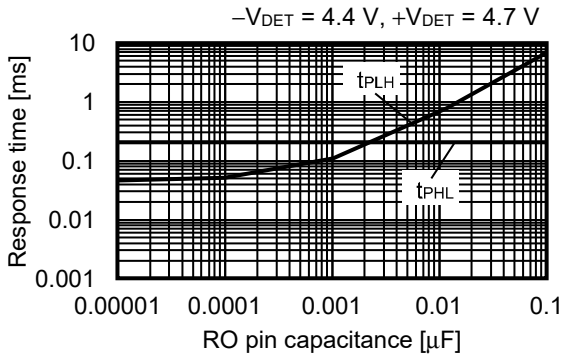
2. 6. 2 Pull-up to 16.0 V



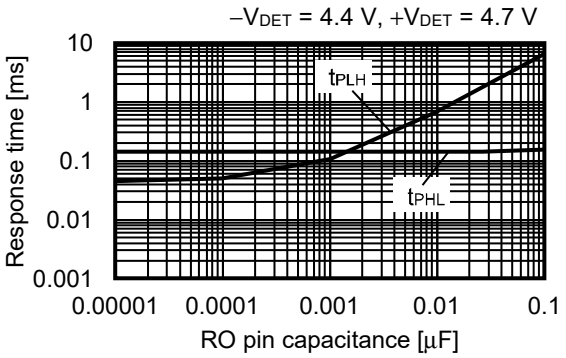
2. 7 Dynamic response vs. RO pin capacitance

2. 7. 1 S-19316 Series A type

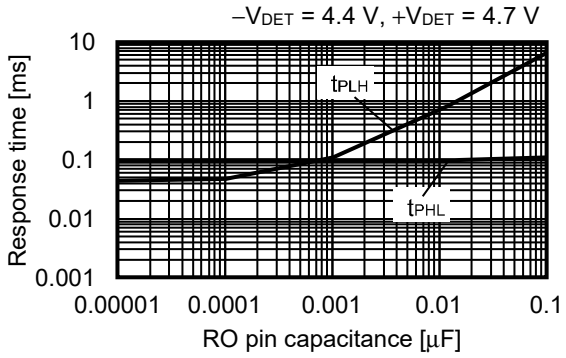
(1) Ta = –40°C

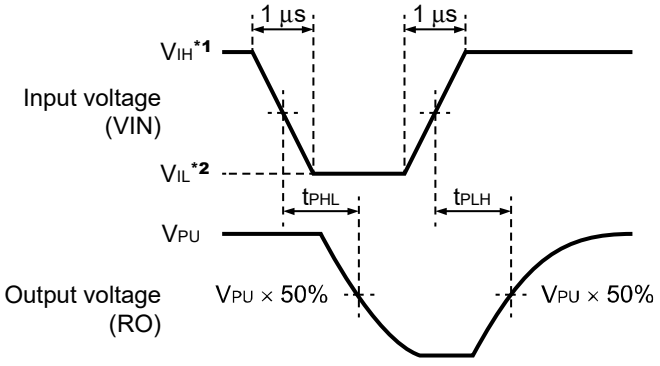


(2) Ta = +25°C



(3) Ta = +125°C





***1.** V_{IH} = 36.0 V
***2.** V_{IL} = 2.5 V

Figure 26 Test Condition of Response Time

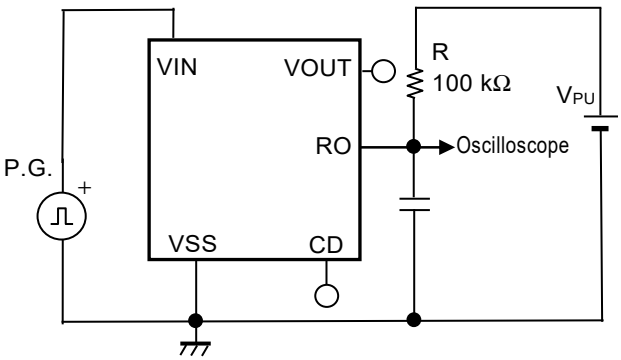
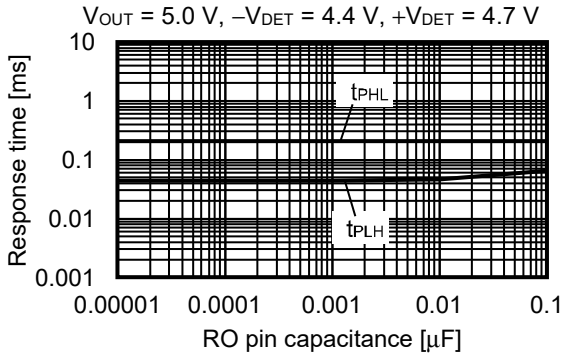


Figure 27 Test Circuit of Response Time

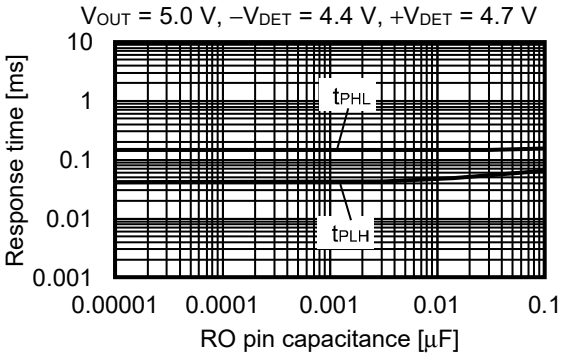
Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

2. 7. 2 S-19316 Series B type

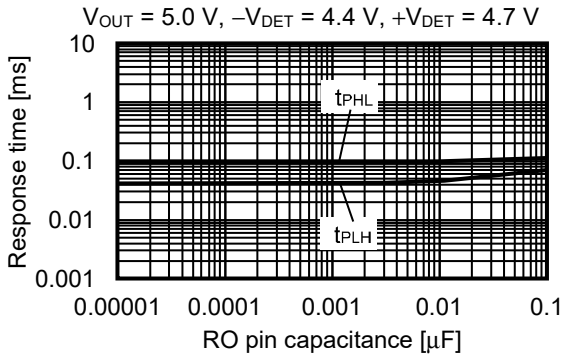
(1) Ta = –40°C

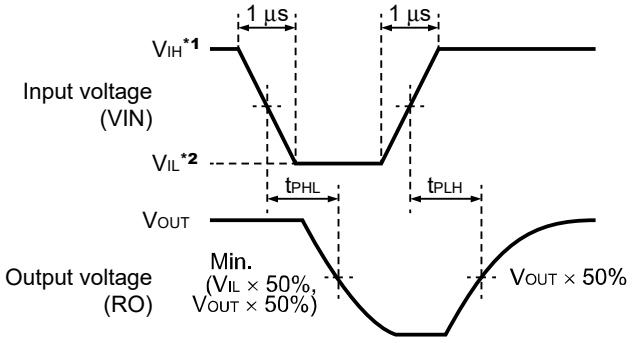


(2) Ta = +25°C



(3) Ta = +125°C





***1.** V_{IH} = 36.0 V
***2.** V_{IL} = 2.5 V

Figure 28 Test Condition of Response Time

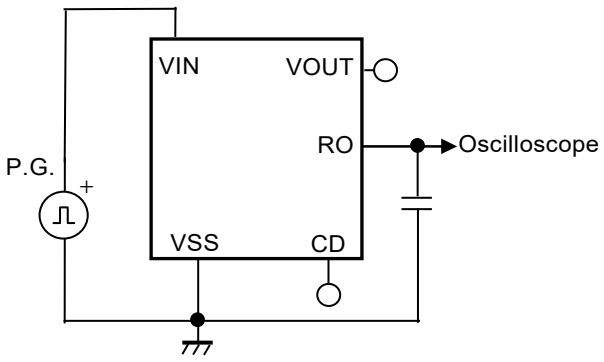


Figure 29 Test Circuit of Response Time

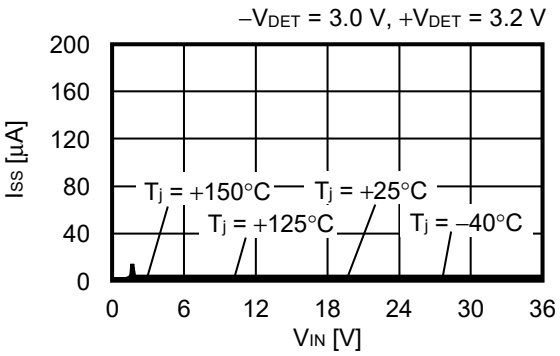
Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

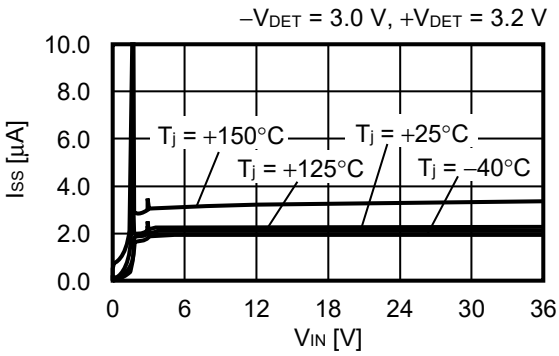
3. Overall

3. 1 Current consumption vs. Input voltage (No load)

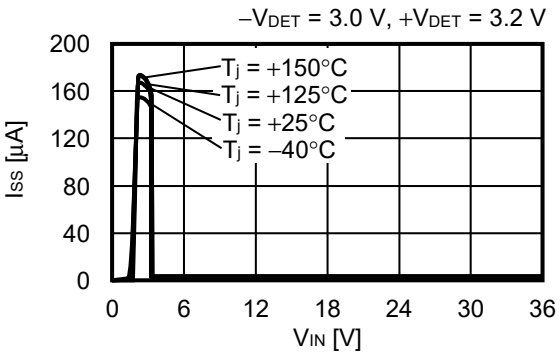
3. 1. 1 S-19316 Series A type

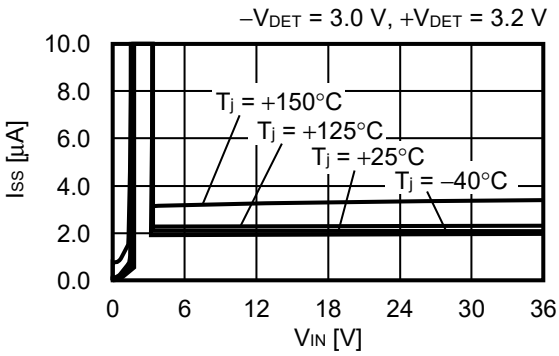
(1) V_{OUT} = 1.8 V



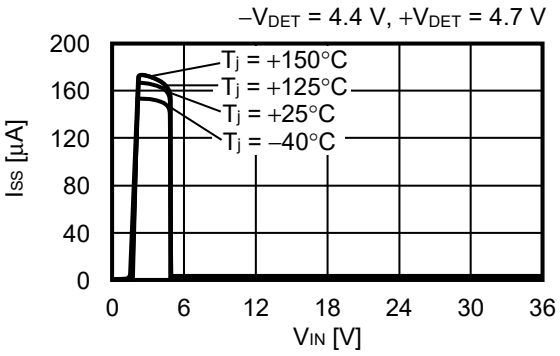


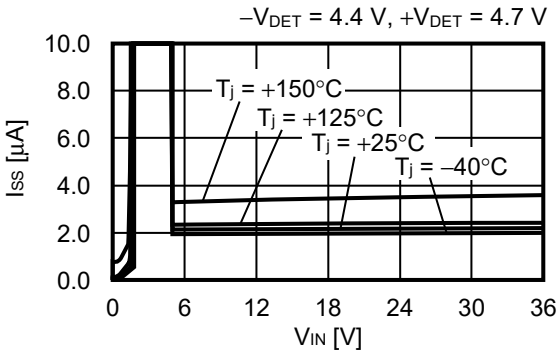
(2) V_{OUT} = 3.3 V





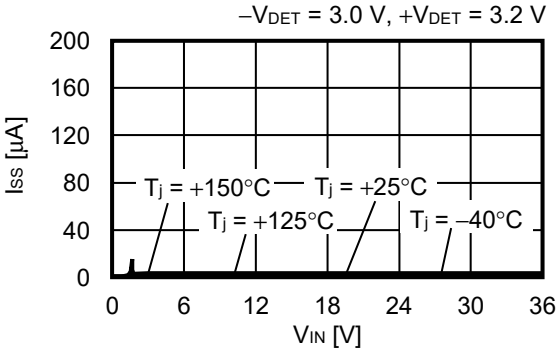
(3) V_{OUT} = 5.0 V

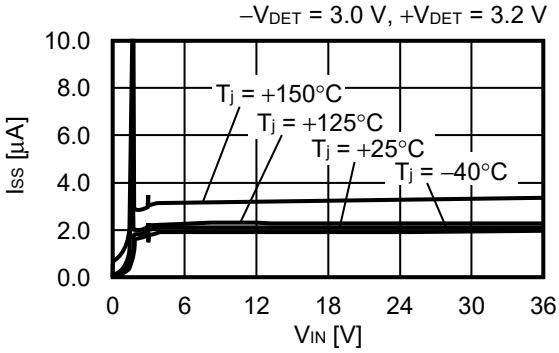




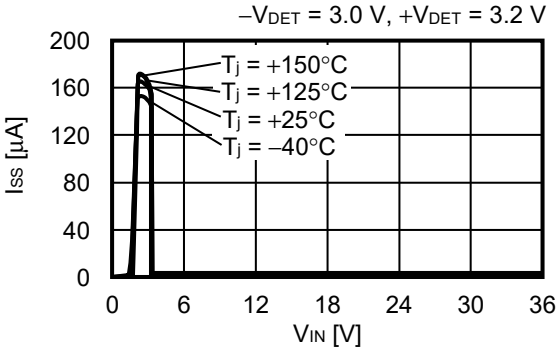
3. 1. 2 S-19316 Series B type

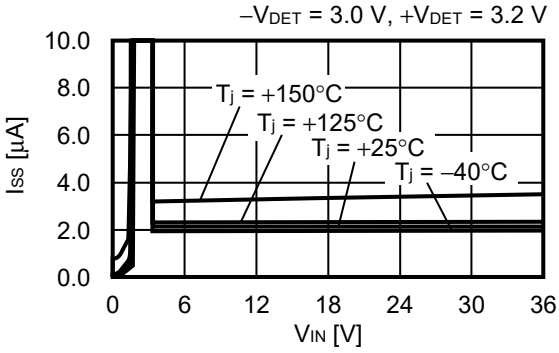
(1) V_{OUT} = 1.8 V



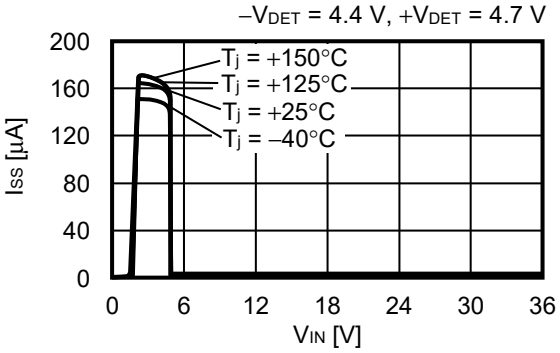


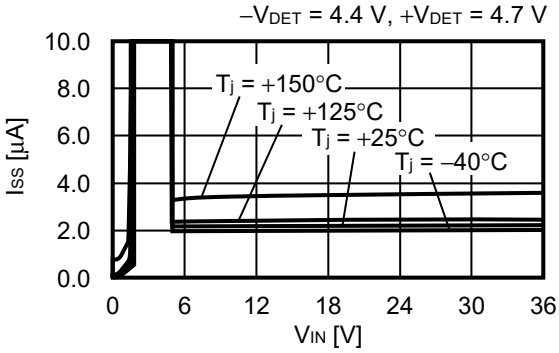
(2) V_{OUT} = 3.3 V





(3) V_{OUT} = 5.0 V

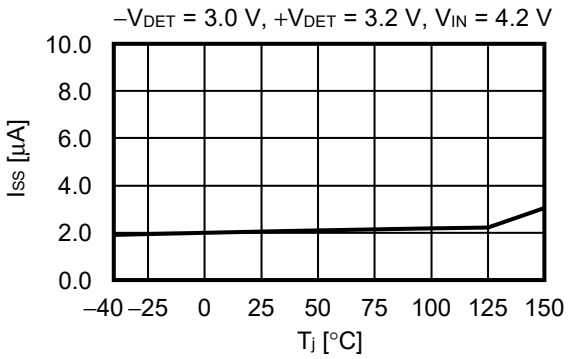




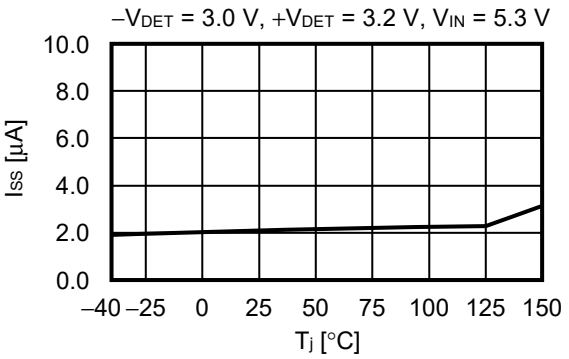
3. 2 Current consumption vs. Junction temperature

3. 2. 1 S-19316 Series A type

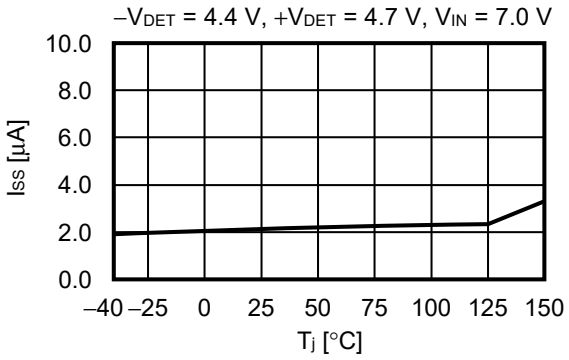
(1) V_{OUT} = 1.8 V



(2) V_{OUT} = 3.3 V

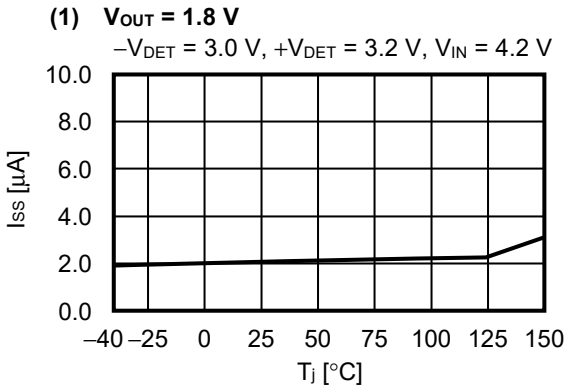


(3) V_{OUT} = 5.0 V

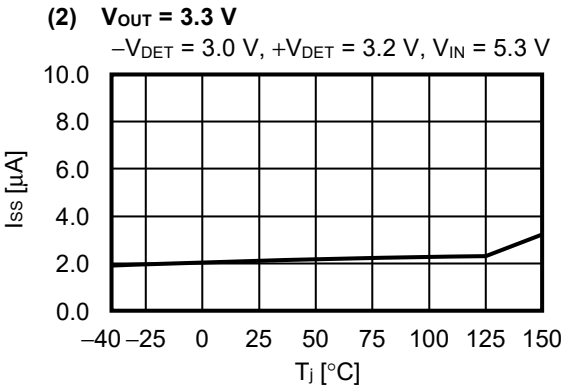


3. 2. 2 S-19316 Series B type

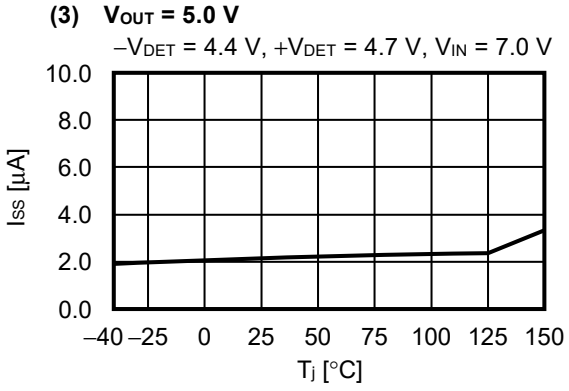
(1) V_{OUT} = 1.8 V



(2) V_{OUT} = 3.3 V



(3) V_{OUT} = 5.0 V

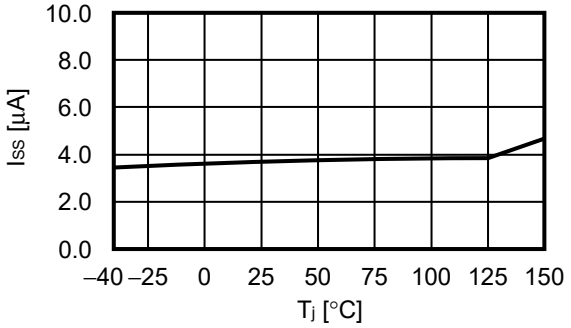


3. 3 Current consumption during release delay time vs. Junction temperature

3. 3. 1 S-19316 Series A type

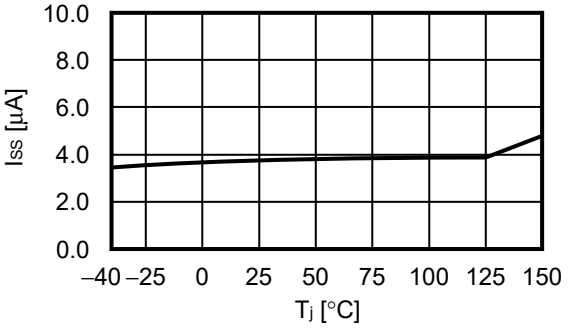
(1) V_{OUT} = 1.8 V

$-V_{DET}$ = 3.0 V, $+V_{DET}$ = 3.2 V, V_{IN} = 4.2 V, V_{CD} = 0.0 V



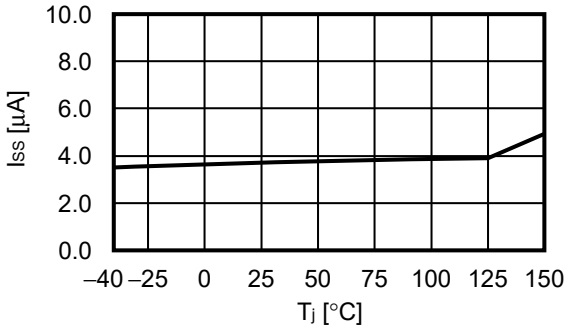
(2) V_{OUT} = 3.3 V

$-V_{DET}$ = 3.0 V, $+V_{DET}$ = 3.2 V, V_{IN} = 5.3 V, V_{CD} = 0.0 V



(3) V_{OUT} = 5.0 V

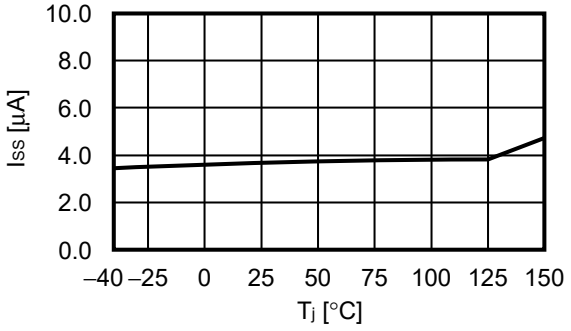
$-V_{DET}$ = 4.4 V, $+V_{DET}$ = 4.7 V, V_{IN} = 7.0 V, V_{CD} = 0.0 V



3. 3. 2 S-19316 Series B type

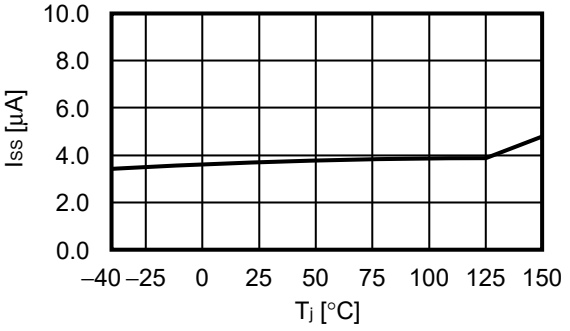
(1) V_{OUT} = 1.8 V

$-V_{DET}$ = 3.0 V, $+V_{DET}$ = 3.2 V, V_{IN} = 4.2 V, V_{CD} = 0.0 V



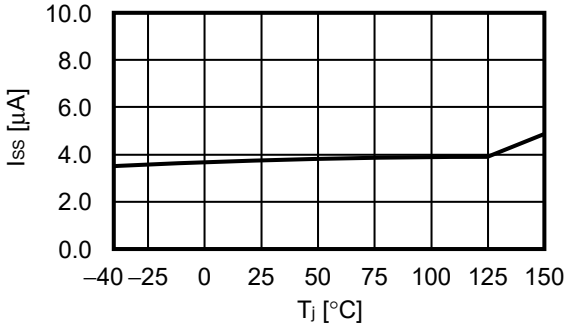
(2) V_{OUT} = 3.3 V

$-V_{DET}$ = 3.0 V, $+V_{DET}$ = 3.2 V, V_{IN} = 5.3 V, V_{CD} = 0.0 V



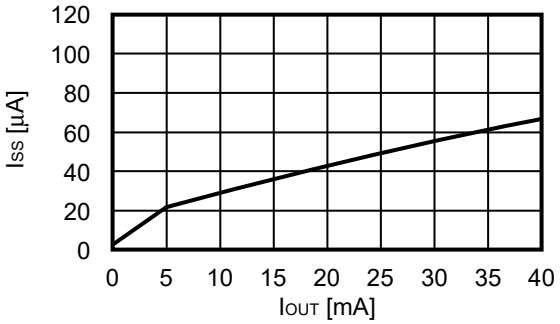
(3) V_{OUT} = 5.0 V

$-V_{DET}$ = 4.4 V, $+V_{DET}$ = 4.7 V, V_{IN} = 7.0 V, V_{CD} = 0.0 V

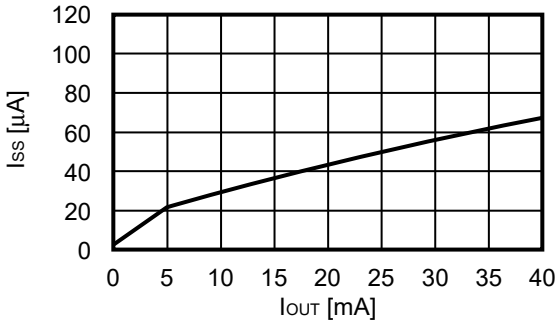


3. 4 Current consumption vs. Output current (Ta = +25°C)

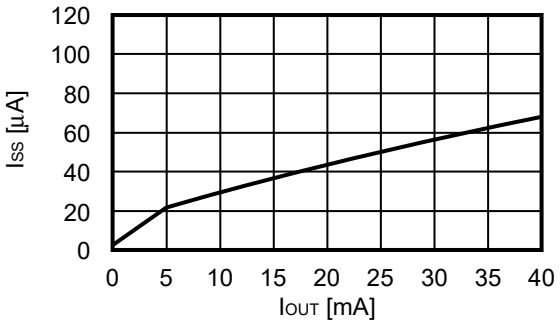
3. 4. 1 V_{OUT} = 1.8 V



3. 4. 2 V_{OUT} = 3.3 V



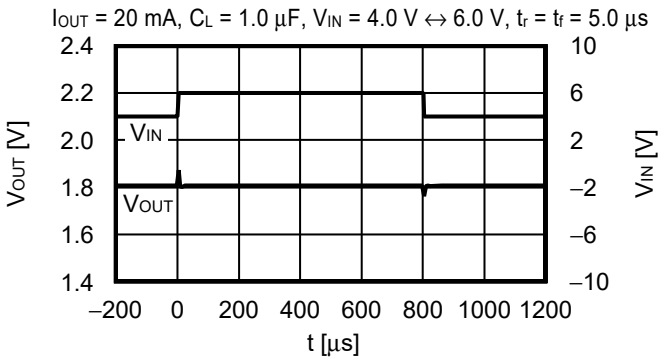
3. 4. 3 V_{OUT} = 5.0 V



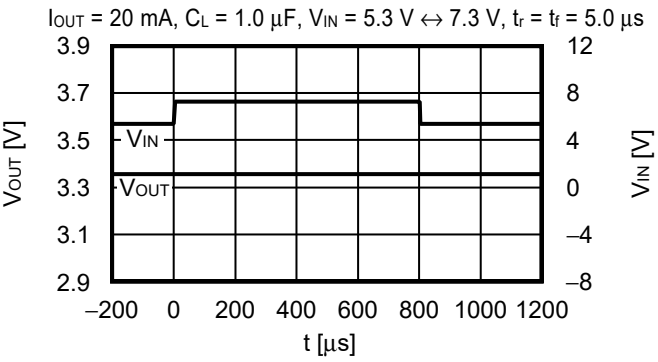
■ Reference Data

1. Transient response characteristics when input (Ta = +25°C)

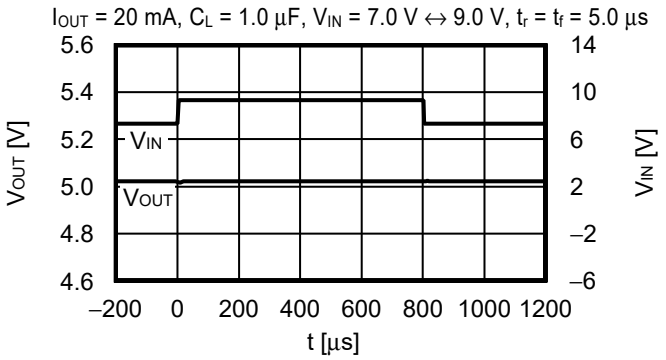
1. 1 V_{OUT} = 1.8 V



1. 2 V_{OUT} = 3.3 V

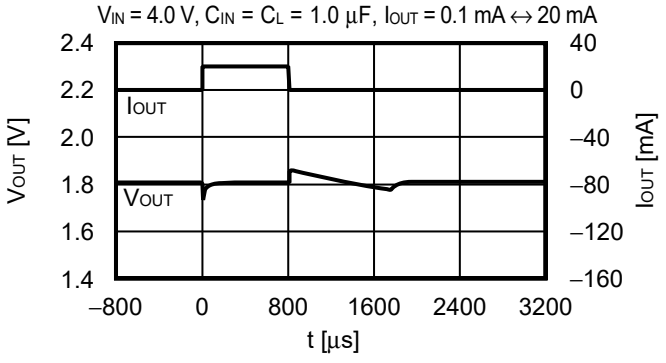


1. 3 V_{OUT} = 5.0 V

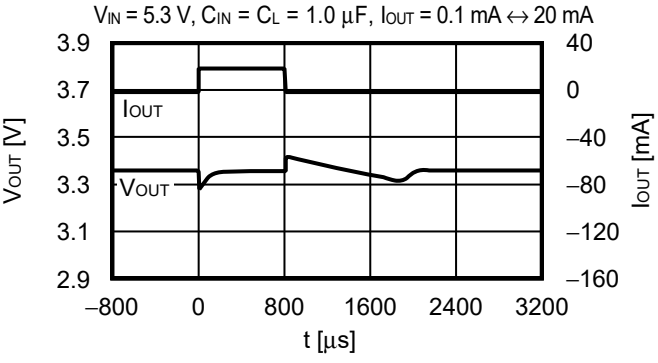


2. Transient response characteristics of load (Ta = +25°C)

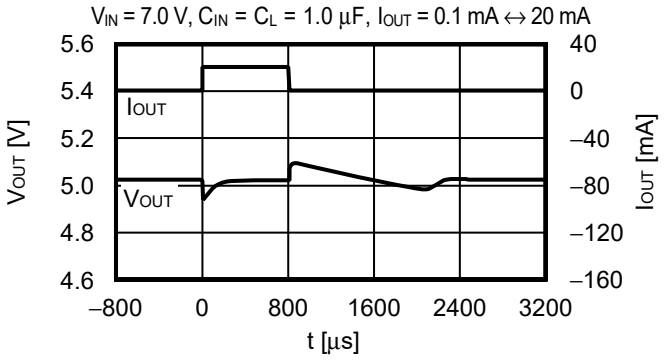
2. 1 V_{OUT} = 1.8 V



2. 2 V_{OUT} = 3.3 V

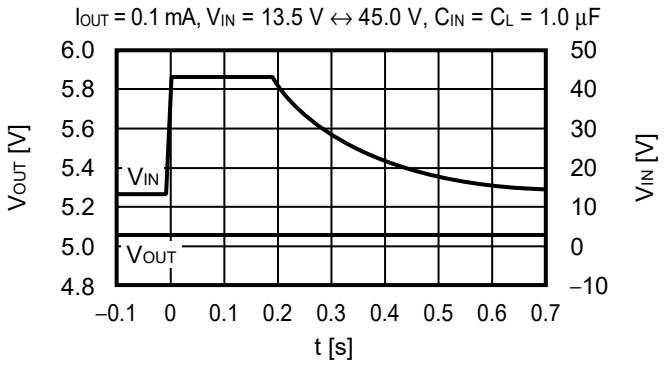


2. 3 V_{OUT} = 5.0 V



3. Load dump characteristics (Ta = +25°C)

3. 1 V_{OUT} = 5.0 V



4. Example of equivalent series resistance vs. Output current characteristics (Ta = +25°C)

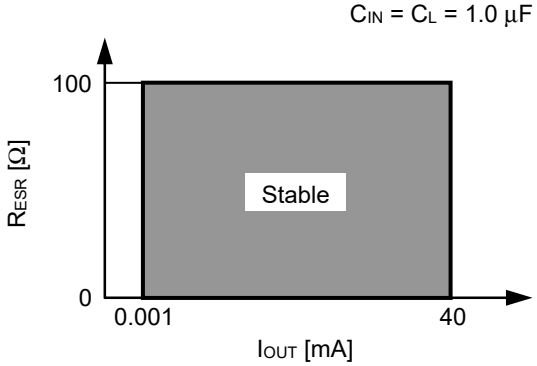
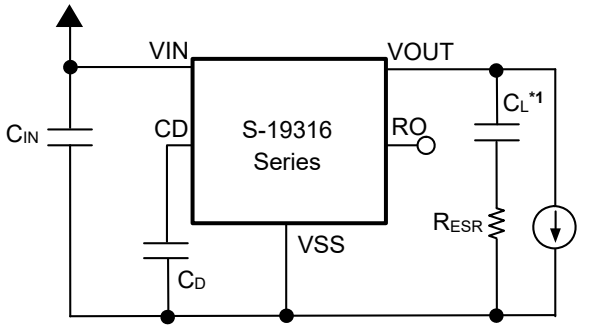


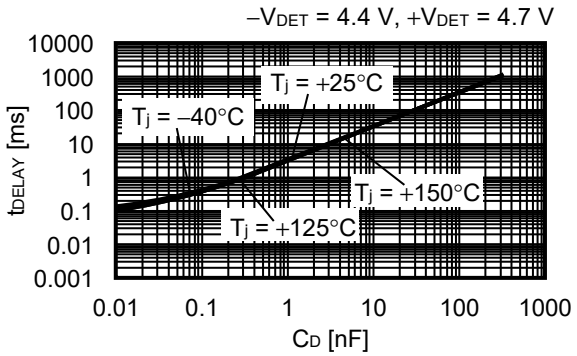
Figure 30



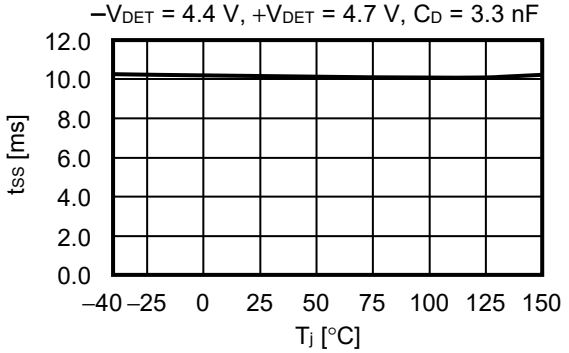
***1.** C_L: TDK Corporation CGA4J3X8R1C105K (1.0 µF)

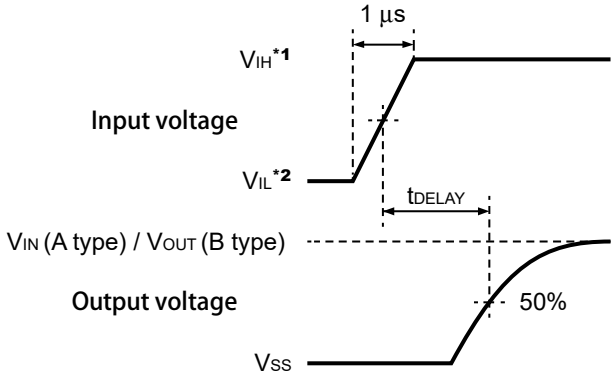
Figure 31

5. Release delay time vs. CD pin capacitance (Without output pin capacitance)



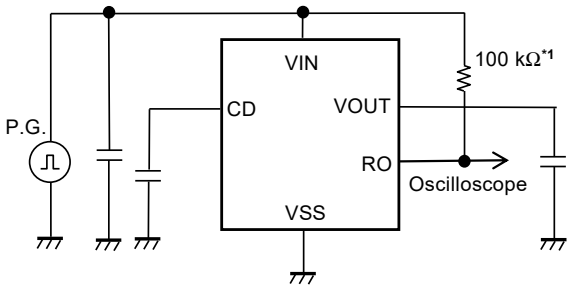
6. Release delay time vs. Junction temperature





*1. $V_{IH} = +V_{DET(S)} + 1.0$ V
*2. When $3.0\ V \le +V_{DET(S)} < 3.5$ V, $V_{IL} = 2.5$ V
When $3.5\ V \le +V_{DET(S)} \le 14.6$ V, $V_{IL} = +V_{DET(S)} - 1.0$ V

Figure 32 Test Condition of Release Delay Time



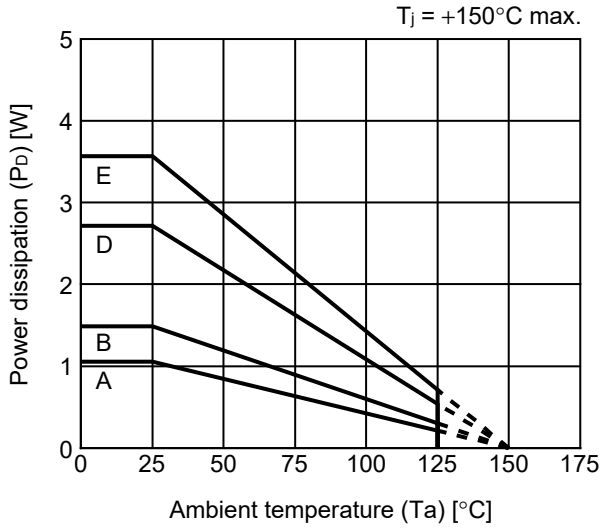
*1. Only S-19316 Series A type

Figure 33 Test Circuit of Release Delay Time

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

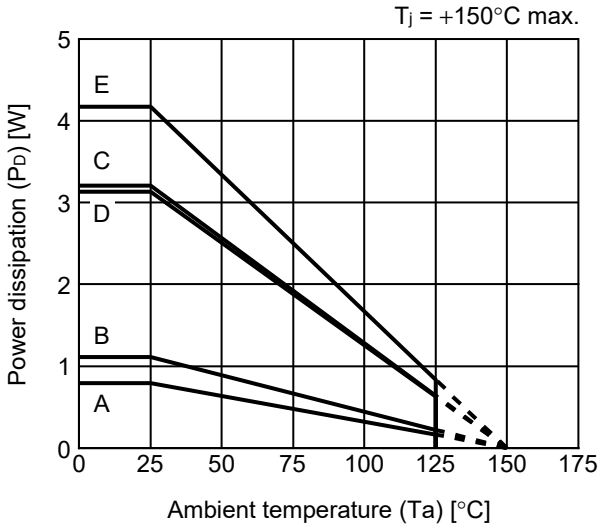
■ Power Dissipation

SOT-89-5



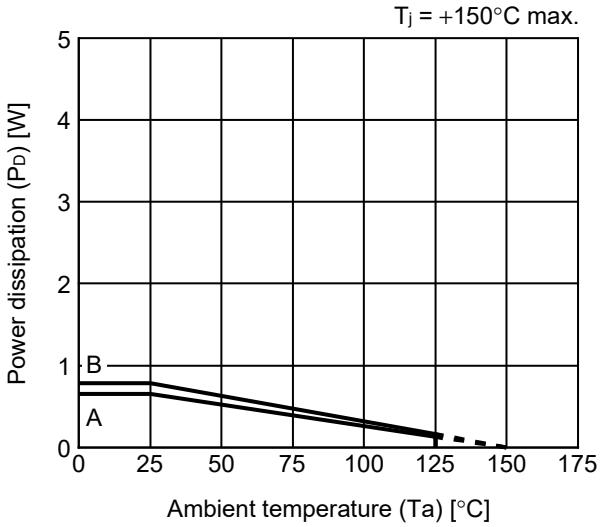
Board	Power Dissipation (P_D)
A	1.05 W
B	1.49 W
C	–
D	2.72 W
E	3.57 W

HTMSOP-8



Board	Power Dissipation (P_D)
A	0.79 W
B	1.11 W
C	3.21 W
D	3.13 W
E	4.17 W

SOT-23-5

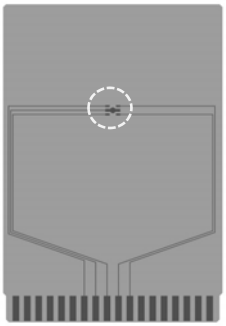


Board	Power Dissipation (P_D)
A	0.65 W
B	0.78 W
C	–
D	–
E	–

SOT-89-5 Test Board

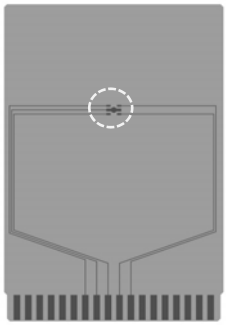
IC Mount Area

(1) Board A



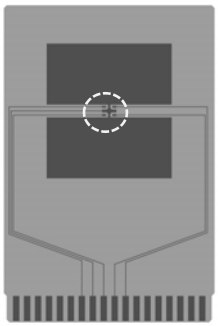
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



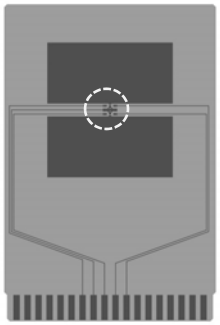
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board D



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(4) Board E



enlarged view

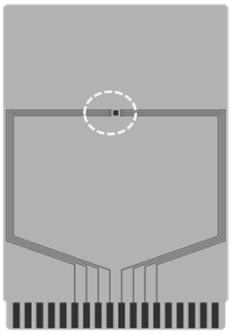
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. SOT895-A-Board-SD-1.0

HTMSOP-8 Test Board

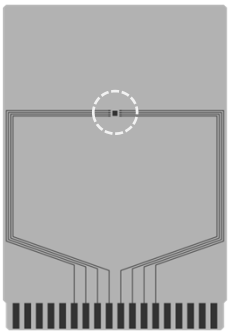
IC Mount Area

(1) Board A



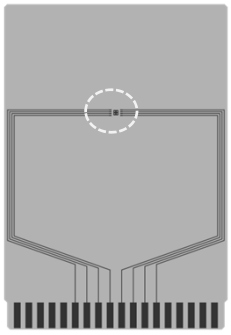
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



enlarged view

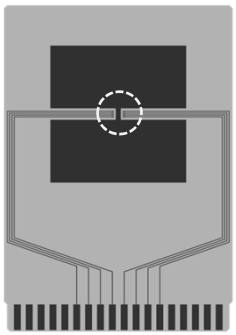
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HTMSOP8-A-Board-SD-1.0

HTMSOP-8 Test Board

IC Mount Area

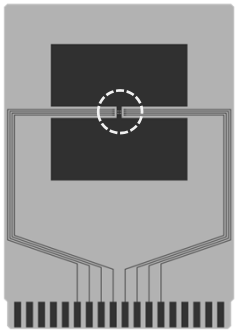
(4) Board D



enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) Board E



enlarged view

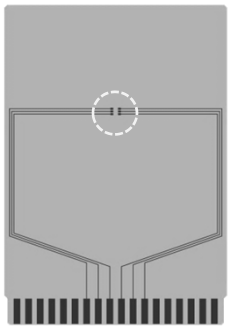
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HTMSOP8-A-Board-SD-1.0

SOT-23-3/3S/5/6 Test Board

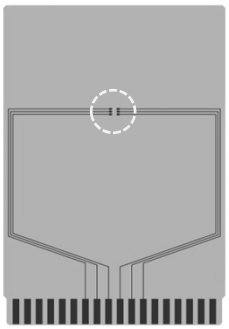
IC Mount Area

(1) Board A



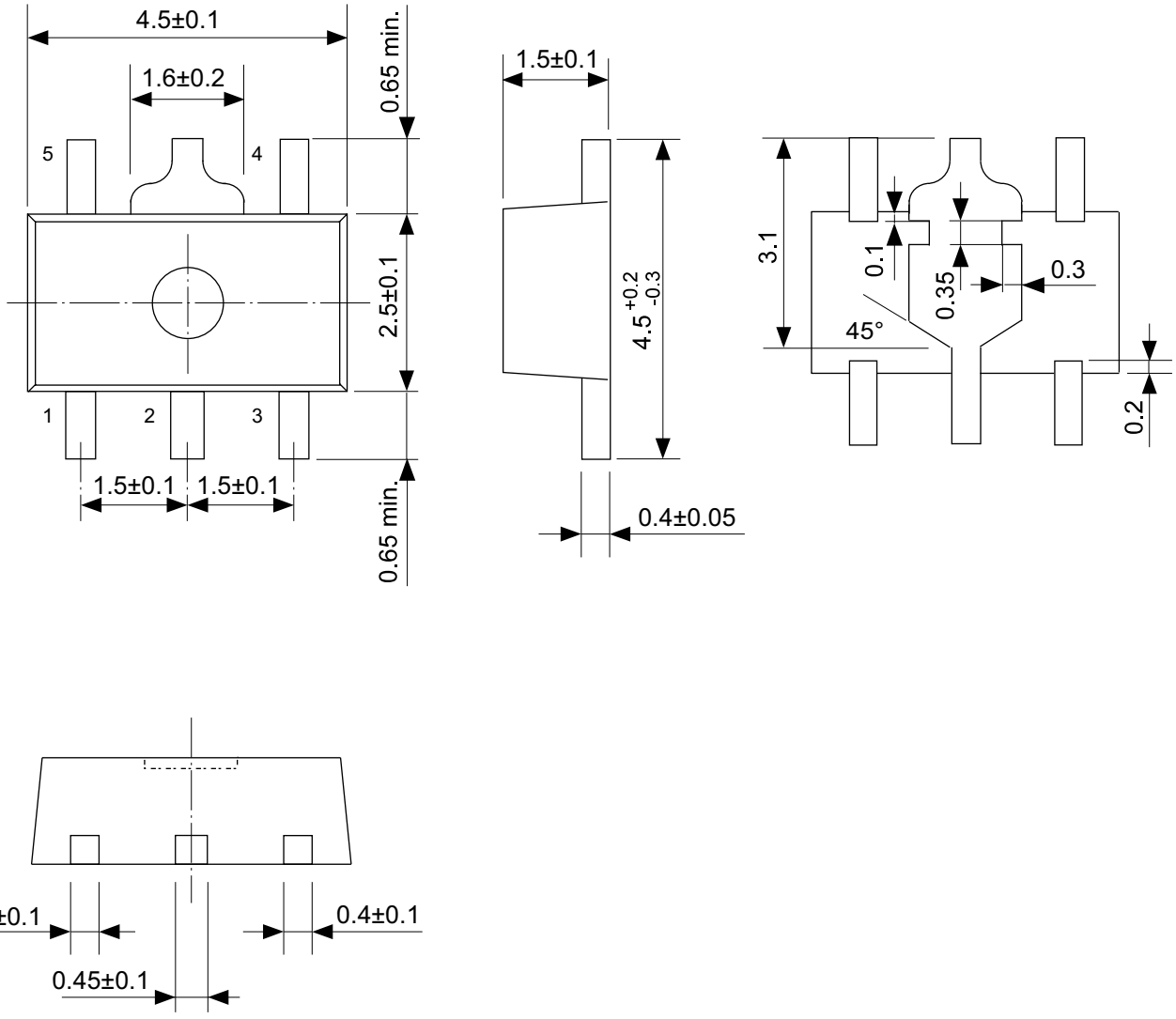
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

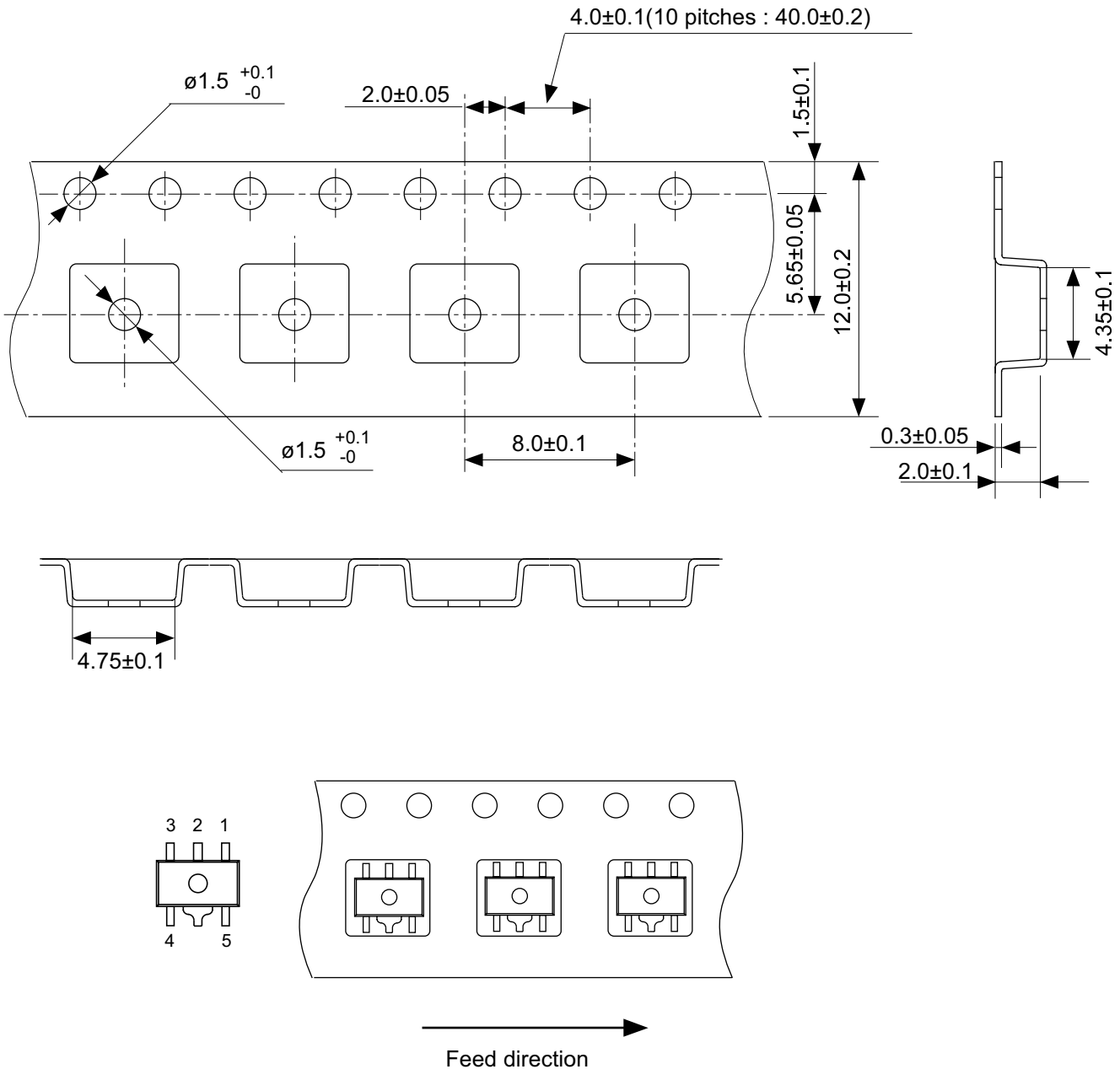
No. SOT23x-A-Board-SD-2.0



No. UP005-A-P-SD-2.0

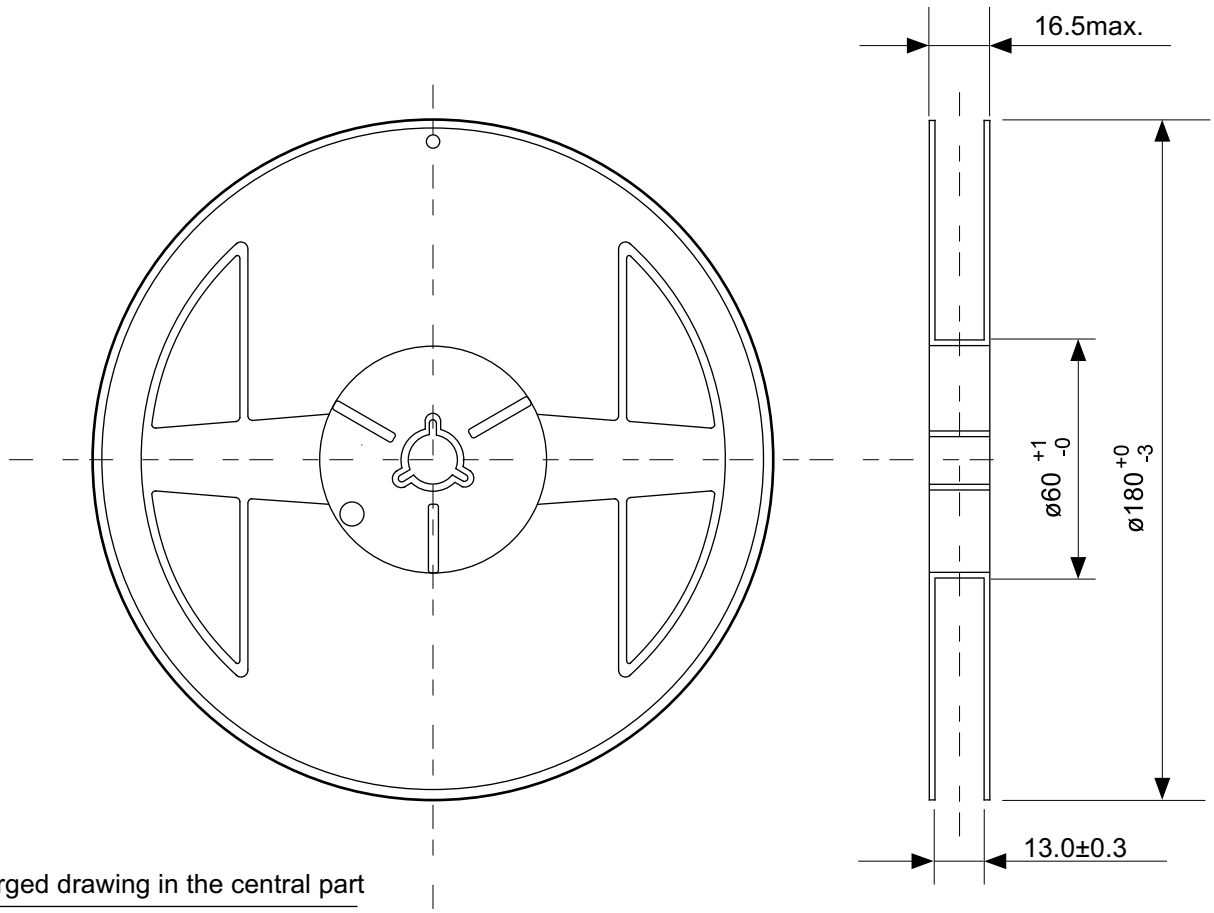
TITLE	SOT895-A-PKG Dimensions
No.	UP005-A-P-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.

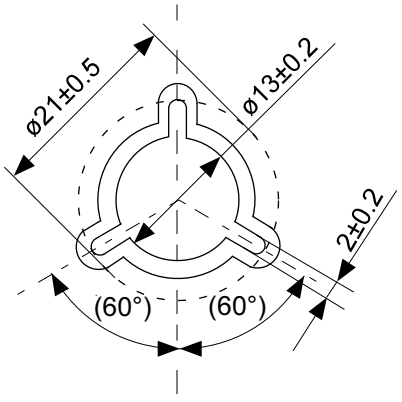


No. UP005-A-C-SD-2.0

TITLE	SOT895-A-Carrier Tape
No.	UP005-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

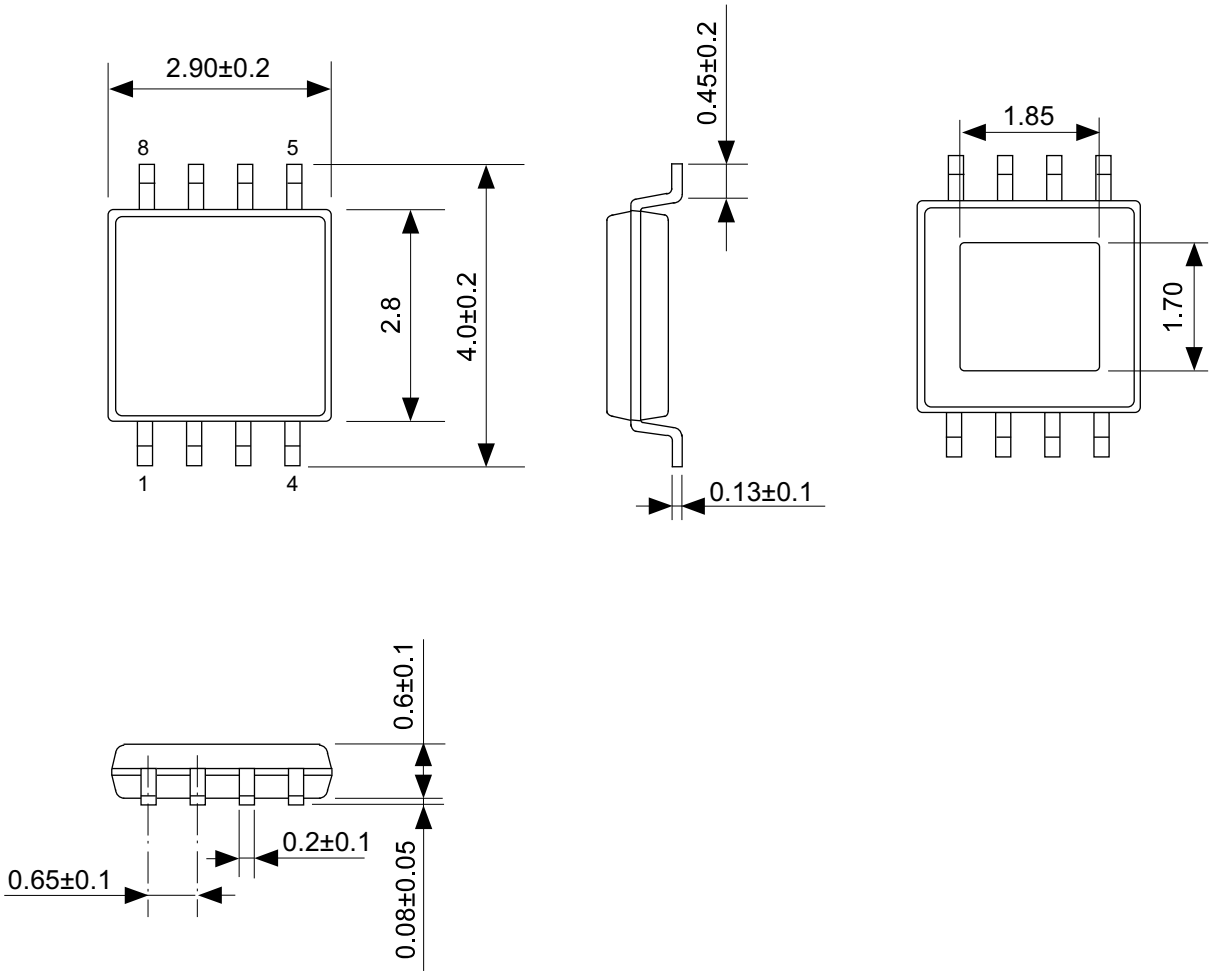


Enlarged drawing in the central part



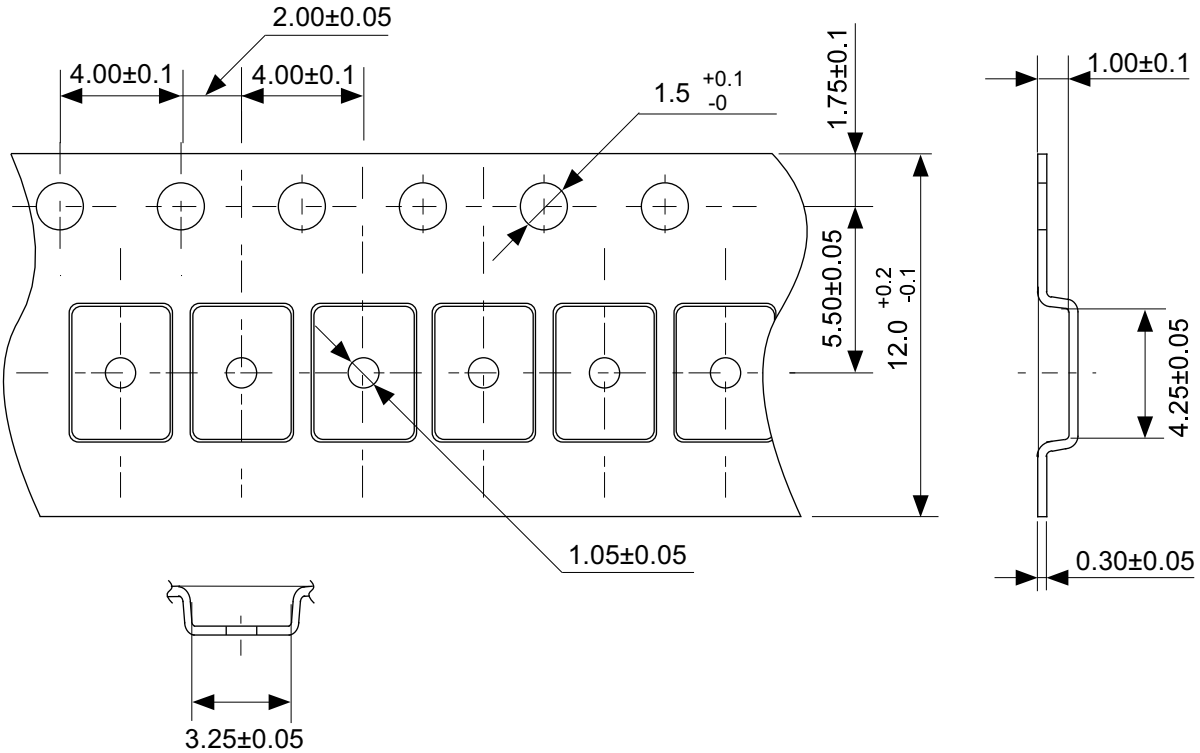
No. UP005-A-R-SD-1.1

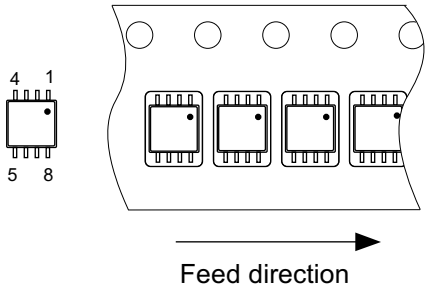
TITLE	SOT895-A-Reel		
No.	UP005-A-R-SD-1.1		
ANGLE		QTY.	1,000
UNIT	mm		
ABLIC Inc.			



No. FP008-A-P-SD-2.0

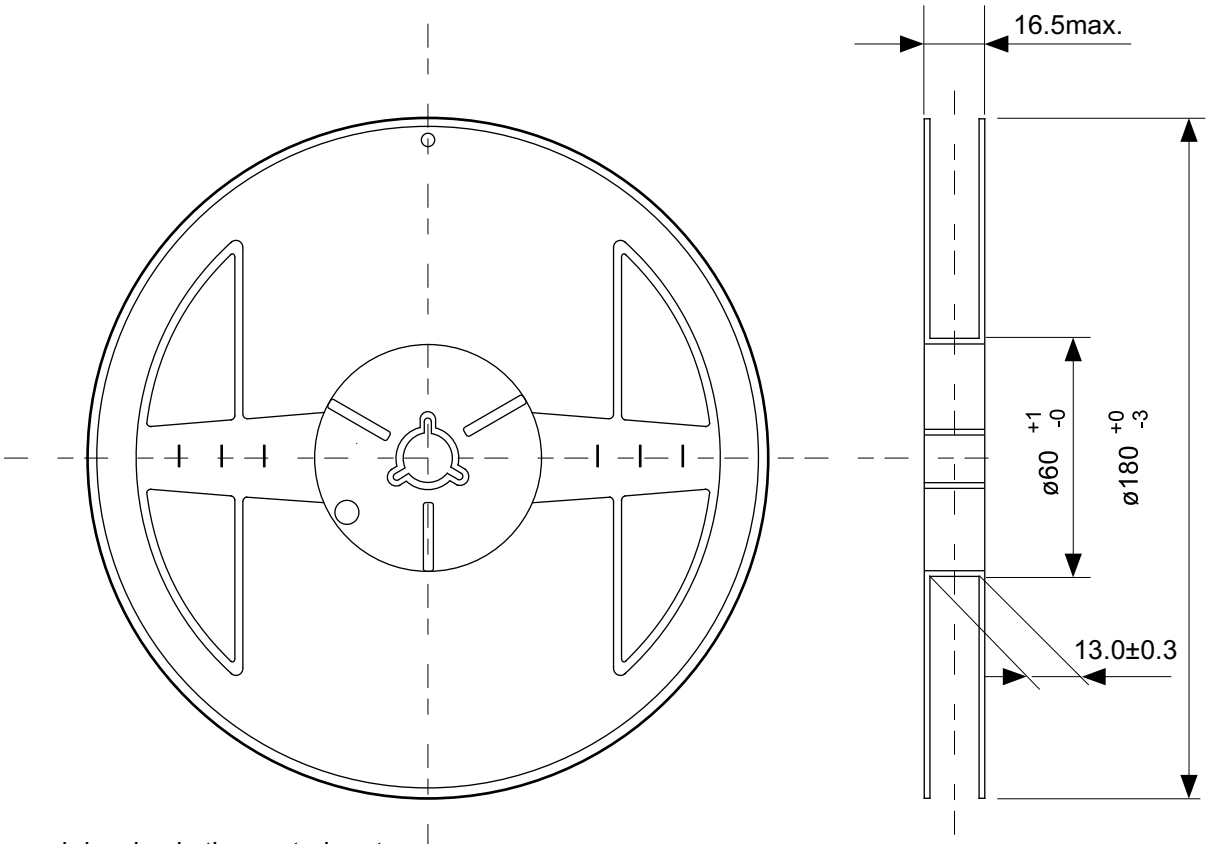
TITLE	HTMSOP8-A-PKG Dimensions
No.	FP008-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



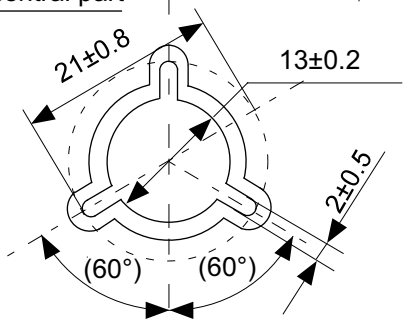


No. FP008-A-C-SD-1.0

TITLE	HTMSOP8-A-Carrier Tape
No.	FP008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

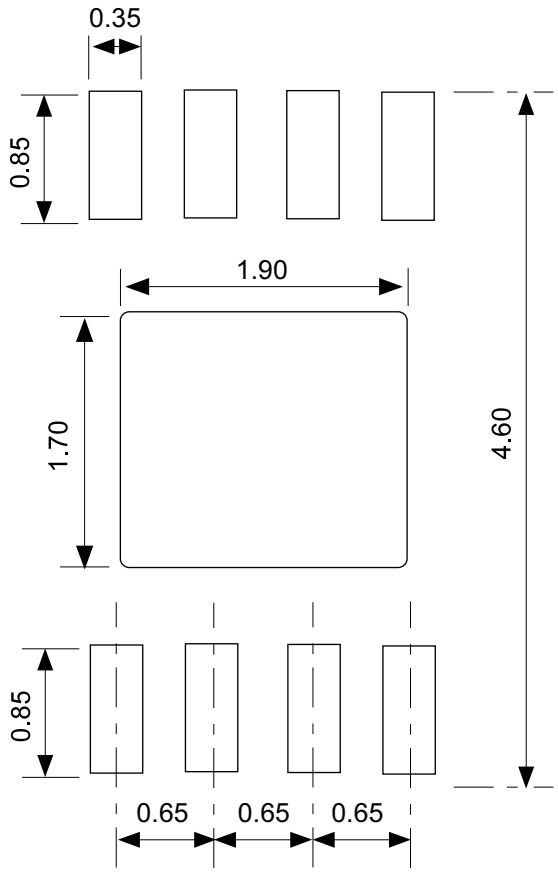


Enlarged drawing in the central part



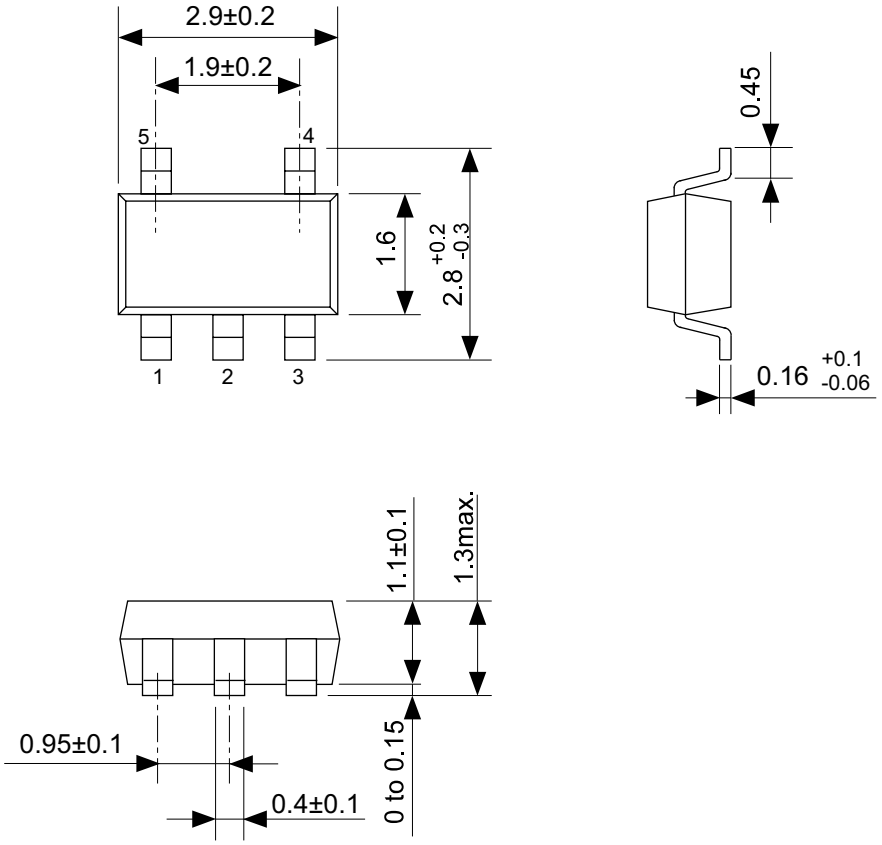
No. FP008-A-R-SD-1.0

TITLE	HTMSOP8-A-Reel		
No.	FP008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			



No. FP008-A-L-SD-2.0

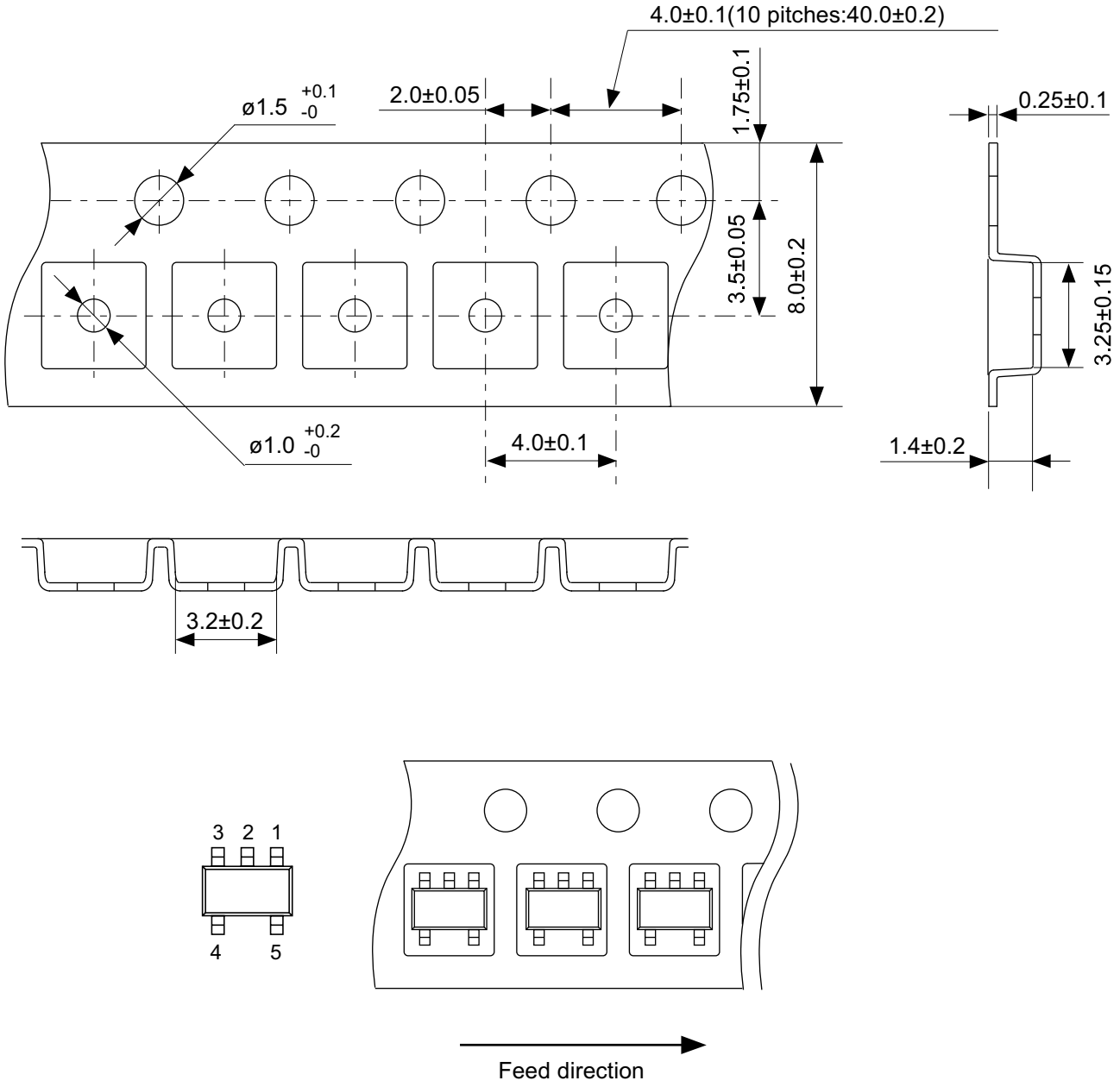
TITLE	HTMSOP8-A -Land Recommendation
No.	FP008-A-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



No. MP005-A-P-SD-1.3

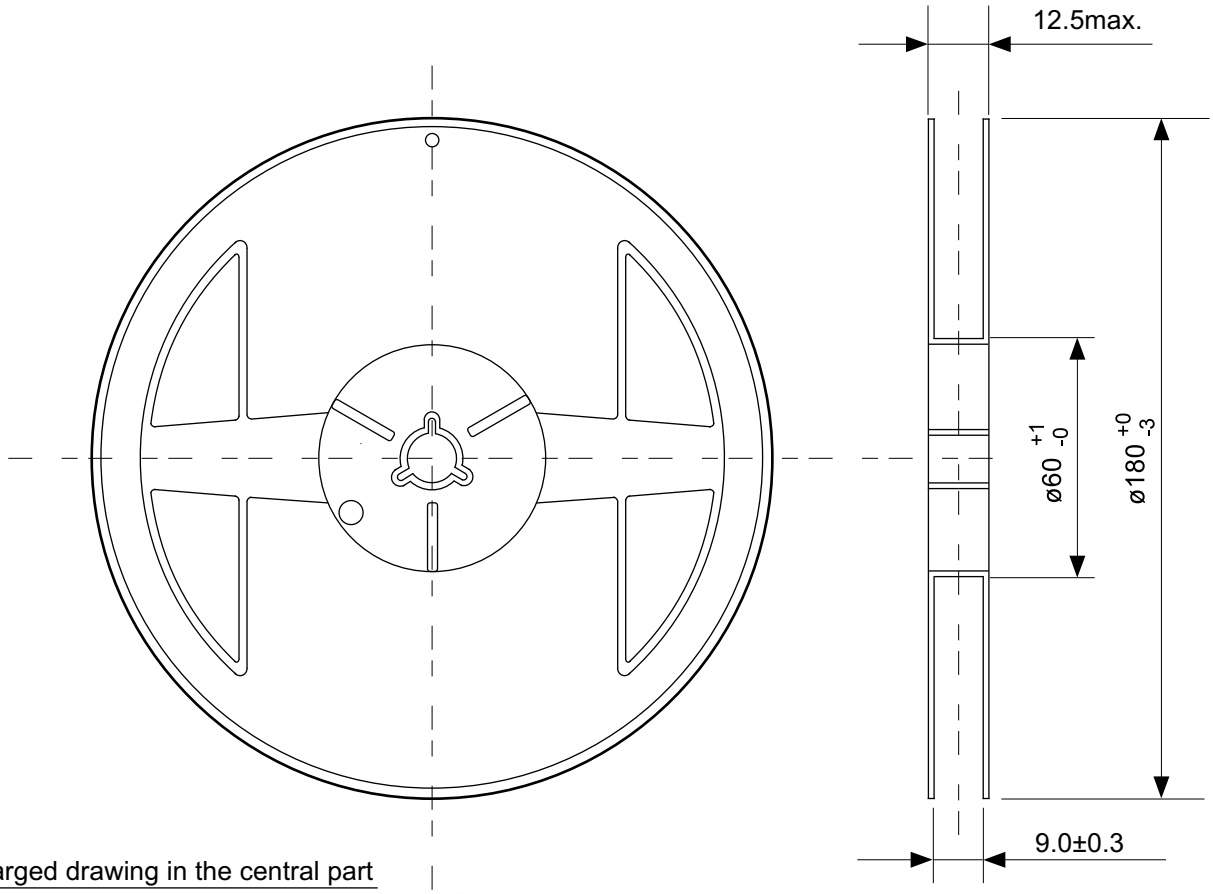
TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm

ABLIC Inc.

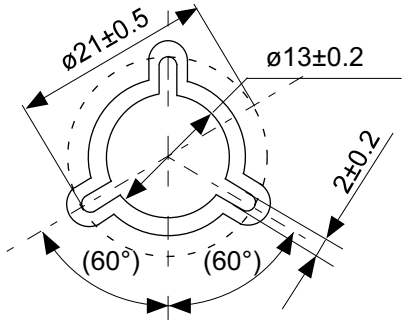


No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			

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   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
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2.4-2019.07