S-8224A/B Series

BATTERY PROTECTION IC FOR 2-SERIAL TO 4-SERIAL CELL PACK (SECONDARY PROTECTION)

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Rev.1.3_00

The S-8224A/B Series is used for secondary protection of lithium-ion rechargeable batteries, and incorporates high-accuracy voltage detection circuits and delay circuits.
Short-circuits between cells accommodate series connection of two cells to four cells.
The S-8224B Series limits its CO pin output voltage to 11.5 V max., so a FET with the gate withstand voltage of 12 V can be used.

■ Features

- High-accuracy voltage detection circuit for each cell
  - Overcharge detection voltage n (n = 1 to 4)
    - 3.600 V to 4.700 V (50 mV step) — Accuracy ±20 mV (Ta = +25°C); Accuracy ±25 mV (Ta = −10°C to +60°C)
  - Overcharge hysteresis voltage n (n = 1 to 4)[*1]
    - 0.0 mV to −550 mV (50 mV step)
    - −300 mV to −550 mV — Accuracy ±20%
    - −100 mV to −250 mV — Accuracy ±50 mV
    - −50 mV — Accuracy ±25 mV
    - 0.0 mV — Accuracy −25 mV to +20 mV
- Delay times for overcharge detection are generated only by an internal circuit (external capacitors are unnecessary)
  - Overcharge detection delay time is selectable: 1 s, 2 s, 4 s, 6 s, 8 s
  - Overcharge release delay time is selectable: 2 ms, 64 ms
- Built-in timer reset delay circuit
- Output control function via CTL pin
- Output form is selectable (S-8224A Series): CMOS output, Nch open-drain output
- Output logic is selectable (S-8224A Series): Active "H", active "L"
- CO pin output voltage is limited to 11.5 V max. (S-8224B Series)[*2]
- High-withstand voltage: Absolute maximum rating 28 V
- Wide operation voltage range: 3.6 V to 28 V
- Wide operation temperature range: Ta = −40°C to +85°C
- Low current consumption
  - During operation (V_{CU} − 1.0 V for each cell): 0.25 µA typ., 0.6 µA max. (Ta = +25°C)
  - During overdischarge (V_{CU} × 0.5 V for each cell): 0.3 µA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free

***1.** Select the overcharge hysteresis voltage calculated as the following formula.
(Overcharge detection voltage n) + (Overcharge hysteresis voltage n) ≥ 3.4 V

***2.** Only output logic active "H" is available.

■ Application

- Lithium-ion rechargeable battery packs (for secondary protection)

■ Package

- SNT-8A

■ Block Diagrams

1. S-8224A Series

1. 1 CMOS output product

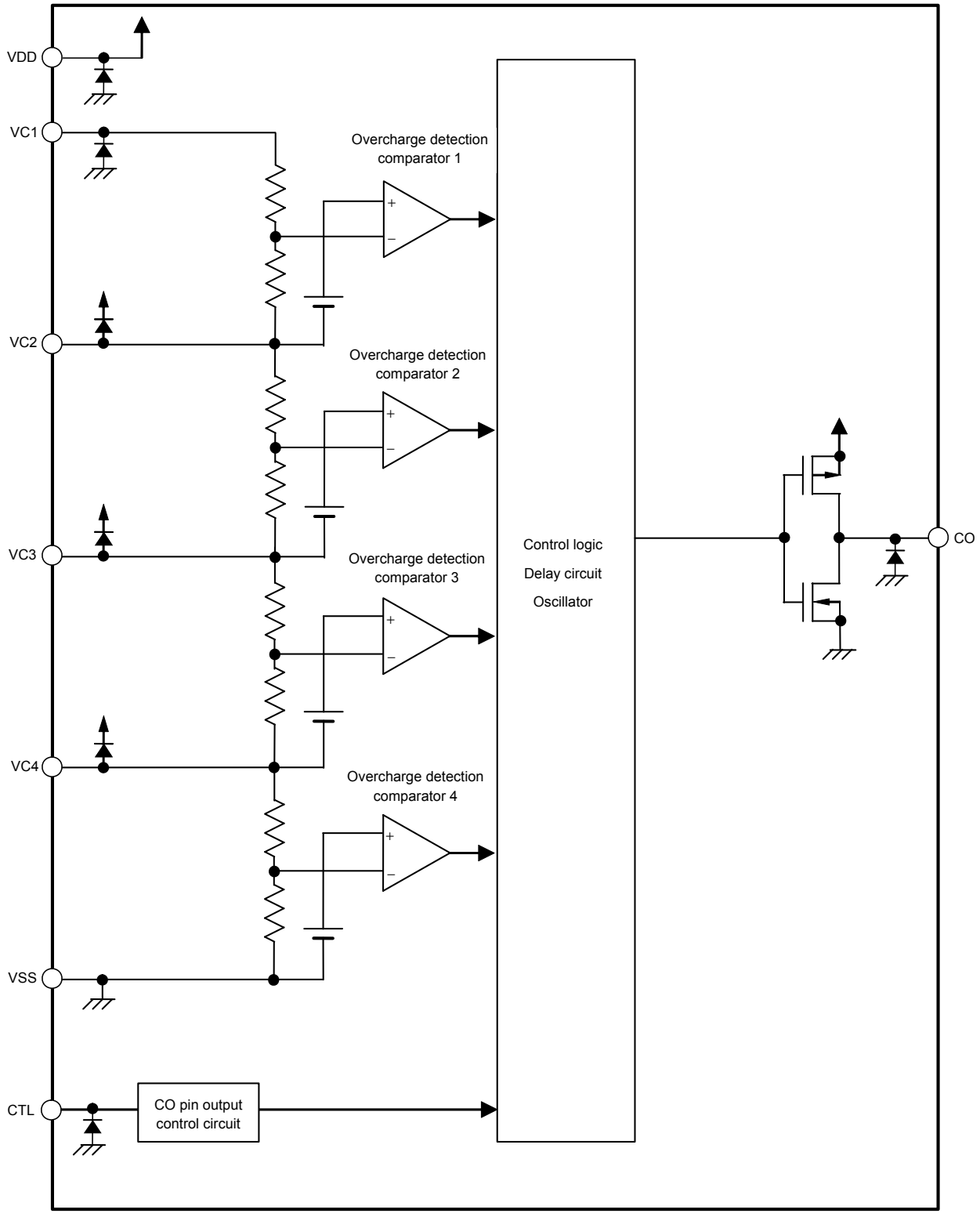


Figure 1

1. 2 Nch open-drain output product

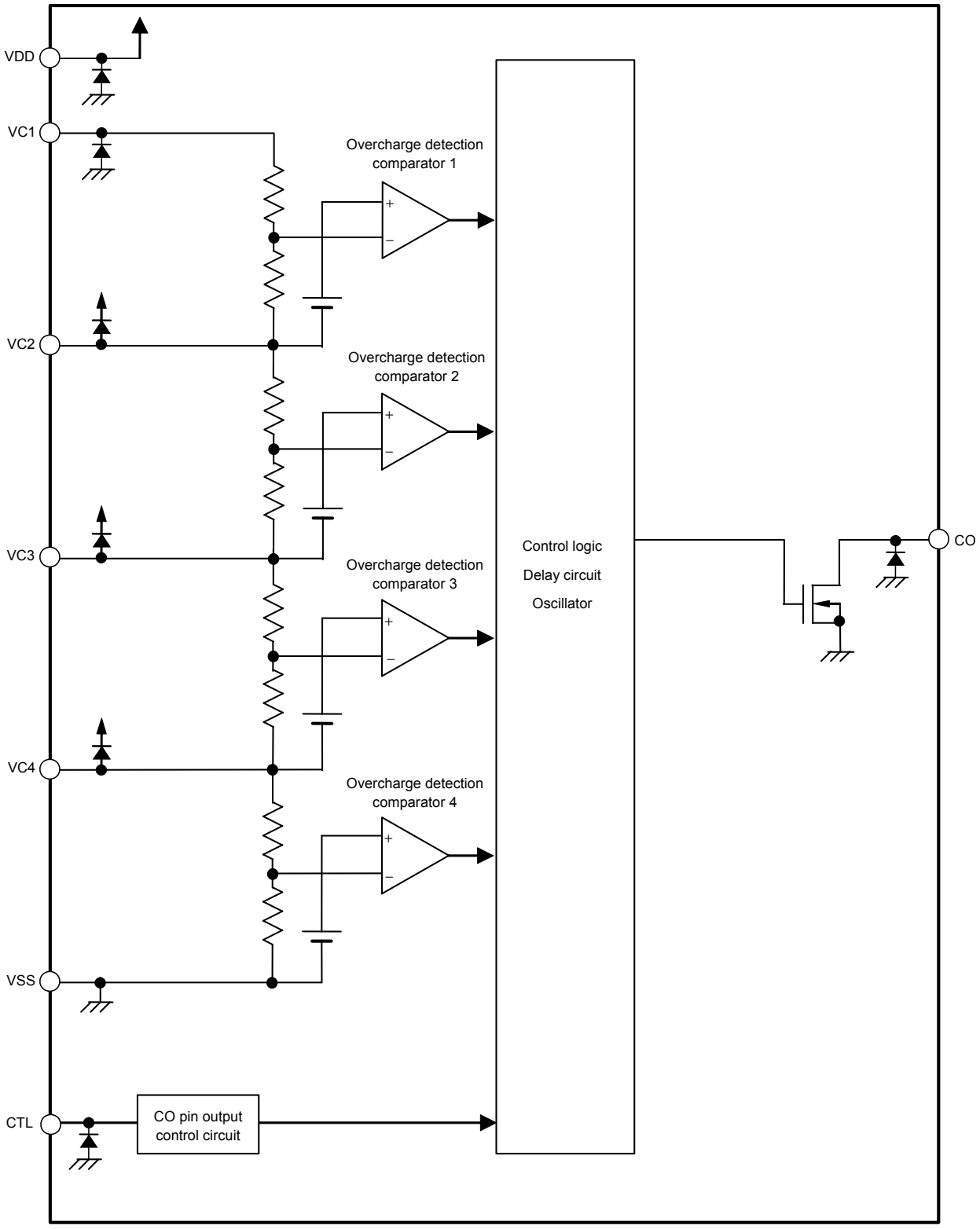


Figure 2

2. S-8224B Series

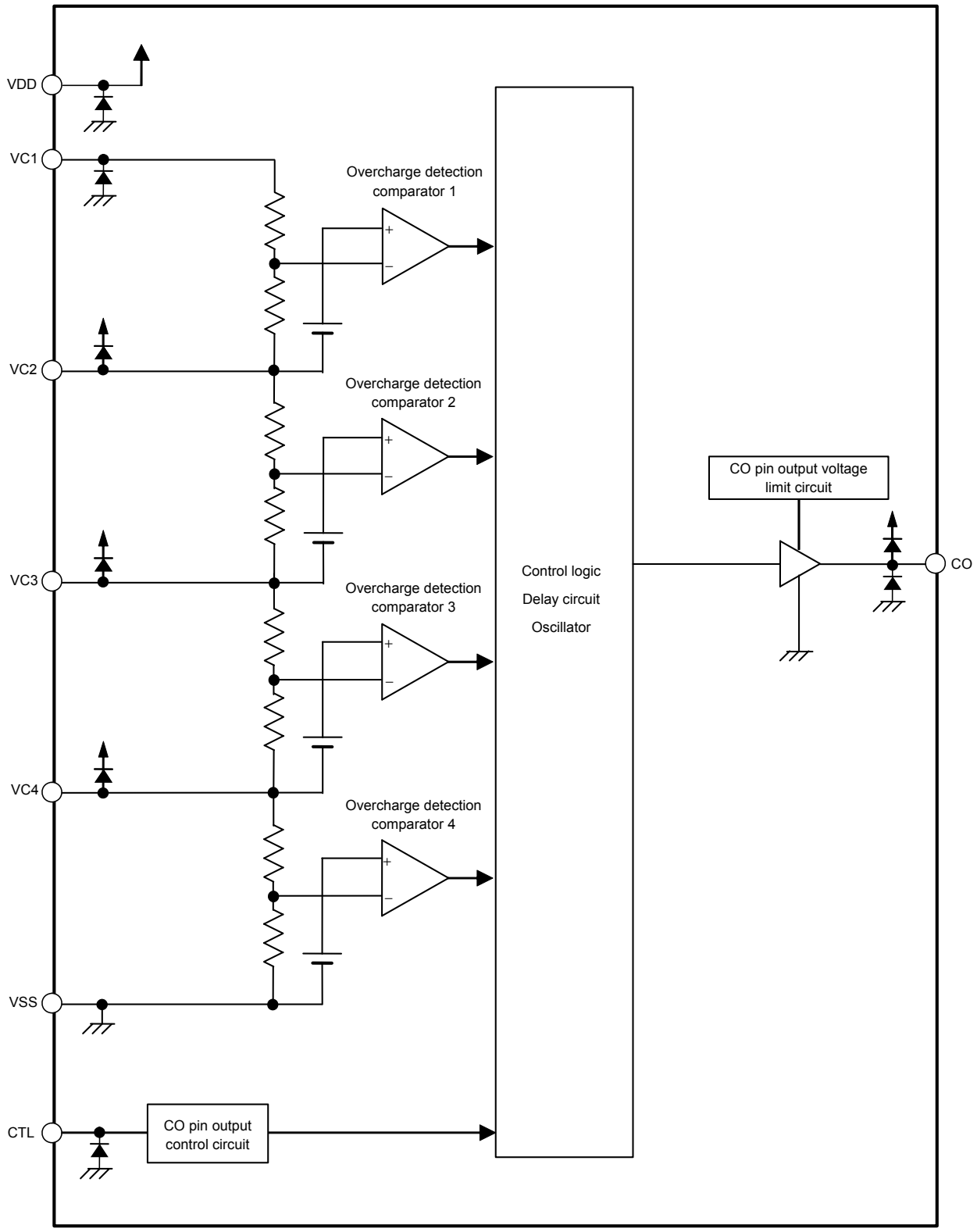
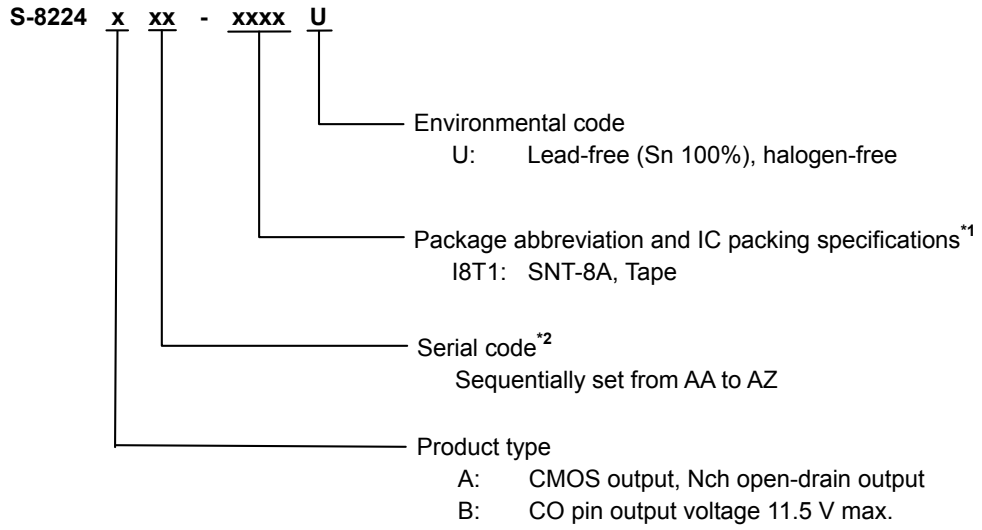


Figure 3

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

3. Product name list

3. 1 S-8224A Series

Table 2

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Hysteresis Voltage [V_{HC}]	Overcharge Detection Delay Time*1 [t_{CU}]	Overcharge Release Delay Time*2 [t_{CL}]	Output Form*3	Output Logic*4
S-8224AAS-I8T1U	4.450 V	−400 mV	4 s	64 ms	CMOS output	Active "H"
S-8224AAT-I8T1U	4.350 V	−400 mV	4 s	64 ms	CMOS output	Active "H"
S-8224AAU-I8T1U	4.500 V	−400 mV	4 s	64 ms	CMOS output	Active "H"
S-8224AAV-I8T1U	4.550 V	−400 mV	6 s	64 ms	CMOS output	Active "H"
S-8224AAW-I8T1U	4.450 V	−400 mV	6 s	64 ms	CMOS output	Active "H"
S-8224AAX-I8T1U	4.350 V	−400 mV	6 s	64 ms	CMOS output	Active "H"
S-8224ABA-I8T1U	4.400 V	−400 mV	6 s	64 ms	CMOS output	Active "H"
S-8224ABB-I8T1U	4.500 V	−400 mV	6 s	64 ms	CMOS output	Active "H"
S-8224ABC-I8T1U	4.600 V	−400 mV	4 s	64 ms	CMOS output	Active "H"
S-8224ABD-I8T1U	4.300 V	−400 mV	2 s	64 ms	CMOS output	Active "H"

***1.** Overcharge detection delay time 1 s / 2 s / 4 s / 6 s / 8 s is selectable.
***2.** Overcharge release delay time 2 ms / 64 ms is selectable.
***3.** Output form CMOS output / Nch open-drain output is selectable.
***4.** Output logic active "H" / active "L" is selectable.

Remark Please contact our sales office for the products with detection voltage value other than those specified above.

3. 2 S-8224B Series

Table 3

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Hysteresis Voltage [V_{HC}]	Overcharge Detection Delay Time*1 [t_{CU}]	Overcharge Release Delay Time*2 [t_{CL}]	Output Logic*3
S-8224BAA-I8T1U	4.350 V	−400 mV	4 s	2 ms	Active "H"
S-8224BAB-I8T1U	4.450 V	−400 mV	6 s	64 ms	Active "H"
S-8224BAC-I8T1U	4.350 V	−400 mV	4 s	64 ms	Active "H"

***1.** Overcharge detection delay time 1 s / 2 s / 4 s / 6 s / 8 s is selectable.
***2.** Overcharge release delay time 2 ms / 64 ms is selectable.
***3.** Only output logic active "H" is available.

Remark Please contact our sales office for the products with detection voltage value other than those specified above.

■ Pin Configuration

1. SNT-8A

Top view

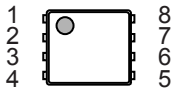


Figure 4

Table 4

Pin No.	Symbol	Description
1	VDD	Positive power supply input pin
2	VC1	Positive voltage connection pin of battery 1
3	VC2	Negative voltage connection pin of battery 1 Positive voltage connection pin of battery 2
4	VC3	Negative voltage connection pin of battery 2 Positive voltage connection pin of battery 3
5	VC4	Negative voltage connection pin of battery 3 Positive voltage connection pin of battery 4
6	VSS	Negative power supply input pin Negative voltage connection pin of battery 4
7	CTL	CO pin output control pin
8	CO	FET gate connection pin for charge control

■ Absolute Maximum Ratings

Table 5

(Ta = +25°C unless otherwise specified)

Item			Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin			V_{DS}	VDD	V_{SS} – 0.3 to V_{SS} + 28	V
Input pin voltage			V_{IN}	VC1	V_{SS} – 0.3 to V_{SS} + 28	V
				VC2, VC3, VC4	V_{DD} – 28 to V_{DD} + 0.3	V
				CTL	V_{SS} – 0.3 to V_{DD} + 0.3	V
CO pin output voltage	S-8224A Series	CMOS output	V_{CO}	CO	V_{SS} – 0.3 to V_{DD} + 0.3	V
		Nch open-drain output			V_{SS} – 0.3 to V_{SS} + 28	V
	S-8224B Series				V_{SS} – 0.3 to V_{DD} + 0.3	V
Operation ambient temperature			T_{opr}	–	–40 to +85	°C
Storage temperature			T_{stg}	–	–40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 6

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SNT-8A	Board A	–	211	–	°C/W
			Board B	–	173	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

Table 7

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage							
Overcharge detection voltage n (n = 1, 2, 3, 4)	V_{CUn}	Ta = +25°C	V_{CU} − 0.020	V_{CU}	V_{CU} + 0.020	V	1
		Ta = −10°C to +60°C*1	V_{CU} − 0.025	V_{CU}	V_{CU} + 0.025	V	1
Overcharge hysteresis voltage n (n = 1, 2, 3, 4)	V_{HCn}	−550 mV ≤ V_{HC} ≤ −300 mV	V_{HC} × 1.2	V_{HC}	V_{HC} × 0.8	V	1
		−250 mV ≤ V_{HC} ≤ −100 mV	V_{HC} − 0.050	V_{HC}	V_{HC} + 0.050	V	1
		V_{HC} = −50 mV	V_{HC} − 0.025	V_{HC}	V_{HC} + 0.025	V	1
		V_{HC} = 0.0 mV	V_{HC} − 0.025	V_{HC}	V_{HC} + 0.020	V	1
Input voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP}	−	3.6	−	28	V	−
CTL pin input voltage "H"	V_{CTLH}	−	V_{DD} × 0.95	−	−	V	2
CTL pin input voltage "L"	V_{CTLL}	−	−	−	V_{DD} × 0.4	V	2
Output voltage							
CO pin output voltage "H"	V_{COH}	S-8224B Series	5.0	8.0	11.5	V	2
Input Current							
Current consumption during operation	I_{OPE}	V1 = V2 = V3 = V4 = V_{CU} − 1.0 V	−	0.25	0.6	μA	3
Current consumption during overdischarge	I_{OPED}	V1 = V2 = V3 = V4 = V_{CU} × 0.5 V	−	−	0.3	μA	3
VC1 pin input current	I_{VC1}	V1 = V2 = V3 = V4 = V_{CU} − 1.0 V	−	−	0.3	μA	4
VCn pin input current (n = 2, 3, 4)	I_{VCn}	V1 = V2 = V3 = V4 = V_{CU} − 1.0 V	−0.3	0	0.3	μA	4
CTL pin input current "H"	I_{CTLH}	−	0.6	1.3	2.0	μA	4
CTL pin input current "L"	I_{CTLL}	−	−0.15	−	−	μA	4
Output Current							
CO pin source current	I_{COH}	S-8224A Series (CMOS output product), S-8224B Series	−	−	−20	μA	5
CO pin sink current	I_{COL}	−	20	−	−	μA	5
CO pin leakage current	I_{COLL}	S-8224A Series (Nch open-drain output product)	−	−	0.1	μA	5
Delay Time							
Overcharge detection delay time	t_{CU}	−	t_{CU} × 0.8	t_{CU}	t_{CU} × 1.2	s	1
Overcharge release delay time	t_{CL}	t_{CL} = 2 ms	1.6	2.0	3.0	ms	1
		t_{CL} = 64 ms	51.2	64	76.8	ms	1
Overcharge timer reset delay time	t_{TR}	−	6	12	20	ms	1
CTL pin response delay time	t_{CTL}	−	−	−	2.5	ms	2
Transition time to test mode	t_{TST}	−	−	−	10	ms	1

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

1. Overcharge detection voltage, overcharge hysteresis voltage (Test circuit 1)

Set SW1 to OFF in CMOS output product of the S-8224A Series and in the S-8224B Series, and set SW1 to ON in Nch open-drain output product of the S-8224A Series.

1. 1 Overcharge detection voltage n (V_{CUn})

Set V0 = 0 V, V1 = V2 = V3 = V4 = V_{CU} − 0.05 V in test circuit 1. The overcharge detection voltage 1 (V_{CU1}) is the V1 voltage when the CO pin output inverts after the voltage of V1 has been gradually increased.
Overcharge detection voltage (V_{CUn}) (n = 2 to 4) can be determined in the same way as when n = 1.

1. 2 Overcharge hysteresis voltage n (V_{HCn})

Set V0 = 0 V, V1 = V_{CU} + 0.05 V, V2 = V3 = V4 = 2.5 V. The overcharge hysteresis voltage 1 (V_{HC1}) is the difference between V1 voltage and V_{CU1} when the CO pin output inverts again after the V1 voltage has been gradually decreased.
Overcharge hysteresis voltage (V_{HCn}) (n = 2 to 4) can be determined in the same way as when n = 1.

2. CTL pin input voltage (Test circuit 2)

Set SW1 to OFF in CMOS output product of the S-8224A Series and in the S-8224B Series, and set SW1 to ON in Nch open-drain output product of the S-8224A Series.

2. 1 CTL pin input voltage "H" (V_{CTLH})

Set V1 = V2 = V3 = V4 = 3.5 V, V5 = 0 V. The CTL pin input voltage "H" (V_{CTLH}) is the V5 voltage when the CO pin output inverts after the voltage of V5 has been gradually increased.

2. 2 CTL pin input voltage "L" (V_{CTLL})

Set V5 =14 V. The CTL pin input voltage "L" (V_{CTLL}) is the V5 voltage when the CO pin output inverts after the voltage of V5 has been gradually decreased.

3. Output voltage (S-8224B Series) (Test circuit 2)

3. 1 CO pin output voltage "H"

The CO pin output voltage "H" (V_{COH}) is the voltage between the CO pin and the VSS pin when V1 = V2 = V3 = V4 = 3.5 V, V5 = 0 V.

4. Input current (Test circuit 4)

4. 1 CTL pin input current "H" (I_{CTLH})

Set SW2 and SW3 to ON and OFF, respectively.
The CTL pin input current "H" (I_{CTLH}) is the current that flows through the CTL pin when V1 = V2 = V3 = V4 = 3.5 V.

4. 2 CTL pin input current "L" (I_{CTLL})

Set SW2 and SW3 to OFF and ON, respectively.
The CTL pin input current "L" (I_{CTLL}) is the current that flows through the CTL pin when V1 = V2 = V3 = V4 = 3.5 V.

5. Output current (Test circuit 5)

5. 1 CMOS output product in S-8224A Series

Set SW4 and SW5 to OFF.

5. 1. 1 Active "H"

(1) CO pin source current (I_{COH})

Set SW4 to ON after setting V1 to V4 = 3.5 V, V5 = 0 V, V6 = 0.5 V. I1 is the CO pin source current (I_{COH}) at that time.

(2) CO pin sink current (I_{COL})

Set SW5 to ON after setting V1 to V4 = 3.5 V, V5 = 14 V, V7 = 0.5 V. I2 is the CO pin sink current (I_{COL}) at that time.

5. 1. 2 Active “L”

(1) CO pin source current (I_{COH})

Set SW4 to ON after setting V1 to V4 = 3.5 V, V5 = 14 V, V6 = 0.5 V. I1 is the CO pin source current (I_{COH}) at that time.

(2) CO pin sink current (I_{COL})

Set SW5 to ON after setting V1 to V4 = 3.5 V, V5 = 0 V, V7 = 0.5 V. I2 is the CO pin sink current (I_{COL}) at that time.

5. 2 Nch open-drain output product in S-8224A Series

Set SW4 and SW5 to OFF.

5. 2. 1 Active "H"

(1) CO pin leakage current (I_{COLL})

Set SW5 to ON after setting V1 to V4 = 7 V, V5 = 0 V, V7 = 28 V. I2 is the CO pin leakage current (I_{COLL}) at that time.

(2) CO pin sink current (I_{COL})

Set SW5 to ON after setting V1 to V4 = 3.5 V, V5 = 14 V, V7 = 0.5 V. I2 is the CO pin sink current (I_{COL}) at that time.

5. 2. 2 Active "L"

(1) CO pin leakage current (I_{COLL})

Set SW5 to ON after setting V1 to V4 = 3.5 V, V5 = 14 V, V7 = 28 V. I2 is the CO pin leakage current (I_{COLL}) at that time.

(2) CO pin sink current (I_{COL})

Set SW5 to ON after setting V1 to V4 = 3.5 V, V5 = 0 V, V7 = 0.5 V. I2 is the CO pin sink current (I_{COL}) at that time.

5. 3 S-8224B Series

Set SW4 and SW5 to OFF.

5. 3. 1 CO pin source current (I_{COH})

Set SW5 to ON after setting V1 to V4 = 3.5 V, V5 = 0 V, V7 = V_{COH} – 0.5 V. I2 is the CO pin source current (I_{COH}) at that time.

5. 3. 2 CO pin sink current (I_{COL})

Set SW5 to ON after setting V1 to V4 = 3.5 V, V5 = 14 V, V7 = 0.5 V. I2 is the CO pin sink current (I_{COL}) at that time.

6. Overcharge detection delay time (t_{CU}), overcharge release delay time (t_{CL}) (Test circuit 1)

Set SW1 to OFF in CMOS output product of the S-8224A Series and in the S-8224B Series, and set SW1 to ON in Nch open-drain output product of the S-8224A Series.
Increase V1 up to 5.2 V after setting V0 = 0 V, V1 = V2 = V3 = V4 = 3.5 V. The overcharge detection delay time (t_{CU}) is the time period until the CO pin output inverts. After that, decrease V1 down to 3.5 V. The overcharge release delay time (t_{CL}) is the time period until the CO pin output inverts.

7. CTL pin response delay time (t_{CTL}) (Test circuit 2)

Set SW1 to OFF in CMOS output product of the S-8224A Series and in the S-8224B Series, and set SW1 to ON in Nch open-drain output product of the S-8224A Series.
Decrease V5 down to 0 V after setting V1 = V2 = V3 = V4 = 3.5 V, V5 = 14 V. The CTL pin response delay time (t_{CTL}) is the time period until the CO pin output inverts.

8. Overcharge timer reset delay time (t_{TR}) (Test circuit 1)

Set SW1 to OFF in CMOS output product of the S-8224A Series and in the S-8224B Series, and set SW1 to ON in Nch open-drain output product of the S-8224A Series.
Increase V1 up to 5.2 V (first rise), and decrease V1 down to 3.5 V within the overcharge detection delay time (t_{CU}) after setting V0 = 0 V, V1 = V2 = V3 = V4 = 3.5 V. After that, increase V1 up to 5.2 V again (second rise), and detect the time period until the CO pin output inverts.
When the period from when V1 has fallen to the second rise is short, CO pin output inverts after t_{CU} has elapsed since the first rise. If the period is gradually made longer, CO pin output inverts after t_{CU} has elapsed since the second rise.
The overcharge timer reset delay time (t_{TR}) is the period from V1 fall until the second rise at that time.

9. Transition time to test mode (t_{TST}) (Test circuit 1)

Set SW1 to OFF in CMOS output product of the S-8224A Series and in the S-8224B Series, and set SW1 to ON in Nch open-drain output product of the S-8224A Series.
Increase V0 up to 8.5 V, and decrease V0 again to 0 V after setting V0 = 0 V, V1 = V2 = V3 = V4 = 3.5 V.
When the period from when V0 was raised to when it has fallen is short, if an overcharge detection operation is performed subsequently, the delay time is t_{CU}. However, when the period from when V0 is raised to when it has fallen is gradually made longer, the delay time during the subsequent overcharge detection operation is shorter than t_{CU}. The transition time to test mode (t_{TST}) is the period from when V0 was raised to when it has fallen at that time.

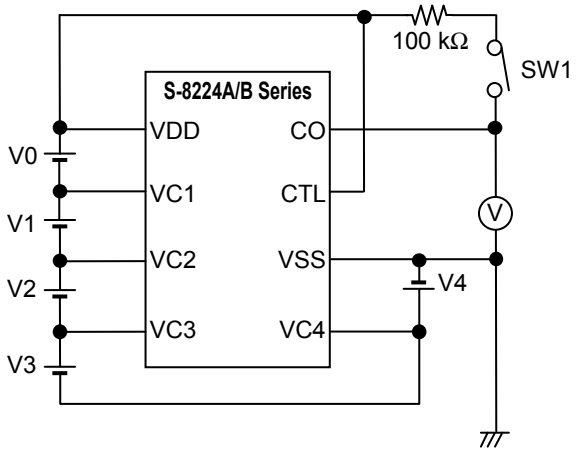


Figure 5 Test Circuit 1

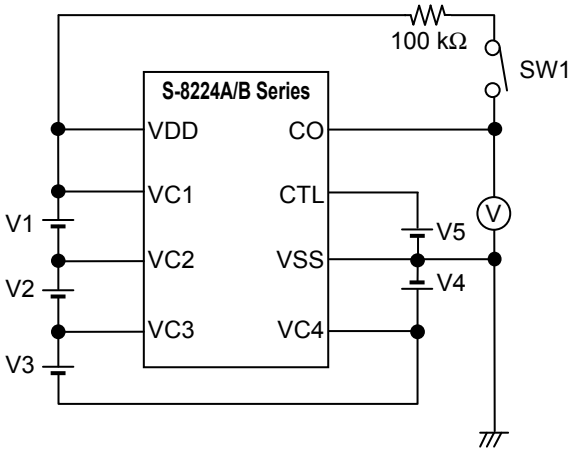


Figure 6 Test Circuit 2

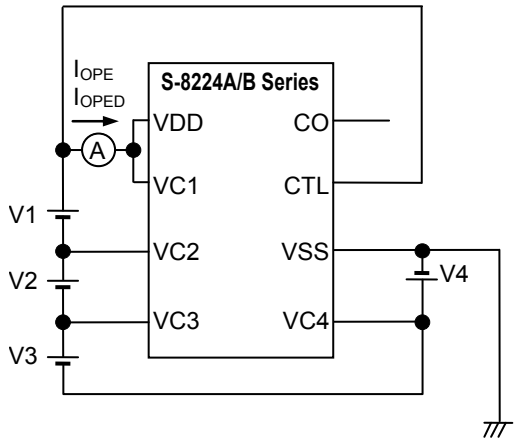


Figure 7 Test Circuit 3

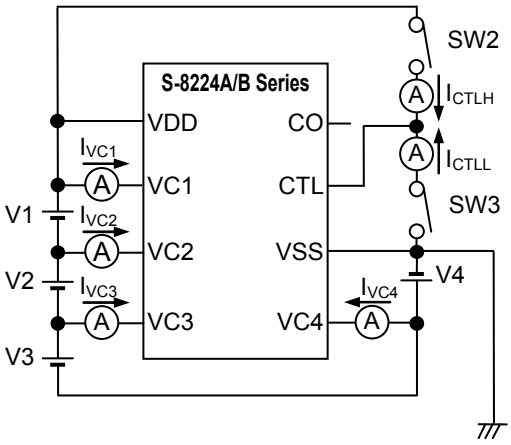


Figure 8 Test Circuit 4

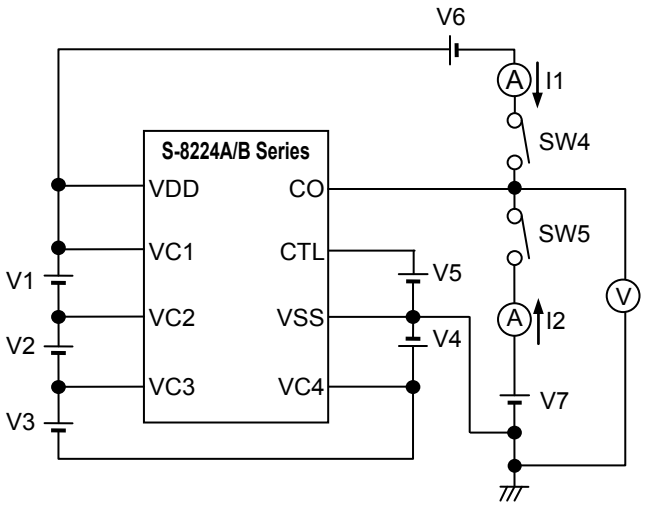


Figure 9 Test Circuit 5

■ Operation

Remark Refer to "■ **Battery Protection IC Connection Examples**".

1. Normal status

If the voltage of each of the batteries is lower than "the overcharge detection voltage (V_{CU}) + the overcharge hysteresis voltage (V_{HC})", the CO pin output changes to "L" (active "H") or "H" (active "L"). This is called normal status.

2. Overcharge status

When the voltage of one of the batteries exceeds V_{CU} during charging under normal conditions and the status is retained for the overcharge detection delay time (t_{CU}) or longer, CO pin output inverts. This status is called overcharge status. Connecting FET to the CO pin provides charge control and a second protection.
If the voltage of each of the batteries is lower than $V_{CU} + V_{HC}$ and the status is retained for the overcharge release delay time (t_{CL}) or longer, S-8224A/B Series changes to normal status.

3. Overcharge timer reset function

When an overcharge release noise that forces the voltage of one of the batteries temporarily below V_{CU} is input during t_{CU} from when V_{CU} is exceeded to when charging is stopped, t_{CU} is continuously counted if the time the overcharge release noise persists is shorter than the overcharge timer reset delay time (t_{TR}). Under the same conditions, if the time the overcharge release noise persists is t_{TR} or longer, counting of t_{CU} is reset once. After that, when V_{CU} has been exceeded, counting t_{CU} resumes.

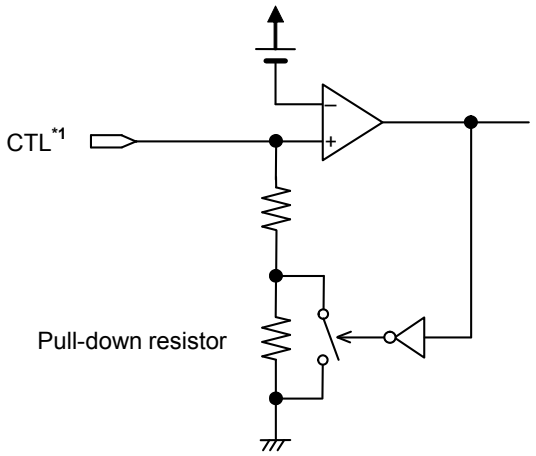
4. CTL pin

The S-8224A/B Series has control pins.
In the S-8224A/B Series, the CTL pin is used to control the output voltage of the CO pin. The CTL pin takes precedence over the overcharge detection circuit.

Table 8 Status Set by CTL Pin

CTL Pin	CO Pin
"H"	Normal status*1
Open	Detection status
"L"	Detection status

***1.** The status is controlled by the overcharge detection circuit.



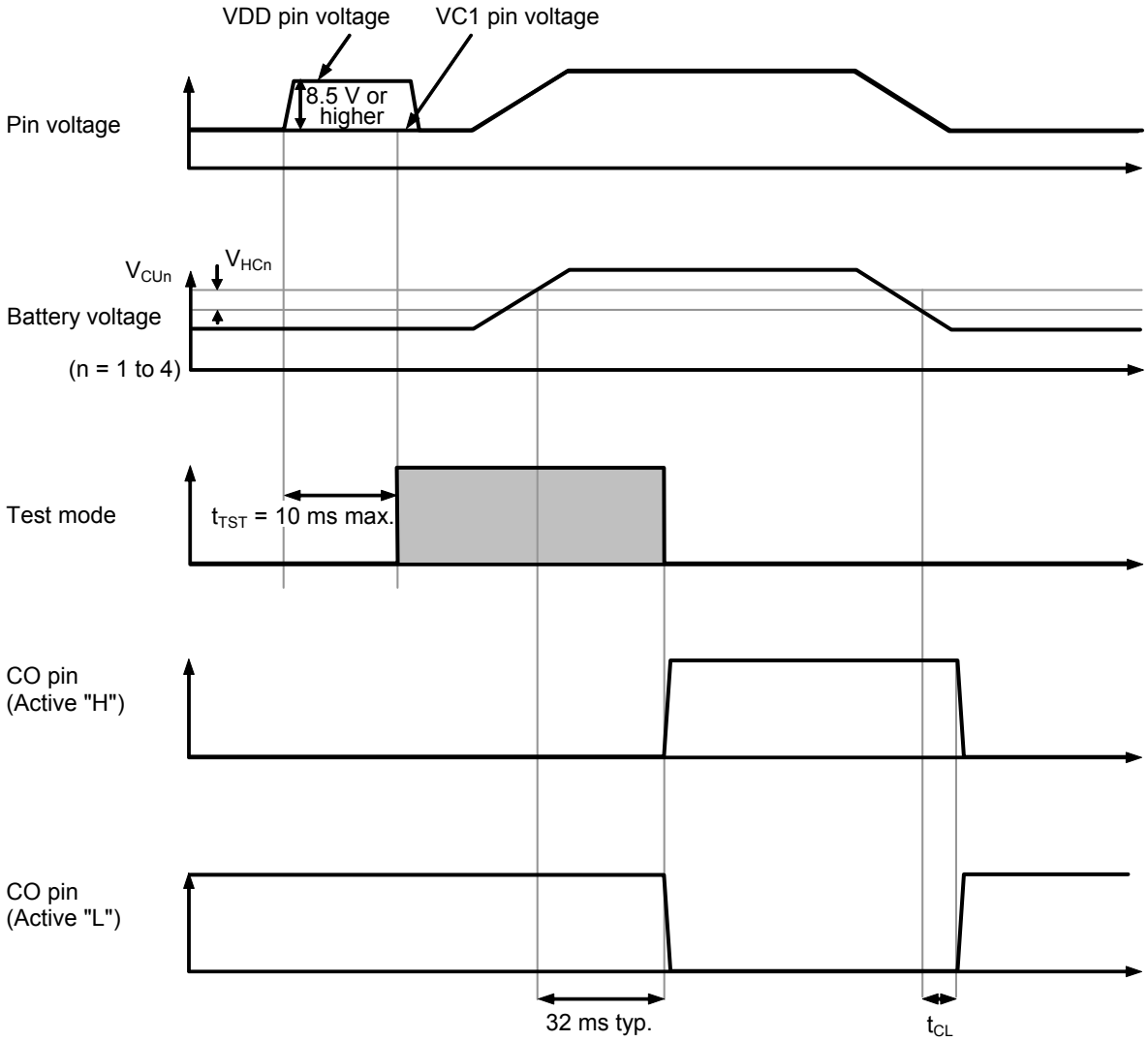
***1.** In the S-8224A/B Series, the inversion voltage "H" to "L" or "L" to "H" of the CTL pin is the VDD pin voltage − 2.8 V typ., and does not have the hysteresis.

Figure 10 Internal Equivalent Circuit of CTL Pin

Caution In the S-8224A/B Series, since the CTL pin implements high resistance of 7 MΩ to 24 MΩ for pull down, be careful of external noise application. If an external noise is applied, the CO pin may become "H". Perform thorough evaluation using the actual application.

5. Test mode

In the S-8224A/B Series, the overcharge detection delay time (t_{CU}) can be shortened by entering the test mode.
The test mode can be set by retaining the VDD pin voltage 8.5 V or more higher than the VC1 pin voltage for at least 10 ms (V1 = V2 = V3 = V4 = 3.5 V, Ta = +25 °C). The status is retained by the internal latch and the test mode is retained even if the VDD pin voltage is decreased to the same voltage as that of the VC1 pin.
If the CO pin becomes detection status when the delay time has elapsed after overcharge detection, the latch for retaining the test mode is reset and the S-8224A/B Series exits from the test mode.



Caution 1. Set the test mode when no batteries are overcharged.
2. The overcharge timer reset delay time (t_{TR}) is not shortened in the test mode.

Figure 11

■ Timing Charts

1. Overcharge detection operation

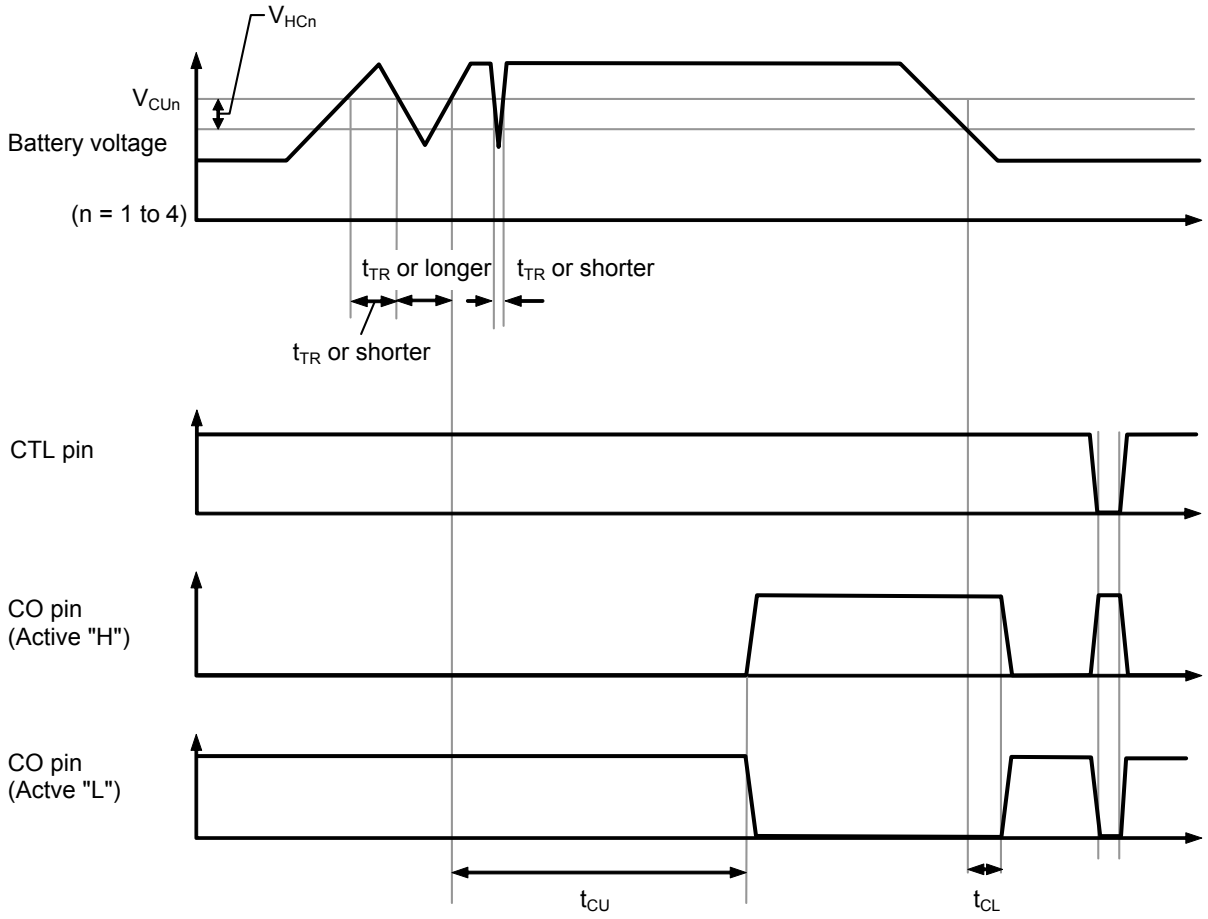


Figure 12

2. Overcharge timer reset operation

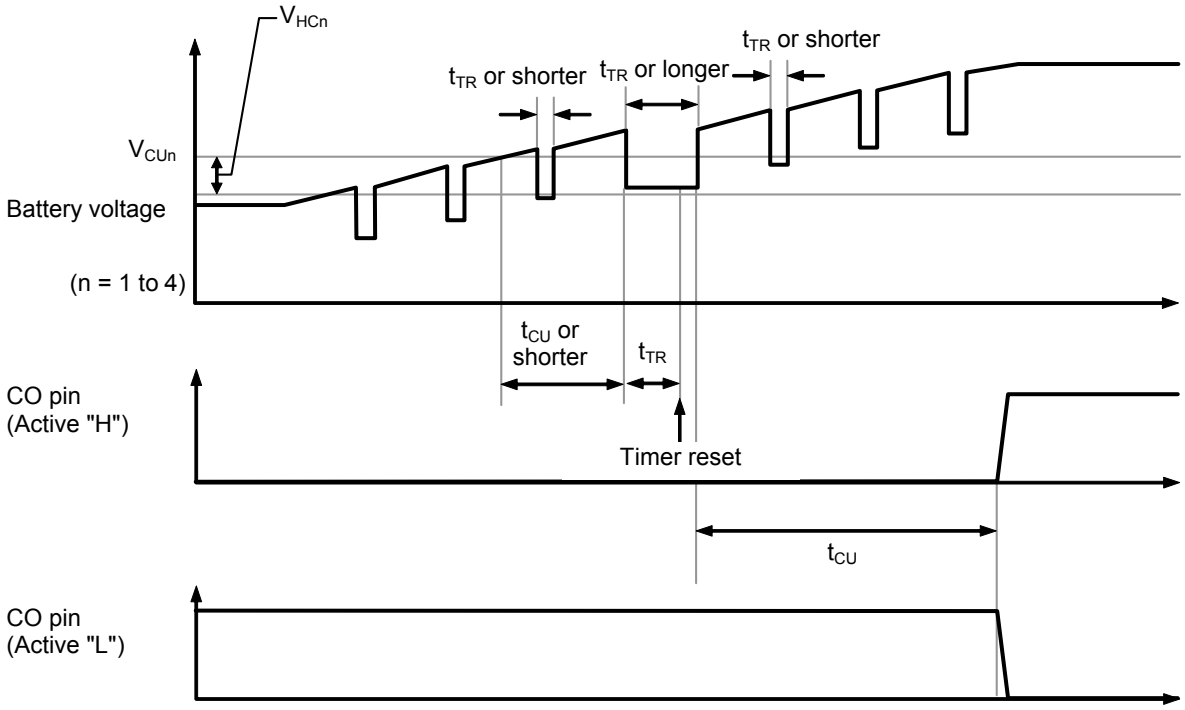
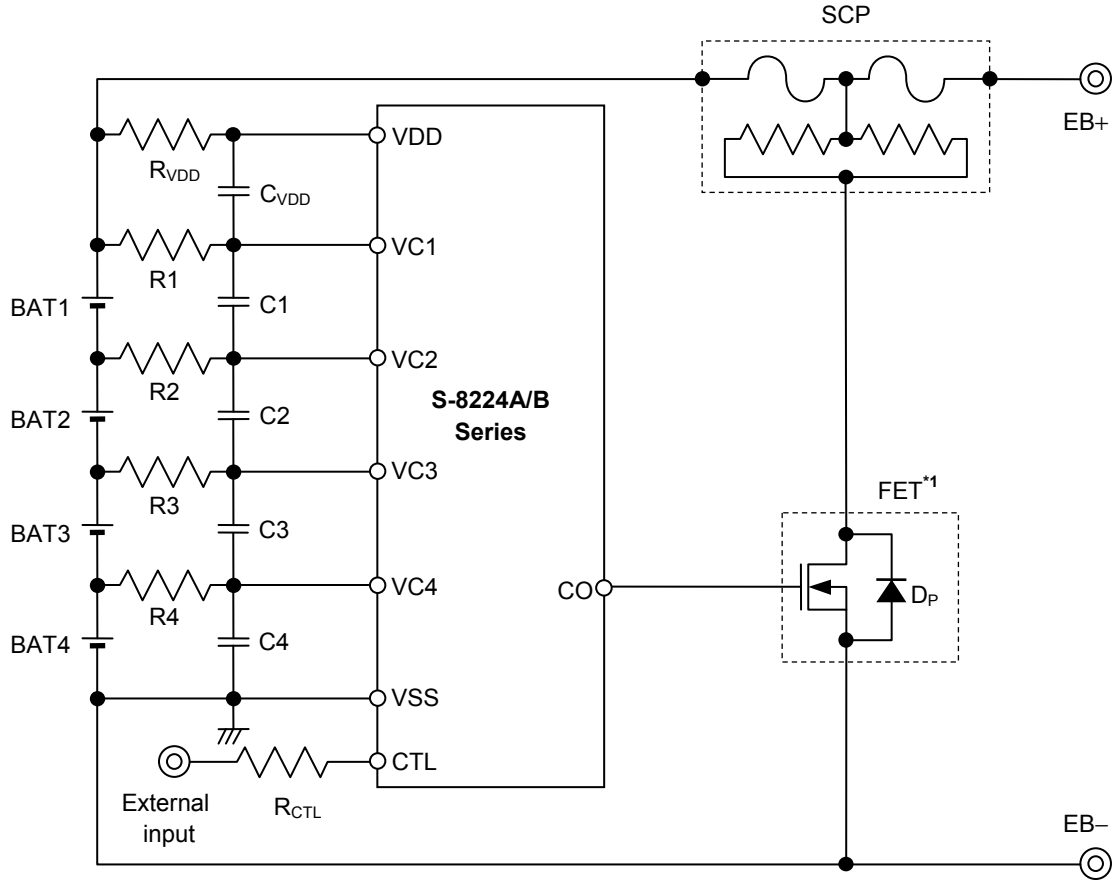


Figure 13

■ Battery Protection IC Connection Examples

1. 4-serial cell



***1.** The S-8224B Series limits its CO pin output voltage to 11.5 V max., so a FET with the gate withstand voltage of 12 V can be used.

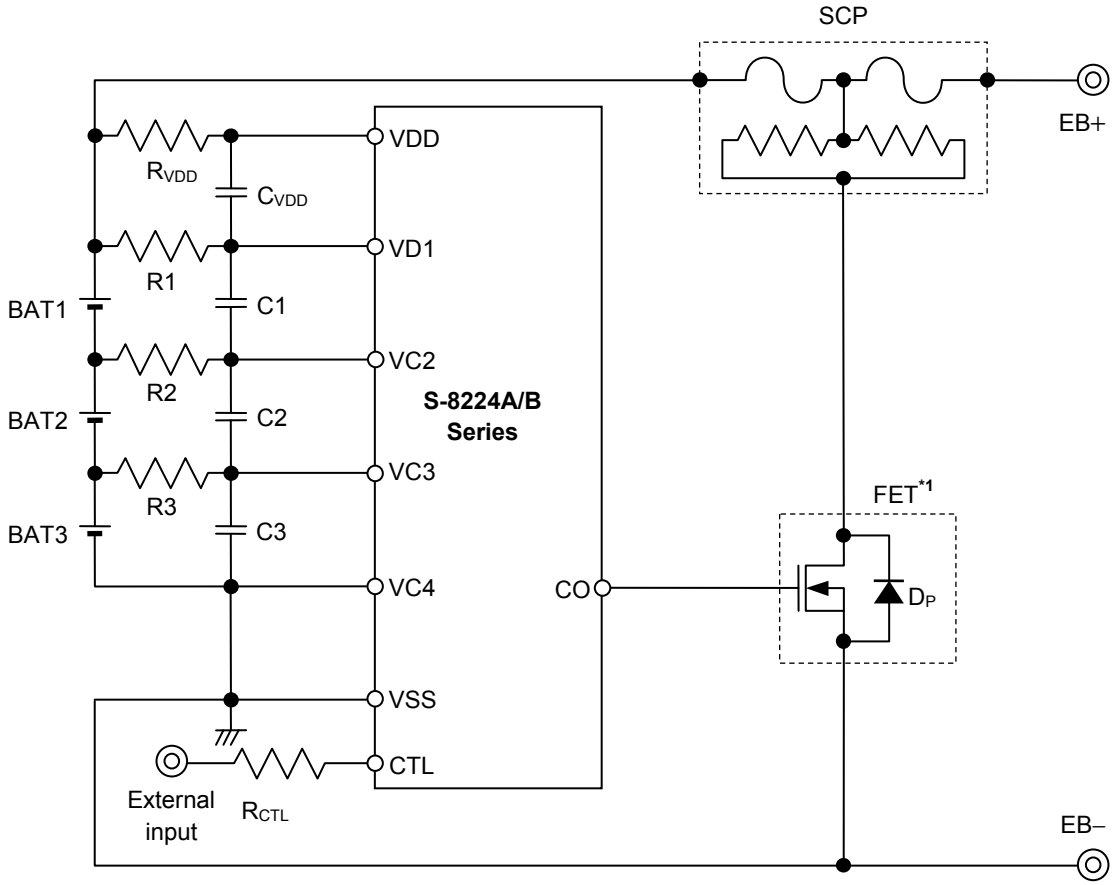
Figure 14

Table 9 Constants for External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R4	0.3	1	10	kΩ
2	C1 to C4, C_{VDD}	0.01	0.1	1	μF
3	R_{VDD}	300	330	1000	Ω

Caution
1. **The above constants are subject to change without prior notice.**
2. **It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**
3. **Set the same constants to R1 to R4 and to C1 to C4 and C_{VDD}.**
4. **Since the CO pin may become detection status transiently when the battery is being connected, be sure to connect the positive terminal of BAT1 last in order to prevent the terminal protection fuse from cutoff.**

2. 3-serial cell



***1.** The S-8224B Series limits its CO pin output voltage to 11.5 V max., so a FET with the gate withstand voltage of 12 V can be used.

Figure 15

Table 10 Constants for External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R3	0.3	1	10	kΩ
2	C1 to C3, C_{VDD}	0.01	0.1	1	μF
3	R_{VDD}	300	330	1000	Ω

Caution
1. **The above constants are subject to change without prior notice.**
2. **It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**
3. **Set the same constants to R1 to R3 and to C1 to C3 and C_{VDD}.**
4. **Since the CO pin may become detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the protection fuse from cutoff.**

3. 2-serial cell

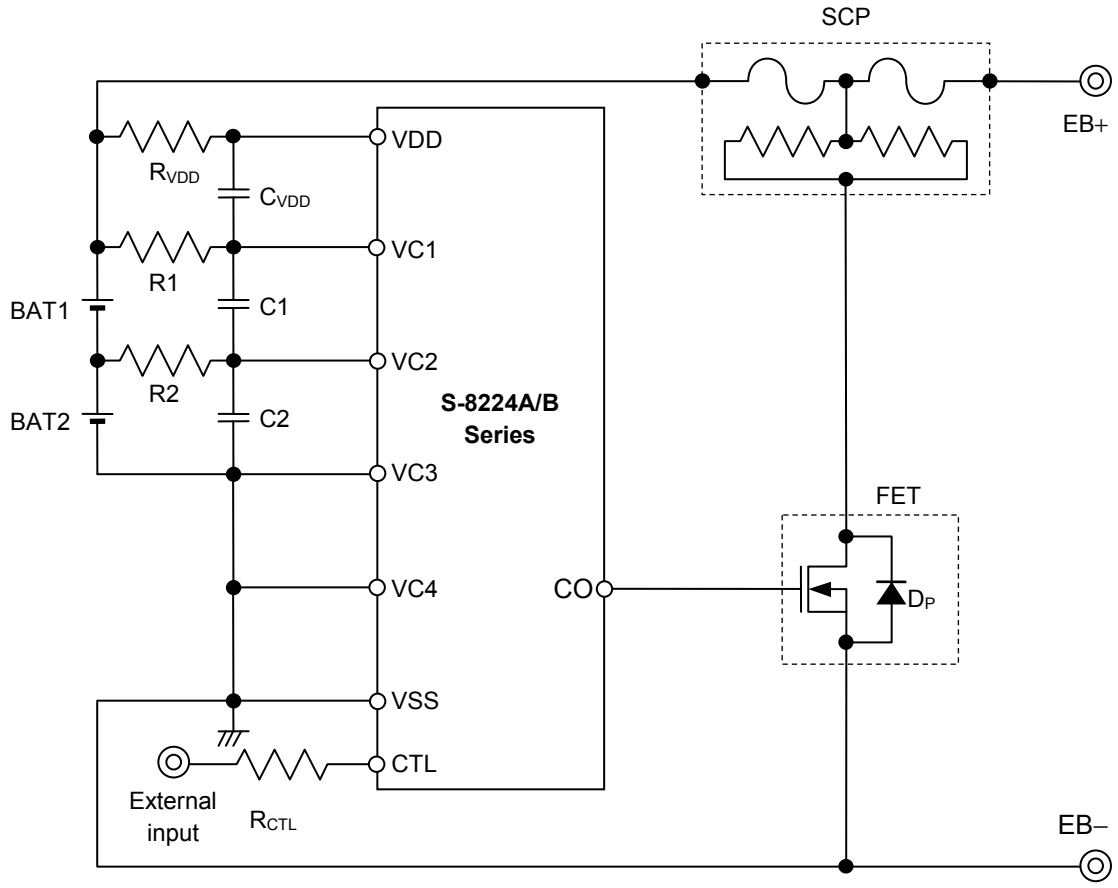


Figure 16

Table 11 Constants for External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R2	0.3	1	10	kΩ
2	C1 to C2, C_{VDD}	0.01	0.1	1	μF
3	R_{VDD}	300	330	1000	Ω

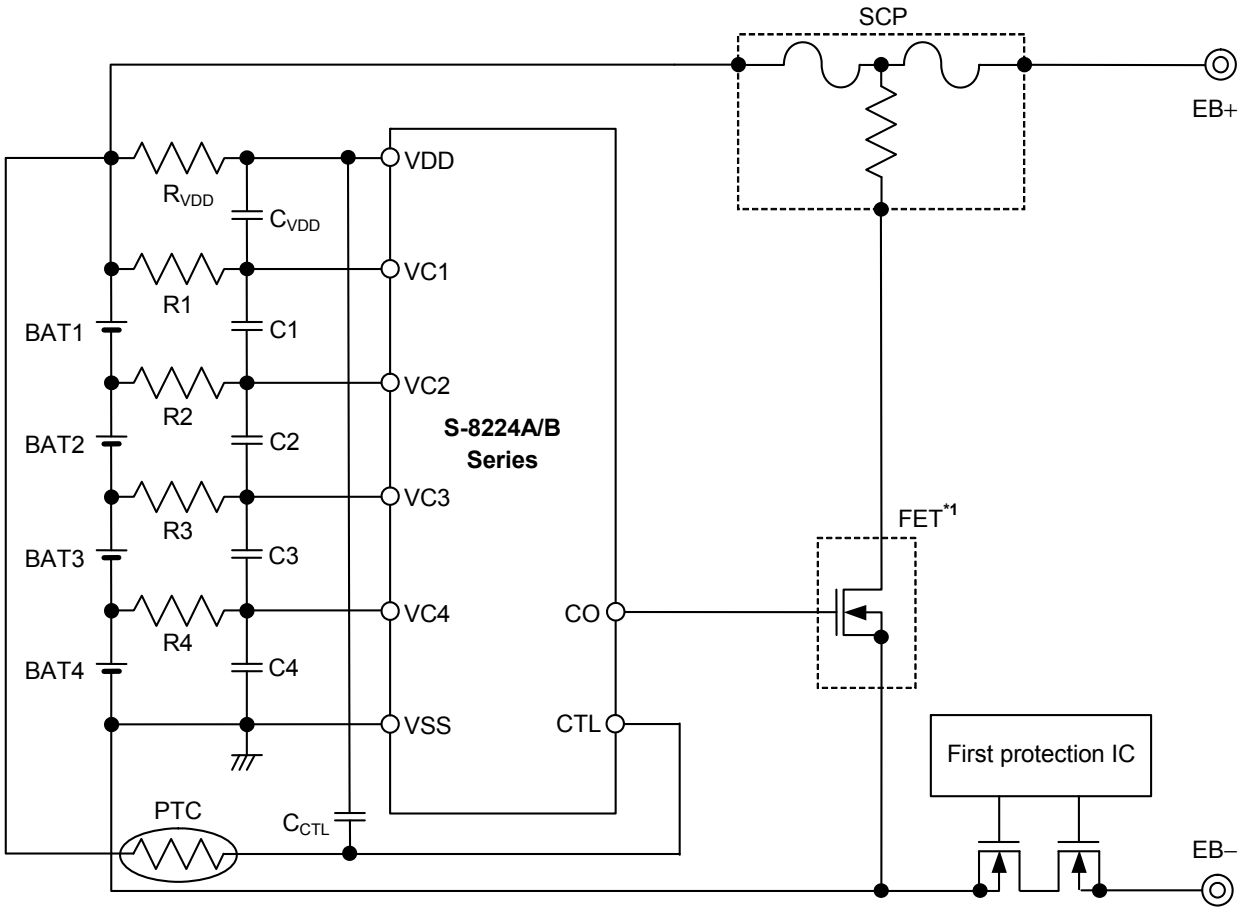
Caution 1. The above constants are subject to change without prior notice.
2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
3. Set the same constants to R1 to R2, and to C1 to C2 and C_{VDD}.
4. Since the CO pin may become detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the protection fuse from cutoff.

■ Precaution

- Do not connect batteries charged with $V_{CU} + V_{HC}$ or higher.
- If the connected batteries include a battery charged with $V_{CU} + V_{HC}$ or higher, the S-8224A/B series may become overcharge status after all pins are connected.
- In some application circuits, even if an overcharged battery is not included, the order of connecting batteries may be restricted to prevent transient output of the CO pin detection pulses when the batteries are connected. Perform thorough evaluation with the actual application circuit.
- Before the battery connection, short-circuit the battery side pins R_{VDD} and R1, shown in the figures in "**■ Battery Protection IC Connection Examples**".
- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Do not apply to this IC an electrostatic discharge that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement of patents owned by a third party by products including this IC.

■ Example of Application Circuit

1. Overheat protection via PTC



***1.** The S-8224B Series limits its CO pin output voltage to 11.5 V max., so a FET with the gate withstand voltage of 12 V can be used.

Figure 17

Caution
1. **The above connection example will not guarantee successful operation. Perform thorough evaluation using the actual application.**
2. **A pull-down resistor is included in the CTL pin. To perform overheat protection via the PTC in the S-8224A/B Series, connect the PTC before connecting batteries.**
3. **When the power fluctuation is large, connect the power supply of the PTC to the VDD pin of the S-8224A/B Series.**
4. **Since the CO pin may become detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.**

[For SCP, contact]

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Thermistor Products Department
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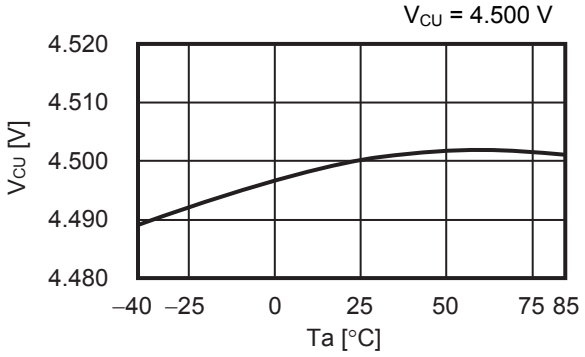
TEL +81-75-955-6863
Contact Us: http://www.murata.com/contact/index.html

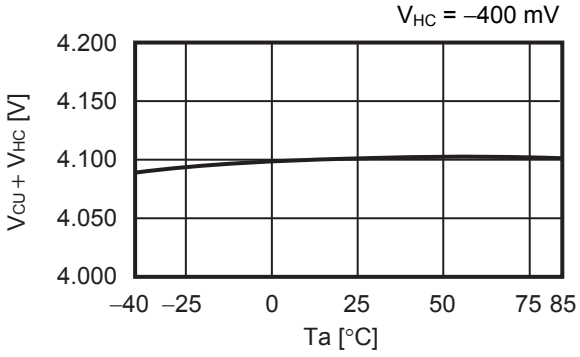
■ Characteristics (Typical Data)

1. Detection voltage

1. 1 V_{CU} vs. Ta

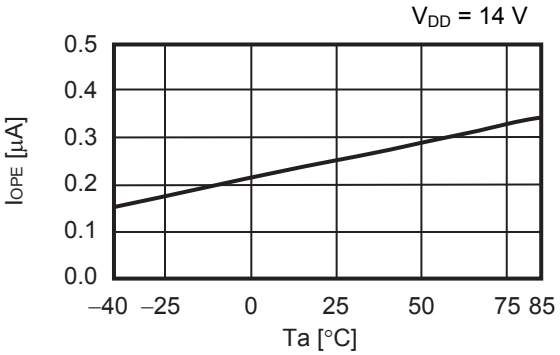


1. 2 $V_{CU} + V_{HC}$ vs. Ta

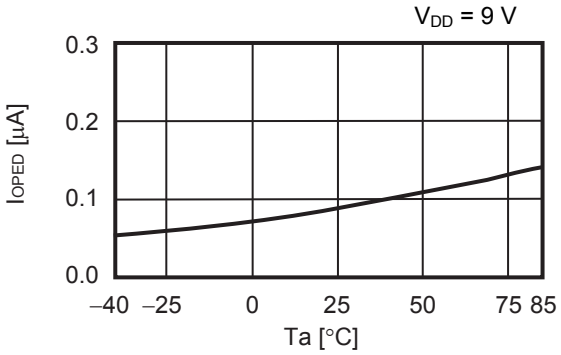


2. Current consumption

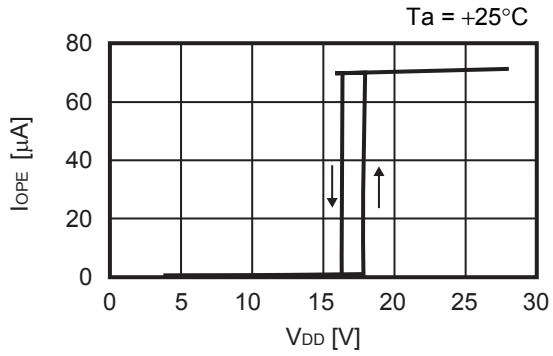
2. 1 I_{OPE} vs. Ta



2. 2 I_{OPED} vs. Ta

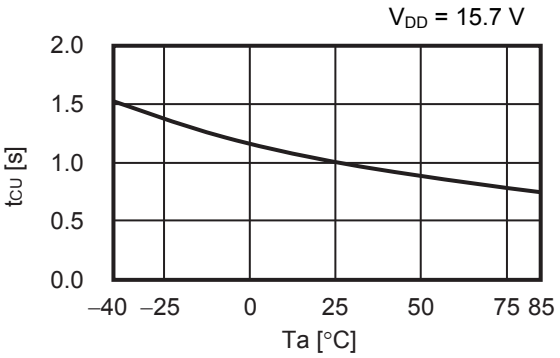


2. 3 I_{OPE} vs. V_{DD}



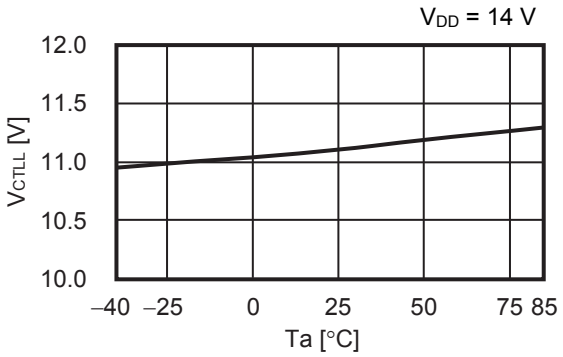
3. Delay time

3. 1 t_{CU} vs. Ta

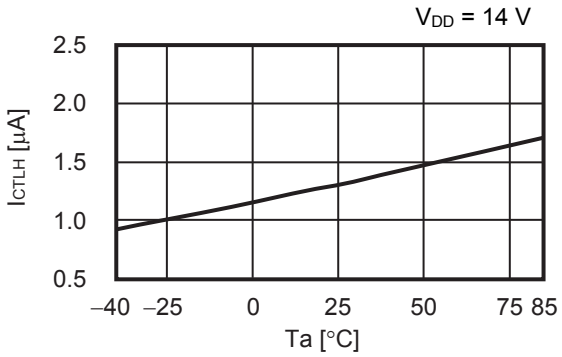


4. CTL pin

4. 1 V_{CTLL} vs. Ta

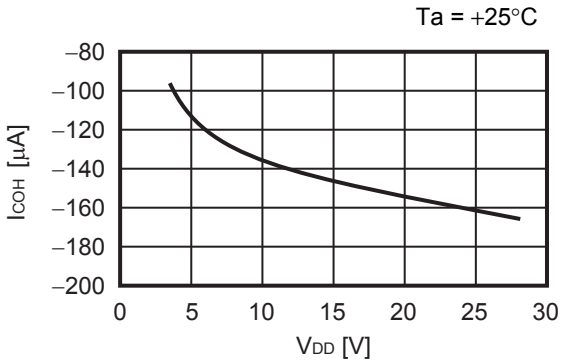


4. 2 I_{CTLH} vs. Ta

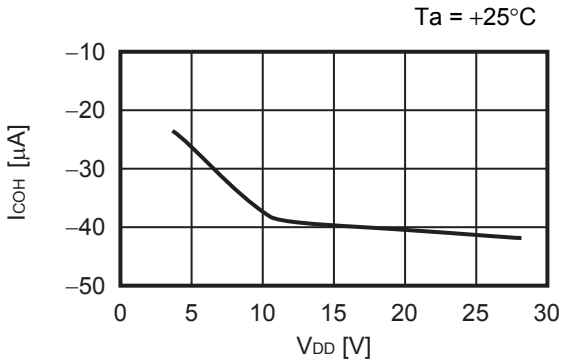


5. Output current

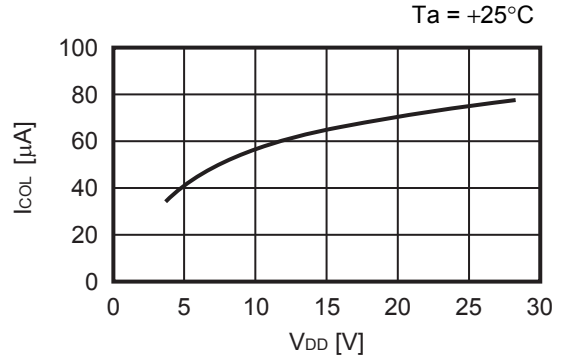
5. 1 I_{COH} vs. V_{DD} (S-8224A Series)



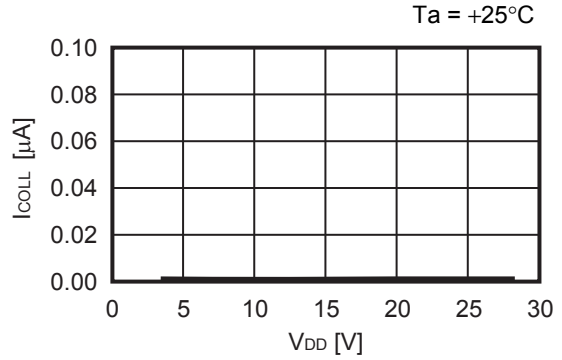
5. 2 I_{COH} vs. V_{DD} (S-8224B Series)



5. 3 I_{COL} vs. V_{DD}

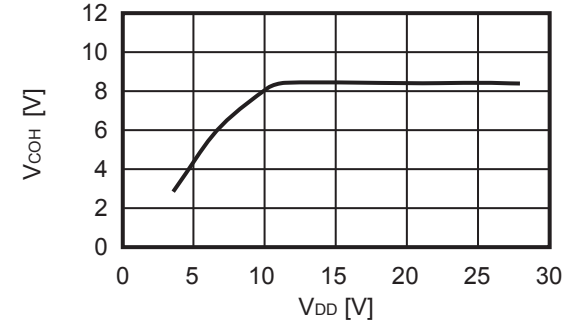


5. 4 I_{COLL} vs. V_{DD}



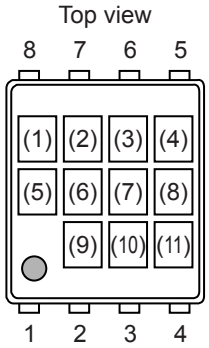
6. Output voltage

6. 1 V_{COH} vs. V_{DD}



■ Marking Specifications

1. SNT-8A



(1)	Blank
(2) to (4)	Product code (Refer to **Product name vs. Product code**)
(5), (6)	Blank
(7) to (11)	Lot number

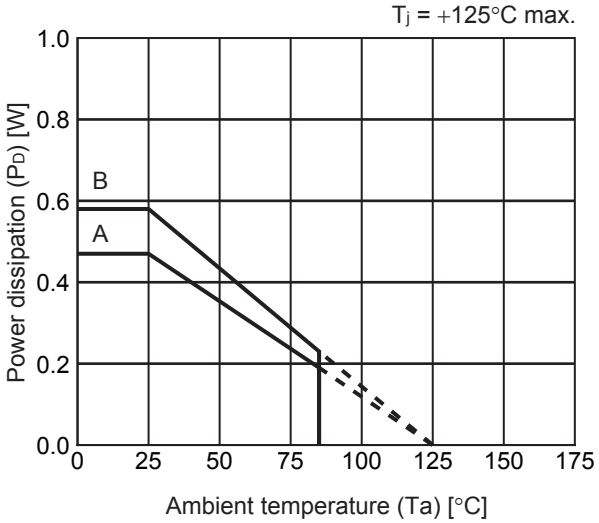
Product name vs. Product code

Product name	Product code		
	(2)	(3)	(4)
S-8224AAS-I8T1U	5	R	S
S-8224AAT-I8T1U	5	R	T
S-8224AAU-I8T1U	5	R	U
S-8224AAV-I8T1U	5	R	V
S-8224AAW-I8T1U	5	R	W
S-8224AAX-I8T1U	5	R	Y
S-8224ABA-I8T1U	6	Z	A
S-8224ABB-I8T1U	6	Z	B
S-8224ABC-I8T1U	6	Z	C
S-8224ABD-I8T1U	6	Z	D

Product name	Product code		
	(2)	(3)	(4)
S-8224BAA-I8T1U	5	S	A
S-8224BAB-I8T1U	5	S	B
S-8224BAC-I8T1U	5	S	C

■ Power Dissipation

SNT-8A

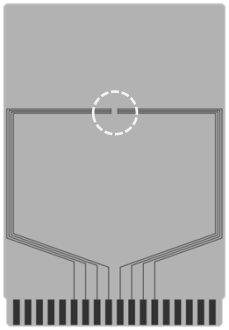


Board	Power Dissipation (P_D)
A	0.47 W
B	0.58 W
C	–
D	–
E	–

SNT-8A Test Board

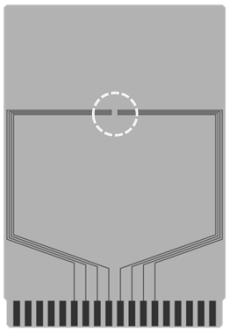
IC Mount Area

(1) Board A



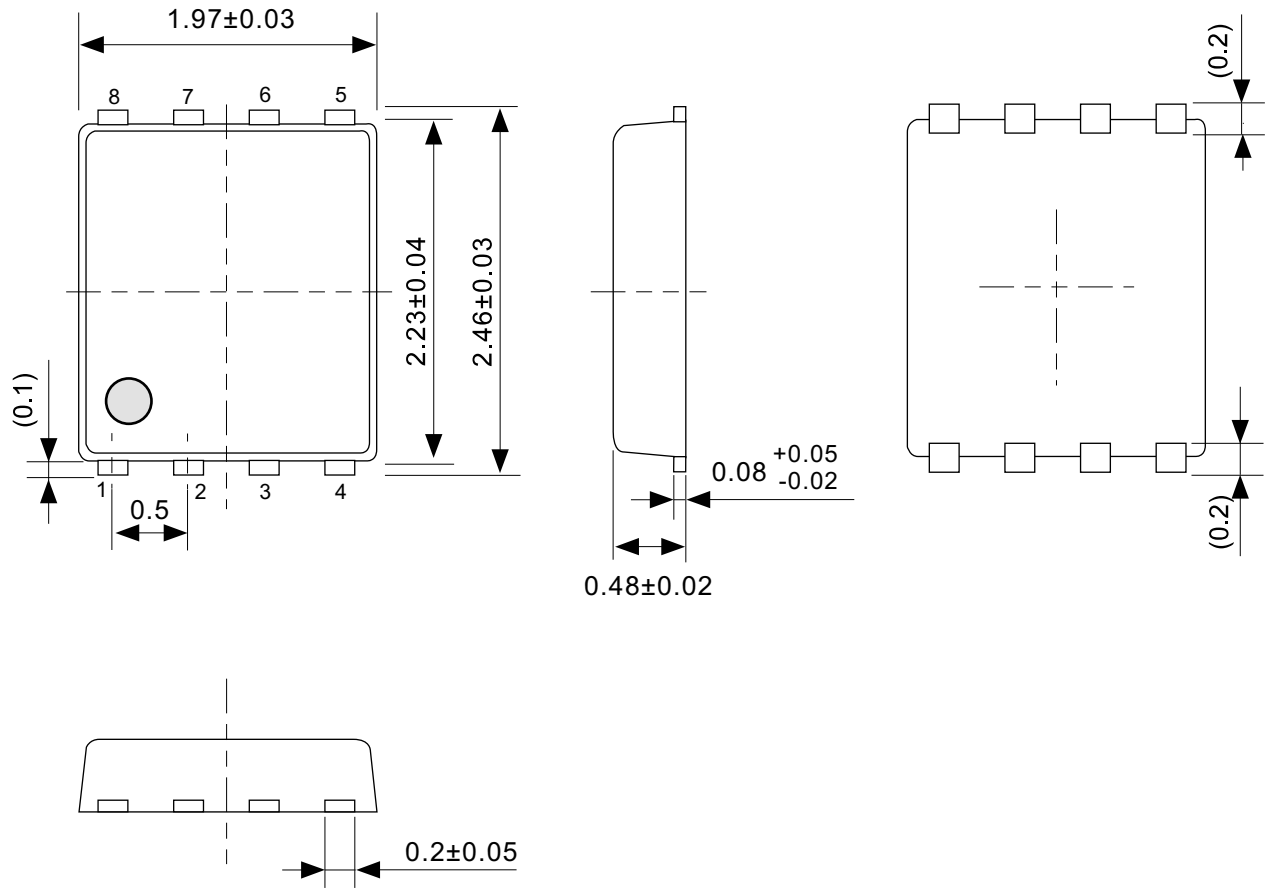
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



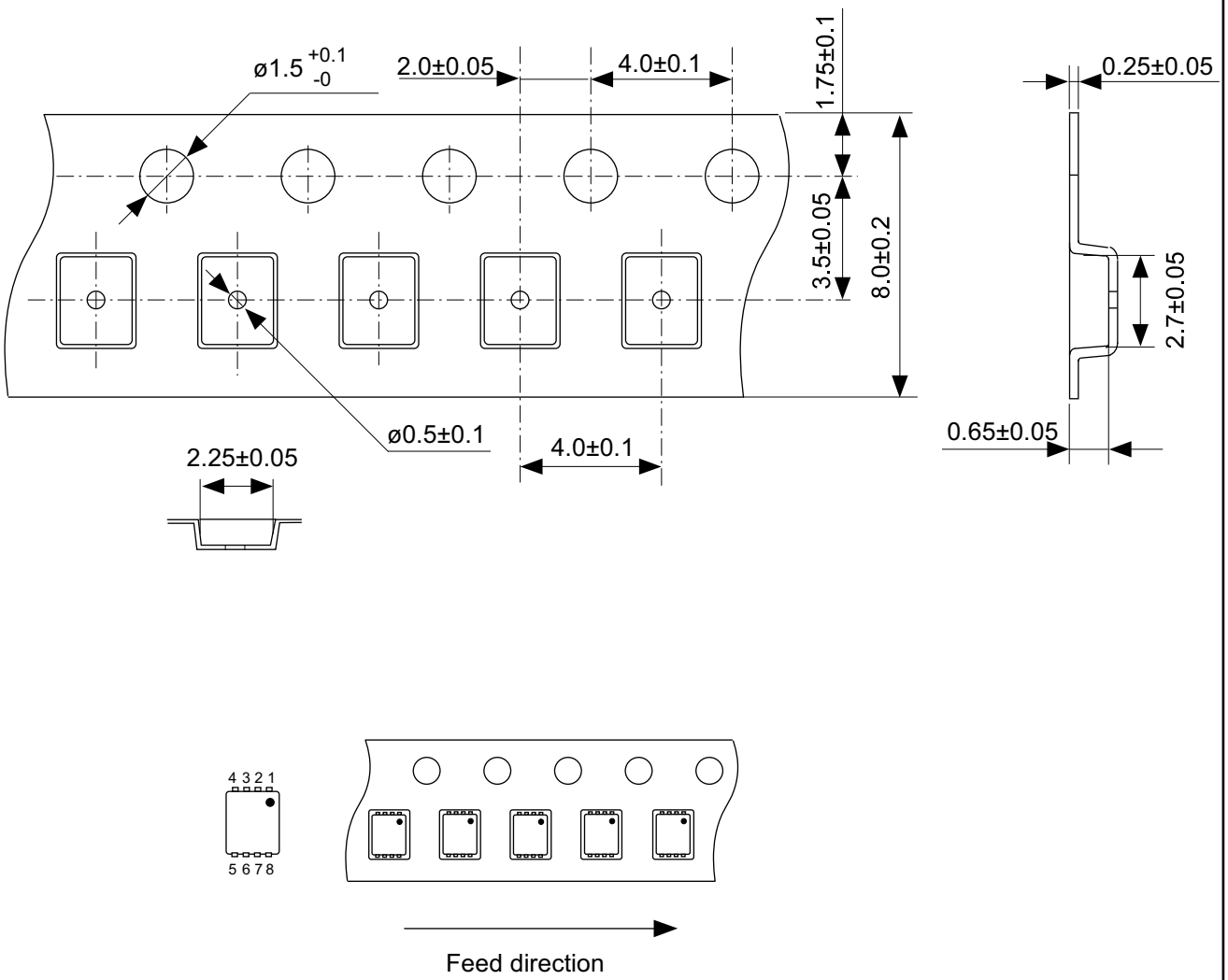
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SNT8A-A-Board-SD-1.0



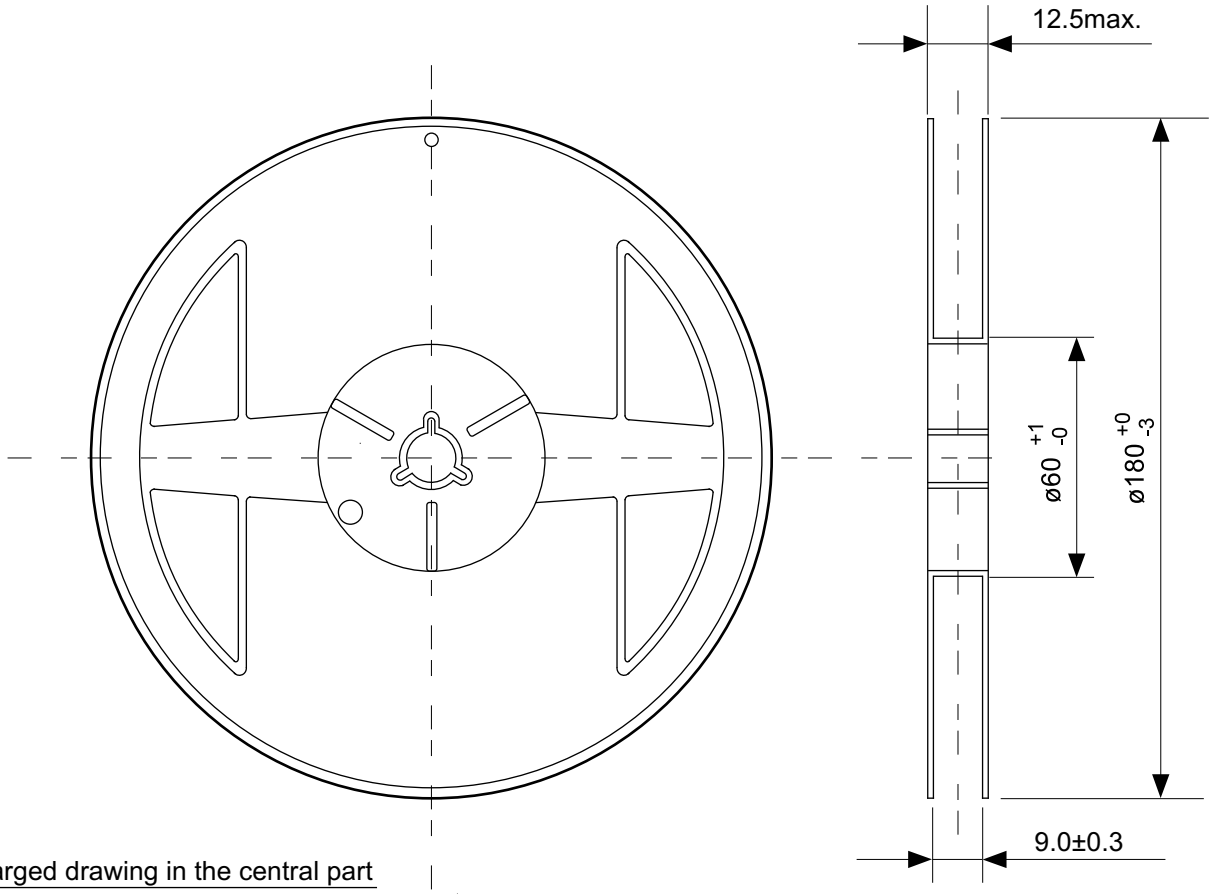
No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

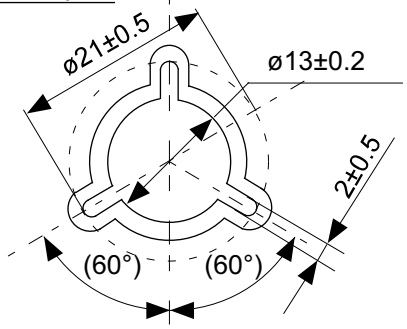


No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

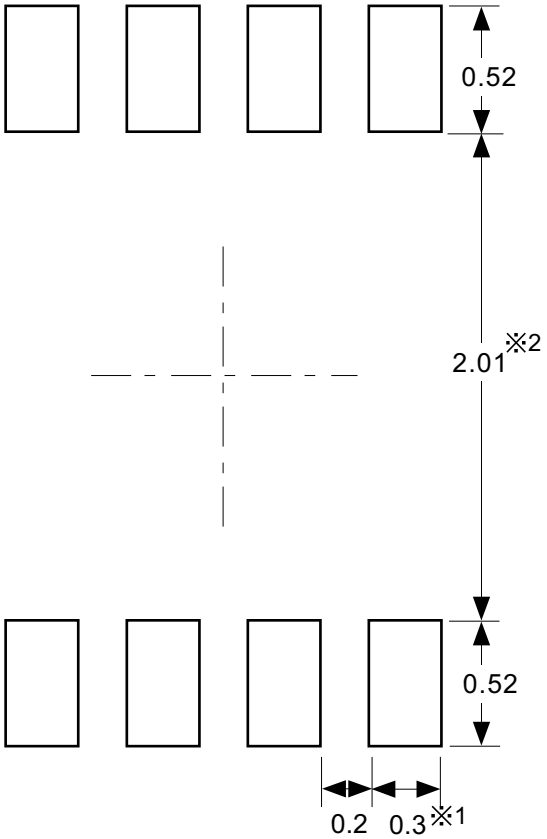


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
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8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
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14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

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