DDR2 SDRAM Data Sheet Addendum

MT47H256M4 – 32 Meg x 4 x 8 banks
MT47H128M8 – 16 Meg x 8 x 8 banks
MT47H64M16 – 8 Meg x 16 x 8 banks

Features

This data sheet addendum provides information to add the X option indicating the Product Longevity Program for data sheet MT47H64M16NF-25E. This addendum does not provide detailed information about the device. Refer to the general market data sheet for a complete description of device functionality, operating modes, and specifications.

- V_{DD} = 1.8V ±0.1V, V_{DDQ} = 1.8V ±0.1V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8
- DLL to align DQ and DQS transitions with CK
- 8 internal banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Selectable burst lengths (BL): 4 or 8
- Adjustable data-output drive strength
- 64ms, 8192-cycle refresh
- On-die termination (ODT)
- Industrial temperature (IT) option
- Automotive temperature (AT) option
- RoHS-compliant
- Supports JEDEC clock jitter specification

Options[1]	Marking
• Configuration	
– 256 Meg x 4 (32 Meg x 4 x 8 banks)	256M4
– 128 Meg x 8 (16 Meg x 8 x 8 banks)	128M8
– 64 Meg x 16 (8 Meg x 16 x 8 banks)	64M16
• FBGA package (Pb-free) – x16	
– 84-ball FBGA (8mm x 12.5mm) Die Rev :H	HR
– 84-ball FBGA (8mm x 12.5mm) Die Rev :M	NF
• FBGA package (Pb-free) – x4, x8	
– 60-ball FBGA (8mm x 10mm) Die Rev :H	CF
– 60-ball FBGA (8mm x 10mm) Die Rev :M	SH
• FBGA package (lead solder) – x16	
– 84-ball FBGA (8mm x 12.5mm) Die Rev :H	HW
• FBGA package (lead solder) – x4, x8	
– 60-ball FBGA (8mm x 10mm) Die Rev :H	JN
• Timing – cycle time	
– 1.875ns @ CL = 7 (DDR2-1066)	-187E
– 2.5ns @ CL = 5 (DDR2-800)	-25E
– 3.0ns @ CL = 5 (DDR2-667)	-3
• Self refresh	
– Standard	None
– Low-power	L
• Special options	
– Product Longevity Program (PLP)	X
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ +85°C)[2]	None
– Industrial (–40°C ≤ T_C ≤ +95°C; –40°C ≤ T_A ≤ +85°C)	IT
• Revision	:H / :M

Notes:
1. Not all options listed can be combined to define an offered product. Use the Part Catalog Search on www.micron.com for product offerings and availability.
2. For extended CT operating temperature see the product data sheet.

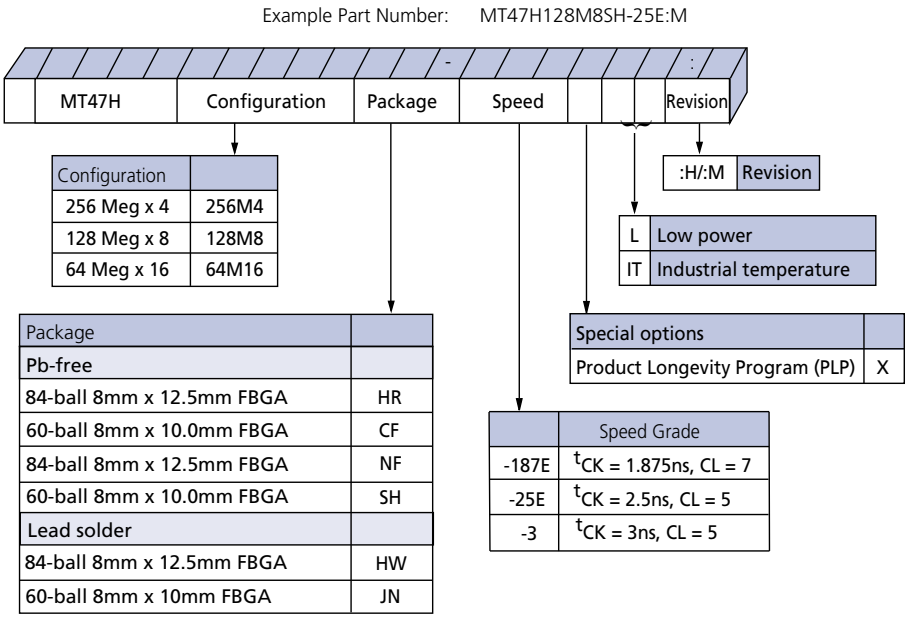
Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)					tRC (ns)
	CL = 3	CL = 4	CL = 5	CL = 6	CL = 7	
-187E	400	533	800	800	1066	54
-25E	400	533	800	800	n/a	55
-3	400	533	667	n/a	n/a	55

Table 2: Addressing

Parameter	256 Meg x 4	128 Meg x 8	64 Meg x 16
Configuration	32 Meg x 4 x 8 banks	16 Meg x 8 x 8 banks	8 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row address	A[13:0] (16K)	A[13:0] (16K)	A[12:0] (8K)
Bank address	BA[2:0] (8)	BA[2:0] (8)	BA[2:0] (8)
Column address	A[11, 9:0] (2K)	A[9:0] (1K)	A[9:0] (1K)

Figure 1: 1Gb DDR2 Part Numbers



Note: 1. Not all speeds and configurations are available in all packages.

FBGA Part Number System

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: http://www.micron.com.

Revision History

Rev. A – 5/14

- Initial release; based on 1Gb: x4, x8, x16 DDR2 SDRAM, Rev. AA 04/14 data sheet (09005aef8565148a)

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-4000
www.micron.com/products/support Sales inquiries: 800-932-4992

This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.